SY8386B

High Efficiency Fast Response, 6A, 28V Input Synchronous Step Down Regulator with 100mA 3.3V LDO

General Description

The SY8386B develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. In addition, it operates at pseudo-constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor. SY8386B also provides a fixed 3.3V LDO with 100mA current capability, which can be used to power the external peripheries, such as the keyboard controller in notebook. The 3.3V LDO can switch over to Buck regulator output to save power loss.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY8386B operates over a wide input voltage range from 4.5V to 24V. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection, over voltage protection and thermal shutdown provide safe operation in all operating conditions.

Ordering Information

SY8386 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8386BRHC	QFN2.5×2.5-16	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (top/bottom): 36/18 mΩ
- Wide Input Voltage Range: 4.5~24V
- Integrated Bypass Switch: 1.2Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz
- Fixed 3.338V Output Voltage
- 6A Output Current Capability
- 100mA LDO Current Capability
- ±1% Internal Reference Voltage
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Discharge Function
- Cycle-by-cycle Valley and Peak Current Limit Protection
- Latch-off Mode Output Under Voltage Protection for Buck
- Latch-off Mode Output Over Voltage Protection for Buck
- Latch-off Mode Over Temperature Protection for Buck
- Auto-recovery Mode Output Under Voltage Protection for LDO
- Auto-recovery Mode Over Temperature Protection for LDO
- Input Under Voltage Lock-out(UVLO)
- RoHS Compliant and Halogen Free
- Compact package: QFN2.5×2.5-16

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

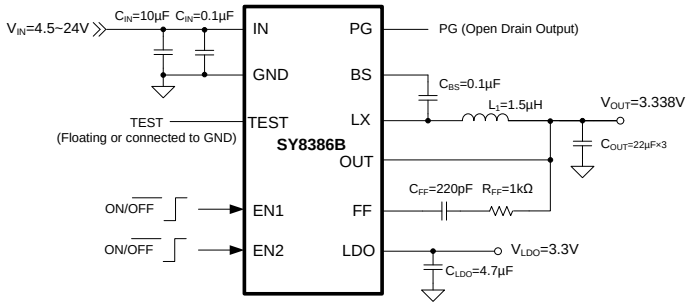


Figure1. Schematic Diagram

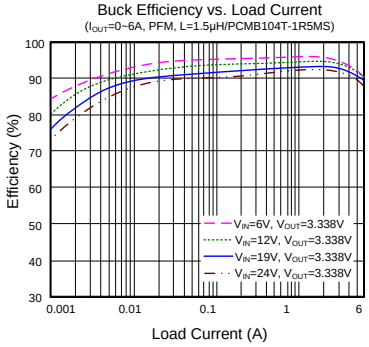
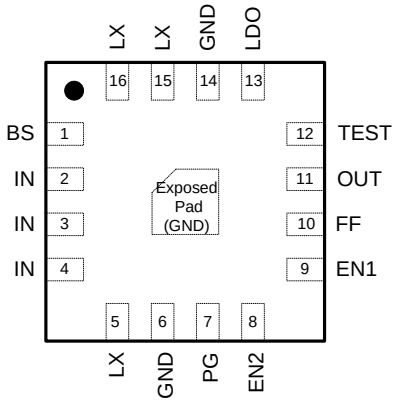


Figure2. Buck Efficiency vs. Load Current

Pinout (top view)



(QFN2.5×2.5-16)

Top Mark: Qq*xyz*, (Device code: Qq, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
IN	2, 3, 4	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.
LX	5, 15, 16	Inductor pin. Connect this pin to the switching node of the inductor.
GND	6, 14, EP	Ground pin.
PG	7	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
EN2	8	Enable control of the IC and internal LDO. Pulling this pin high to turn on the IC and internal LDO. Do not leave this pin floating.
EN1	9	Enable control of the Buck regulator. Pulling this pin high to turn on the regulator. Do not leave this pin floating. The pin is also used for controlling operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. When its voltage is less than 1.6V, the Buck regulator works under ultra-sonic mode. When its voltage is larger than 2.2V, the Buck regulator works under PFM mode.
FF	10	Output feed forward pin. Connect the RC network from the output to this pin.
OUT	11	Output pin. Connect to the output of Buck regulator. This pin also provides the bypass input for internal LDO.
TEST	12	For factory use only. Leave this pin floating or connect it to GND in application.
LDO	13	3.3V LDO output. Decouple this pin to ground with at least a 4.7μF capacitor.

Block Diagram

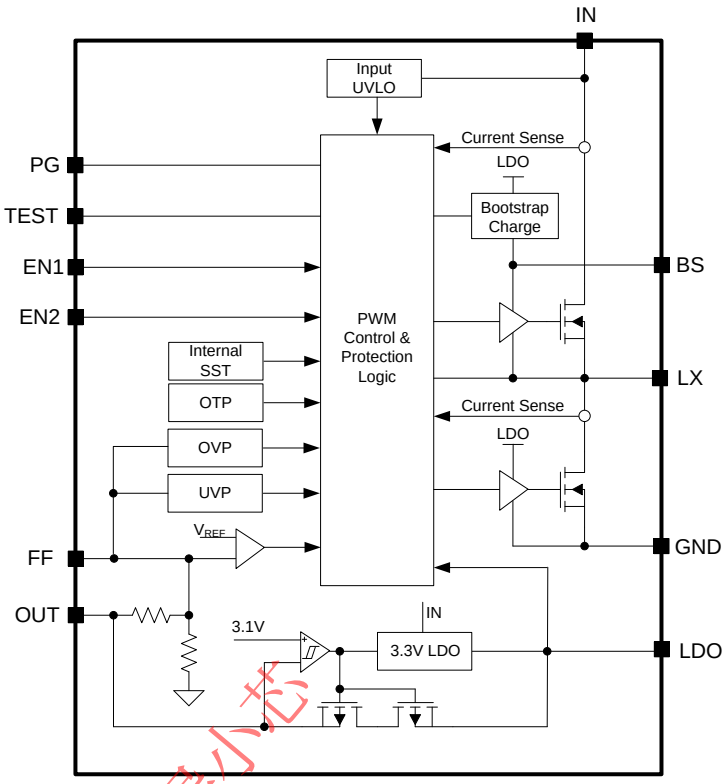


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 28V
IN-LX, LX, PG, EN2, EN1 Voltage---------- -0.3V to 26V
BS-LX, LDO Voltage---------- -0.3V to 4V
OUT, FF, TEST Voltage---------- -0.3V to 6V
Maximum Power Dissipation, $P_{D,MAX,}$ @ T_A = 25°C QFN2.5×2.5-16 ---------- 3W
Package Thermal Resistance (Note 2)
$\theta_{JA,}$ QFN2.5×2.5-16 ---------- 33°C/W
$\theta_{JC,}$ QFN2.5×2.5-16 ---------- 5.5°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration ---------- -5V to 29V
Dynamic LX Voltage in 20ns Duration ---------- -1V to 28V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 24V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, C_{OUT}= 66µF, C_{FF}=220pF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		24	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			4.2	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Quiescent Current	I_Q	I_{OUT}=0A, EN2=EN1=1, V_{OUT}=V_{SET}×105%		75	90	µA
Shutdown Current 1	I_{SHDN1}	EN2=1, EN1=0		40	50	µA
Shutdown Current 2	I_{SHDN2}	EN2=0, EN1=0		6	10	µA
Output Voltage Set-point	V_{SET}	CCM	3.305	3.338	3.371	V
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			36		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			18		mΩ
Output Discharge Current	I_{DIS}	V_{OUT}=3.338V		90		mA
Top FET Current Limit	$I_{LMT,TOP}$		12			A
Bottom FET Current Limit	$I_{LMT,BOT}$		8			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$	USM mode		4		A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%V_{SET}		1.2		ms
EN2/EN1 Input Voltage High	$V_{EN,H}$		1			V
EN2/EN1 Input Voltage Low	$V_{EN,L}$				0.4	V
EN1 Voltage for Ultra-sonic Mode	$V_{EN1,USM}$		1		1.6	V
EN1 Voltage for PFM Mode	$V_{EN1,PFM}$		2.2		V_{IN}	V
Internal EN1 Resistor to GND	R_{EN1}			2.5		MΩ
Switching Frequency	f_{SW}		510	600	690	kHz
Ultra-sonic Mode Frequency	f_{USM}	USM mode, I_{OUT}=0A		27		kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=V_{INMAX} (Note 4)		50		ns
Min OFF Time	$t_{OFF,MIN}$			150		ns
Output Over Voltage Threshold	V_{OVP}	V_{FF} rising	117	120	123	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			5		%V_{REF}
Output OVP Delay	$t_{OVP,DLY}$	(Note 4)		20		µs
Output Under Voltage Protection Threshold	V_{UVP}		55	60	65	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$	(Note 4)		200		µs
Power Good Rising Threshold	$V_{PG,R}$	V_{FF} rising (good)	86	90	94	%V_{REF}
Power Good Falling Threshold	$V_{PG,F}$	V_{FF} falling	81	85	89	%V_{REF}
Power Good Delay	$t_{PG,R}$	Low to high (Note 4)		200		µs
	$t_{PG,F}$	High to low (Note 4)		10		µs
Power Good Low Voltage	$V_{PG,LOW}$	V_{FF}=0V, I_{PG}=5mA			0.4	V
LDO Output Voltage	V_{LDO}	V_{IN}=12V, I_{LDO}=30mA	3.15	3.3	3.45	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=100mA		300		mV
LDO Output Current Limit	$I_{LMT,LDO}$		130		400	mA
Bypass Switch $R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.2		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		2.9	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP,HYS}$			0.2		V
Bypass Switch OVP Voltage	$V_{BYP,OVP}$			120		%V_{LDO}
Over Temperature Protection Temperature	T_{OTP}	T_J rising (Note 4)		150		°C
Over Temperature Protection Recovery Hysteresis	$T_{OTP,HYS}$	(Note 4)		15		°C

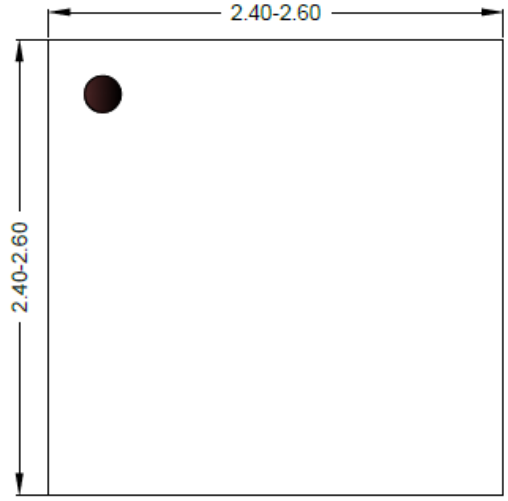
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

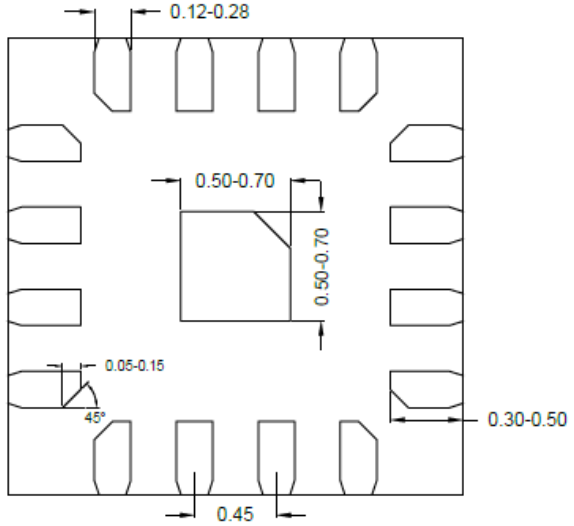
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

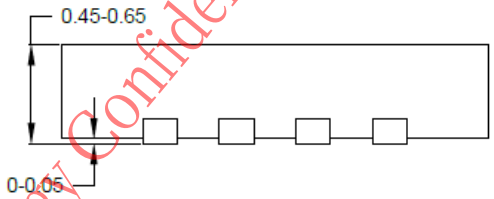
QFN2.5×2.5-16 Package Outline Drawing



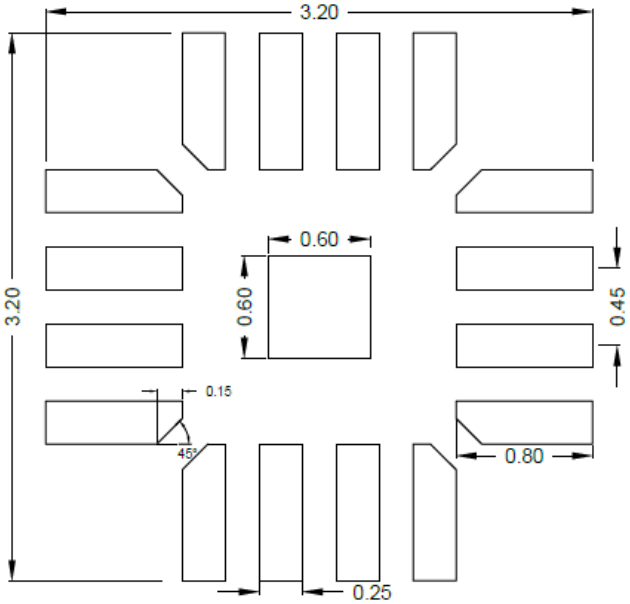
Top view



Bottom view



Side view

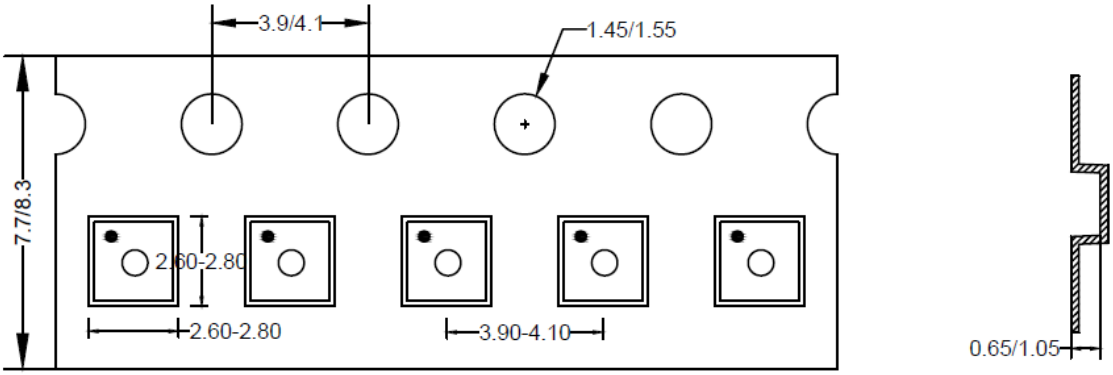


Recommended PCB Layout
(Reference only)

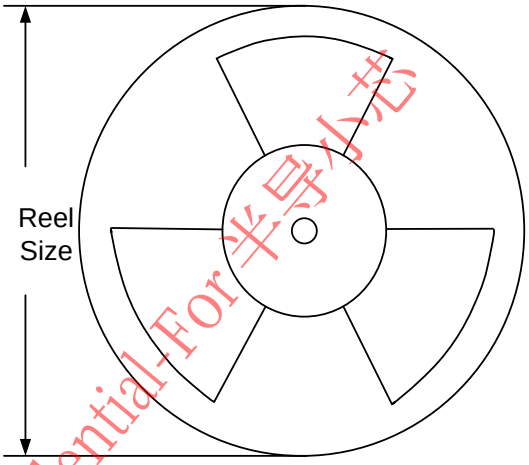
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN2.5×2.5 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5×2.5	8	4	7”	400	160	3000

3. Others: NA