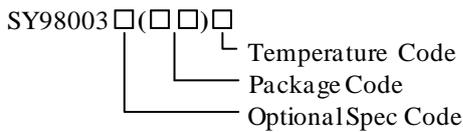


General Description

The SY98003A is a 3MHz, 3A synchronous step-down converter which integrates an inductor and a control IC in one tiny package (3.0mm×3.0mm, H=1.1mm max). It operates over a wide input voltage range from 2.75V to 5.5V. It integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information



Ordering Number	Package	Note
SY98003AQNC	QFN3×3-10	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 35/15 mΩ
- 2.75-5.5V Input Voltage Range
- 3 MHz Switching Frequency Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 3A Continuous Output Current Capability
- Shutdown Mode Draws <math><0.1\mu\text{A}</math> Supply Current
- 100% Dropout Operation
- Power Good Indicator
- OCP/UVLO/OTP Protections
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×3-10

Applications

- Mobile Phone, Smart Phone
- Bluetooth Headsets
- WiMAX PDA, MID, UMPC
- Portable Game Console
- Digital Camera, Camcorder

Typical Applications

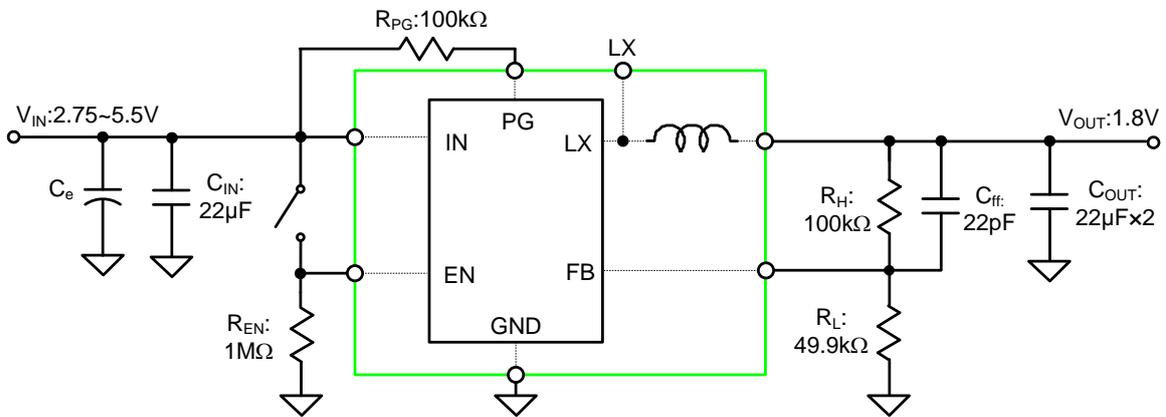
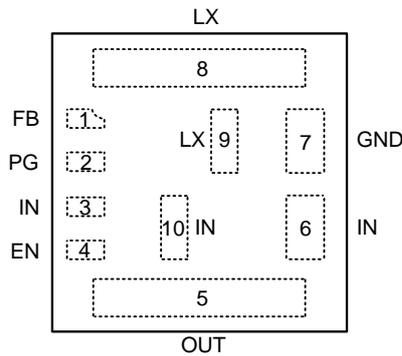


Figure1. Schematic Diagram

Pinout (top view)



(QFN3×3-10)

Top Mark: DCMxyz for SY98003A (device code: DCM, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Fig.1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$.
PG	2	Power good indicator, open drain. When the output voltage exceeds 90% of regulation point, it becomes high, low otherwise.
IN	3,6,10	Power input pin.
EN	4	Enable control. Pulled high to turn on. Do not leave it floating.
OUT	5	Output pin. Decouple this pin to the ground with at least a 40μF ceramic capacitor.
GND	7	Ground pin.
LX	8,9	Built-in inductor node. Leave it floating.

Absolute Maximum Ratings (Note 1)

IN, LX	-----	6.0V
All other pins	-----	$V_{IN} + 0.5V$
Power Dissipation, P_D @ $T_A = 25^\circ C$ QFN3×3	-----	2W
Package Thermal Resistance (Note 2)		
θ_{JA}	-----	50 $^\circ C/W$
θ_{JC}	-----	5 $^\circ C/W$
Junction Temperature Range	-----	150 $^\circ C$
Lead Temperature (Soldering, 10 sec.)	-----	260 $^\circ C$
Storage Temperature Range	-----	-65 $^\circ C$ to 150 $^\circ C$

Recommended Operating Conditions (Note 3)

Supply Input Voltage	-----	2.75V to 5.5V
Junction Temperature Range	-----	-40 $^\circ C$ to 125 $^\circ C$
Ambient Temperature Range	-----	-40 $^\circ C$ to 85 $^\circ C$

Electrical Characteristics

($V_{IN} = 5V$, $V_{OUT} = 2.5V$, $C_{OUT} = 22\mu F \times 2$, $T_A = 25^\circ C$, $I_{OUT} = 1A$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.75		5.5	V
Quiescent Current	I_Q	$I_{OUT}=0$, $EN=1$, $FB=105\% \times V_{REF}$		68		μA
Shutdown Current	I_{SHDN}	$EN=0$		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)N}$			15		m Ω
PFET $R_{DS(ON)}$	$R_{DS(ON)P}$			35		m Ω
Input Peak Current Limit	I_{LIM}		4.5			A
Internal soft-start Time	t_{SS}			0.8		ms
PGOOD Under-voltage Threshold	$V_{FB, LV}$			0.54		V
Short Circuit Protection Threshold	V_{SCP}			0.25		V
Min ON Time				60		ns
Max Duty Cycle			100			%
EN Rising Threshold	V_{ENH}		1.2			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.75	V
UVLO Hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	f_{OSC}			3		MHz
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			15		$^\circ C$
LX Node Discharge Resistor	R_{DSH}			50		Ω

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

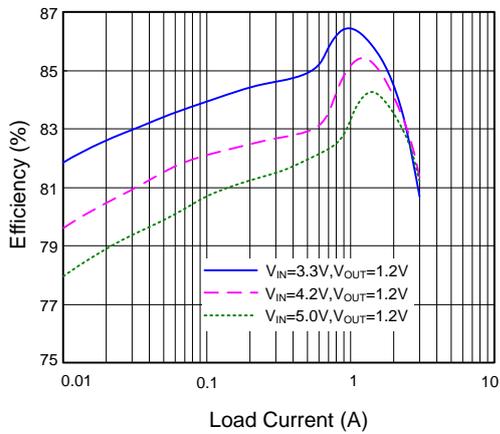
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of QFN3 \times 3-10 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

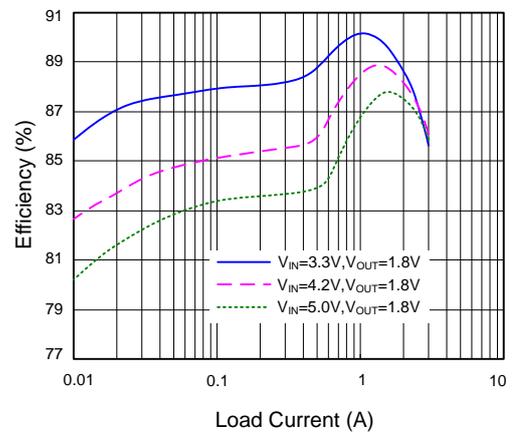
Typical Performance Characteristics

($T_A=25\text{ }^\circ\text{C}$, the divider resistor is shown in Table1, unless otherwise noted.)

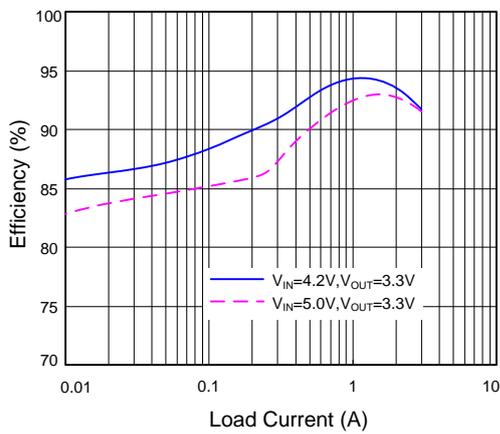
Efficiency vs. Load Current



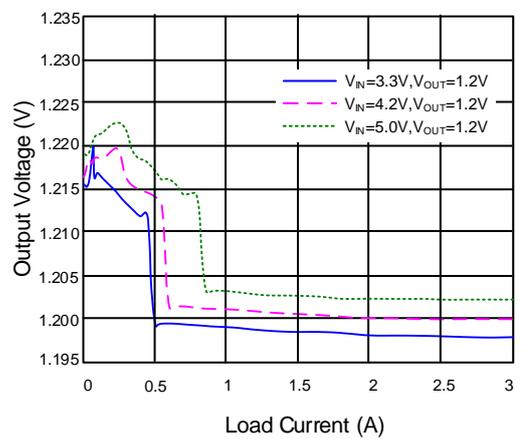
Efficiency vs. Load Current



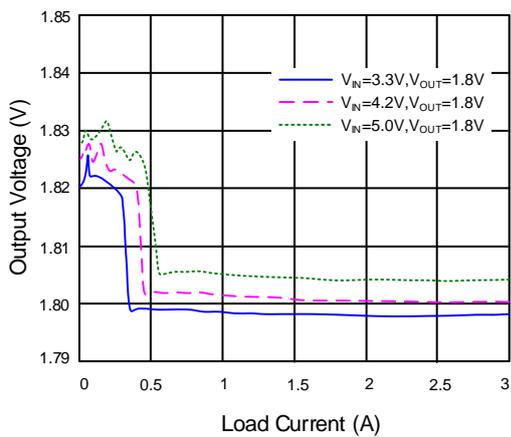
Efficiency vs. Load Current



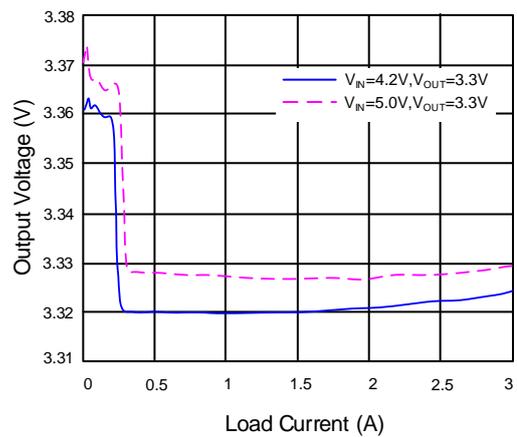
Load Regulation



Load Regulation

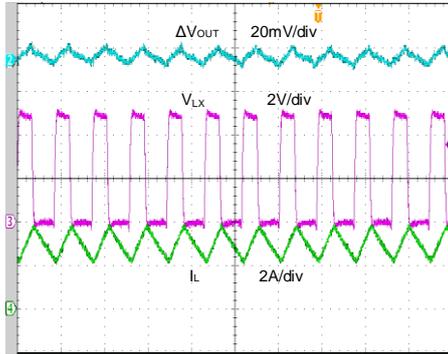


Load Regulation



Output Ripple

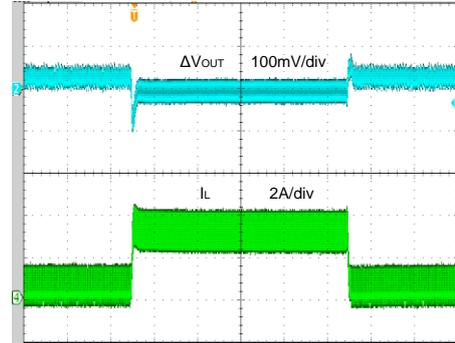
($V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=3.0A$)



Time (400ns/div)

Load Transient

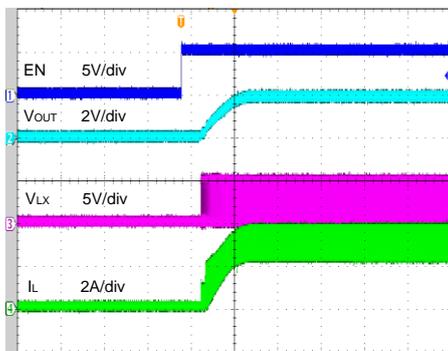
($V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=0.3 \sim 3.0A$)



Time (100µs/div)

Startup From Enable

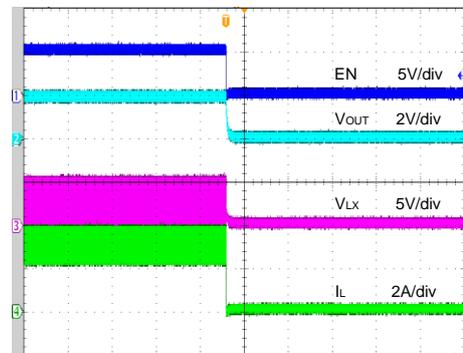
($V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=3.0A$)



Time (800µs/div)

Shutdown from Enable

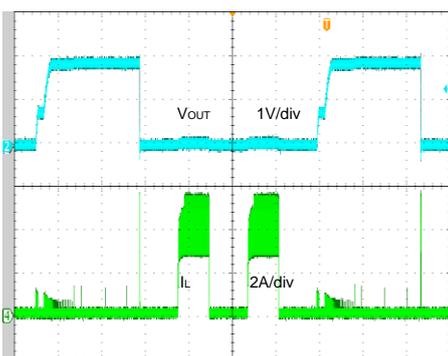
($V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=3.0A$)



Time (800µs/div)

Short Circuit Protection

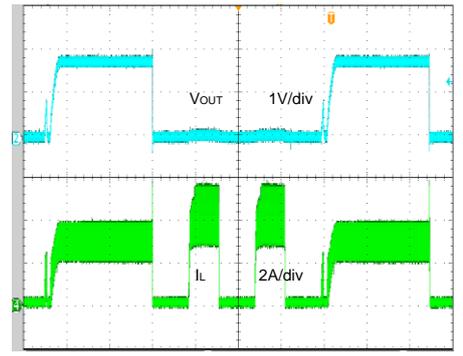
($V_{IN}=5.0V, V_{OUT}=1.8V, 0A$ to Short)



Time (4ms/div)

Short Circuit Protection

($V_{IN}=5.0V, V_{OUT}=1.8V, 3.0A$ to Short)



Time (4ms/div)

Operation

The SY98003A is a 3MHz, 3A synchronous step-down converter which integrates an inductor and a control IC in one tiny package (3.0mm×3.0mm, H=1.1mm max). It operates over a wide input voltage range from 2.75V to 5.5V. It integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in the SY98003A, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN} and the output capacitor C_{OUT} and the feedback resistors (R_H and R_L) need to be selected for the targeted application specifications.

Feedback Resistor Dividers R_H and R_L :

Choose R_H and R_L to program the proper output voltage. A value of between 90kΩ and 1MΩ is highly recommended for R_H resistor. If R_L is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \times R_L}{0.6V}$$

Table1. Divider Resistor Recommendation

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)
3.3	100	22.1
1.8	100	49.9
1.2	100	100

The SY98003A operates in PFM (Pulse Frequency Mode) at light load condition to save power loss. In PFM, the power FETs stop switching when V_{OUT} is higher than the regulation voltage. And the switching will be suspended for a span of time depending on the load condition. Once detected output voltage is dropping out of the regulation, the switching will continue to ramp up the output voltage. The average output voltage is a little higher than the reference voltage consequently in PFM. Specially, if the SY98003A application load current is within PFM range and the output voltage accuracy is a concerned requirement, below adjusted feedback resistor divider values are recommended:

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)	Typical I_{OUT} Range in PFM for 5V Input(A)
3.3	98	22.1	0~0.3
1.8	98	49.9	0~0.6
1.2	98	100	0~1

Input Capacitor C_{IN} :

A typical X7R or better grade ceramic capacitor greater than 10μF capacitance is recommended. To minimize the potential noise problem, this ceramic capacitor should be placed really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and the IN/GND pins.

Output Capacitor C_{OUT} :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X7R or better grade ceramic capacitor with 6V rating and greater than 40μF capacitance.

Load Transient Considerations:

The SY98003A integrates the compensation components to achieve good stability and fast transient response. In some applications, adding a 22pF ceramic capacitor in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

For the minimum noise problems, the following components should be placed close to the IC: C_{IN} and C_{OUT} .

- 1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C_{IN} must be close to the IN and the GND pins. The loop area formed by C_{IN} and the GND must be minimized.
- 3) Connect the LX pins together to reduce the inductor DCR. It is strongly recommended to reduce the LX routing area to avoid the potential noise problem.
- 4) The trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FB pin.

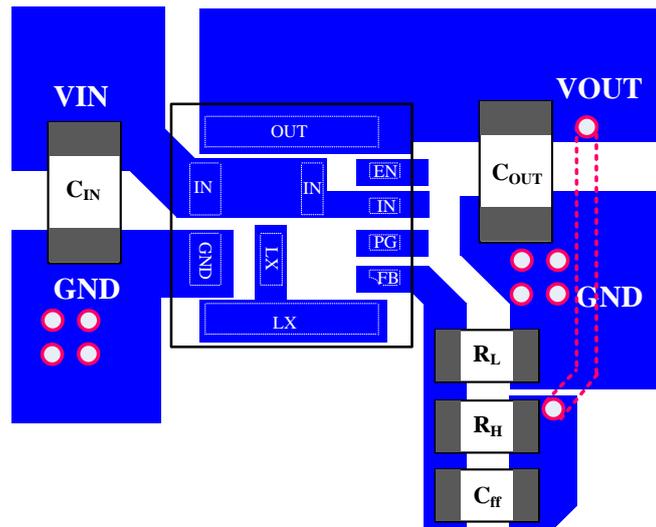
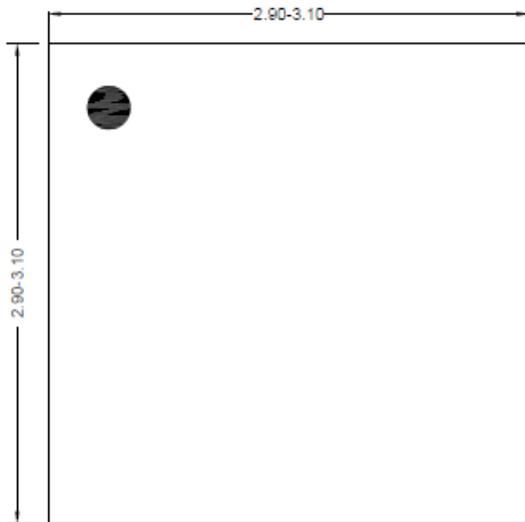
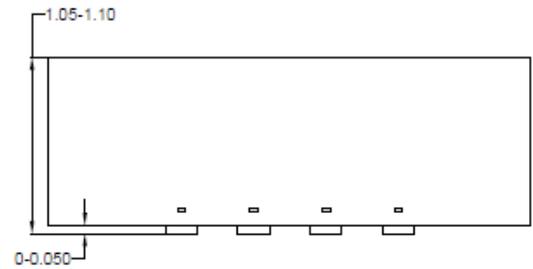


Figure2. PCB Layout Suggestion

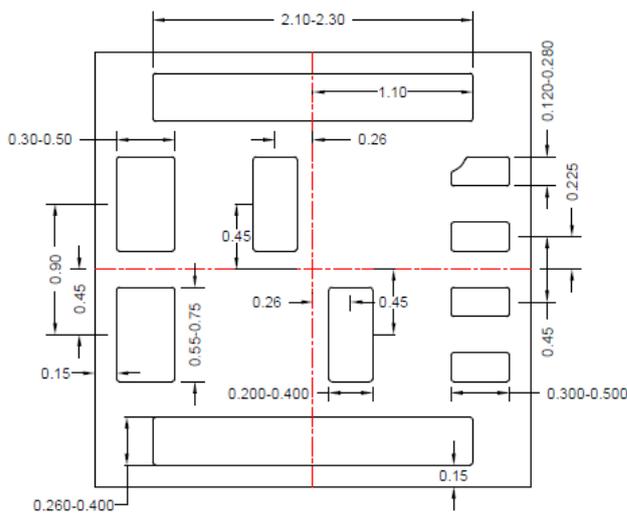
QFN3×3-10 Package Outline Drawing



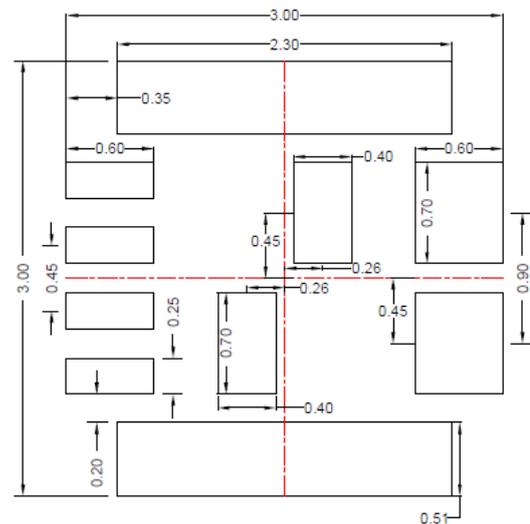
Top View



Front view



Bottom View



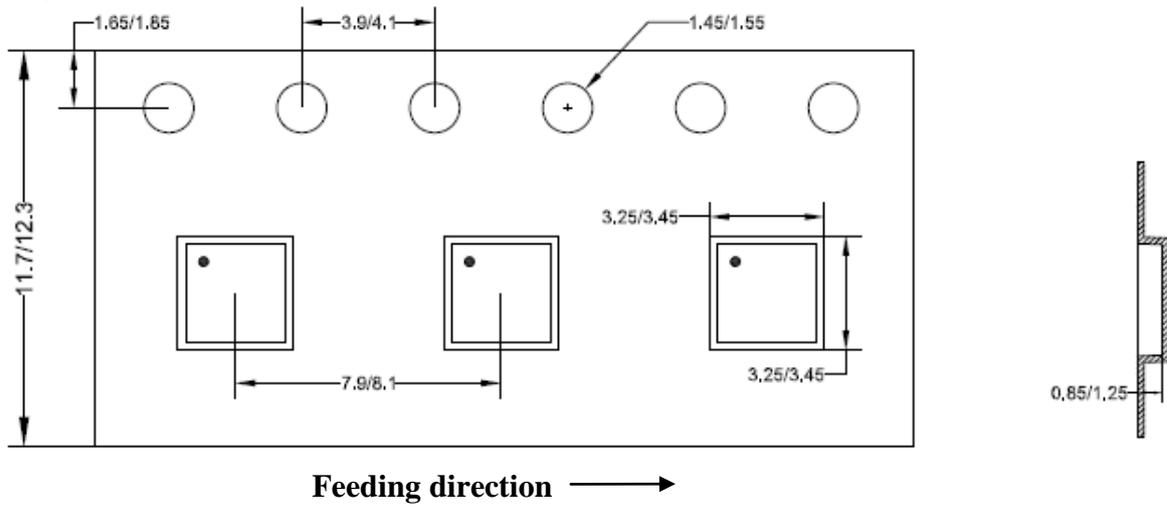
**Recommended PCB layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

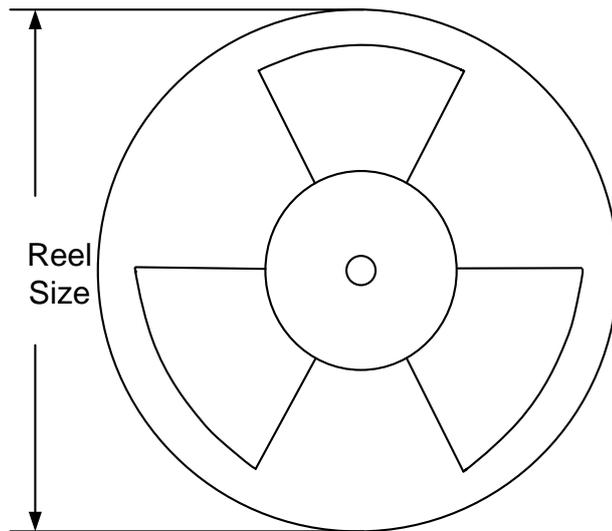
Taping & Reel Specification

1. Taping orientation

QFN3×3



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.17, 2020	Revision 0.9B	1. Add Load Regulation waveforms in page 4. 2. Update the “Feedback Resistor Dividers R_H and R_L ” operation information in page 6
Feb. 17, 2020	Revision 0.9A	Update POD information
Oct. 8, 2019	Revision 0.9	Initial Release

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