Application Note: SY98103A

High Efficiency, Built-in Inductor, 1MHz, 3A, 18V Input Synchronous Step Down Regulator

General Description

SY98103A is a high efficiency, 1MHz synchronous step down DC/DC converter capable of delivering 3A current, which integrates an inductor into a compact 3×3×2mm package. The SY98103A operates over a wide input voltage range from 4.5V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY98103A features enable control. The device also provides cycle-by-cycle current limit, short circuit protection and thermal shutdown protection for reliable operation.

Ordering Information

SY98103□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY98103ATRC	QFN3×3-7	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 50mΩ/30mΩ
- 4.5-18V Input Voltage Range
- 3A load Current Capability
- ±1% 0.6V Reference
- Pseudo-constant Frequency:1MHz
- Instant PWM Architecture to Achieve Fast Transient Responses.
- Internal Soft-start Limits the Inrush Current
- Current Limit Fold-back Mode Output Short Circuit Protection
- Over Temperature Protection with Auto Recovery
- Cycle-by-cycle Peak Current Limitation
- Input UVLO
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×3-7

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV
- Telecom Applications

Typical Applications

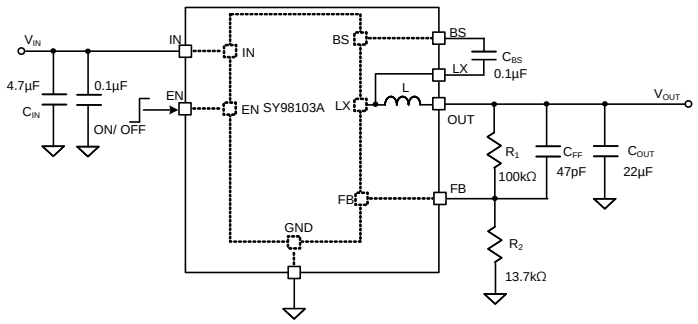


Figure1. Schematic Diagram

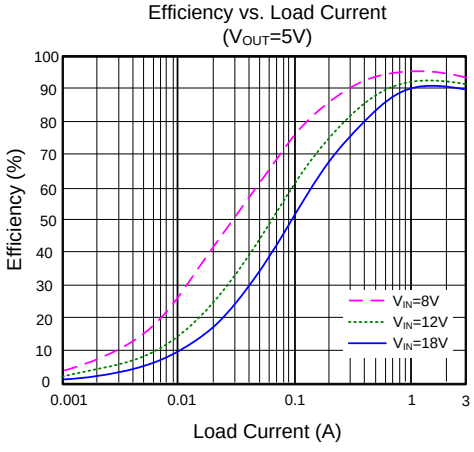
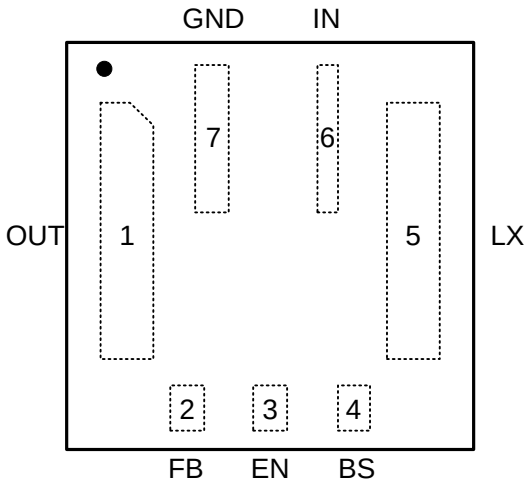


Figure2. Efficiency vs. Load Current

Pinout (top view)



(QFN3×3-7)

Top Mark: **CJA*xyz***, **(**Device code: CJA; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
OUT	1	Output pin. Decouple this pin to ground with at least a 22μF MLCC.
FB	2	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{SET}=0.6\times(1+R_1/R_2)$.
EN	3	Enable control. Pull high to turn on. Do not leave it floating.
BS	4	Boot-strap pin. Supply high side gate driver. Decouple this pin to LX pin with a 0.1μF ceramic capacitor.
LX	5	Inductor pin. Connect this pin to the switching node of the inductor.
IN	6	Input pin. Decouple this pin to GND pin with at least a 4.7μF ceramic capacitor.
GND	7	Ground pin.

Block Diagram

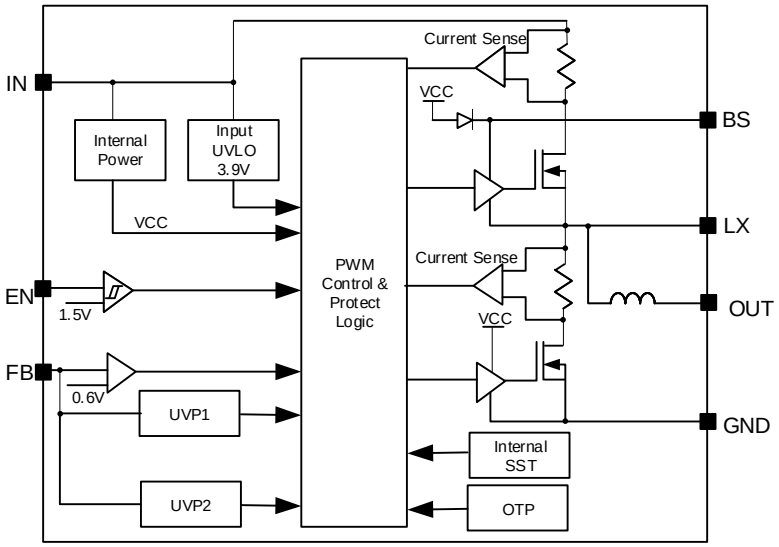


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 19V
BS-LX ---------- 4V
All Other Pins ---------- V_{IN} + 0.3V
Power Dissipation, P_D @ T_A = 25℃, QFN3×3-7---------- 1.75W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 40℃
θ_{JC} ---------- 4℃
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 4)

Supply Input Voltage ---------- 4.5V to 18V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} =5V, C_{OUT} = 22μF, T_A = 25℃, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		18	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		180		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=1V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			50		mΩ
Bottom FET RON	$R_{DS(ON)2}$			30		mΩ
TOP FET Peak Current Limit	$I_{LMT,TOP}$	**(Note 5)**	9.0			A
Bottom FET Valley Current Limit	$I_{LMT,BOT}$			4.0		A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$			-4.0		A
EN Input Voltage High	$V_{EN,\ H}$		1.5			V
EN Input Voltage Low	$V_{EN,\ L}$				0.4	V
Input UVLO Threshold	V_{UVLO}				4.5	V
Input UVLO Hysteresis	V_{HYS}			0.5		V
Output Voltage Range	V_{OUT}	**(Note 6)**	0.6		5.5	V
Output Under Voltage Threshold 1	$V_{UVP,1}$	V_{FB} falling, $I_{LIM,BOTTOM}$ foldback to 40%		33.3		%V_{REF}
Output Under Voltage Threshold 2	$V_{UVP,2}$	V_{FB} falling, $I_{LIM,BOTTOM}$ foldback to 15%		50		mV
Min ON Time	$t_{ON,MIN}$	V_{IN}=$V_{IN,MAX}$		50		ns
Min Off Time	$t_{OFF,MIN}$			150		ns
Switching Frequency	f_{SW}			1.0		MHz
Soft-start Time	t_{SS}			1.4		ms
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a four-layer Silergy Evaluation Board.

Note3: LX spike voltage is tested by oscilloscope with bandwidth limited within 100MHz~250MHz. The test loop should be minimized.

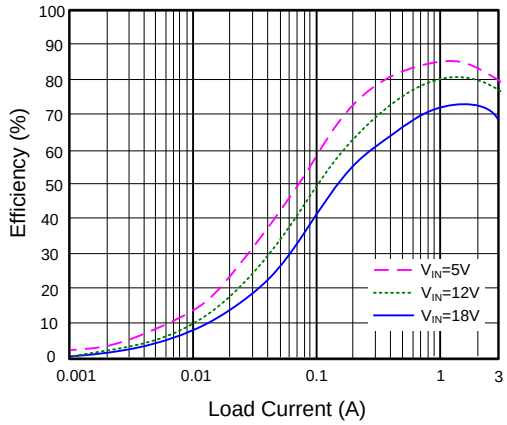
Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: The values are guaranteed by design.

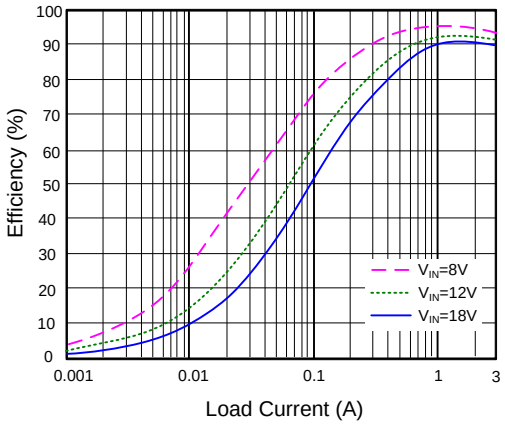
Note 6: The minimum on/off time should be considered for the given V_{IN}/V_{OUT} range in the real application.

Typical Performance Characteristics

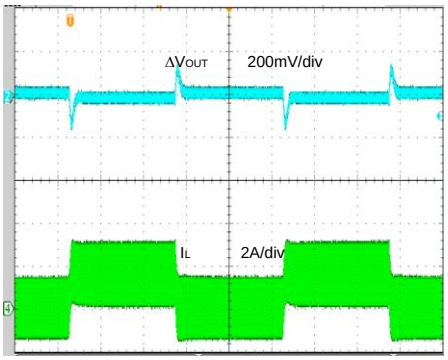
Efficiency vs. Load Current
(V_{OUT}=1.2V)



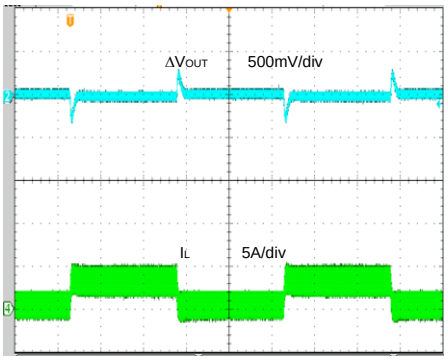
Efficiency vs. Load Current
(V_{OUT}=5V)



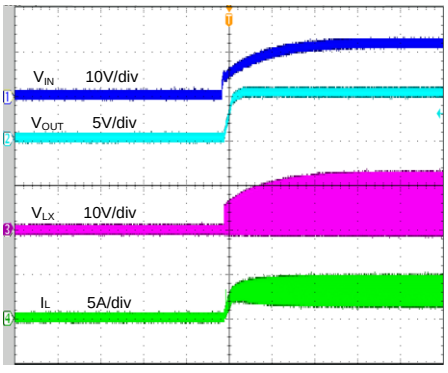
Load Transient
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0~1.5A)



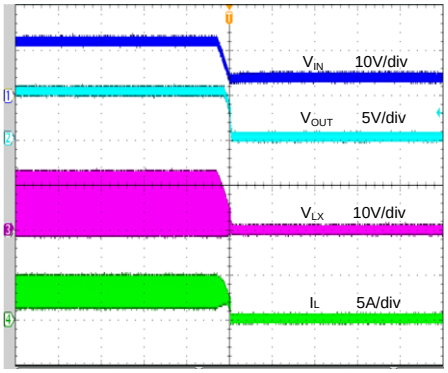
Load Transient
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.3~3A)



Startup from V_{IN}
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)

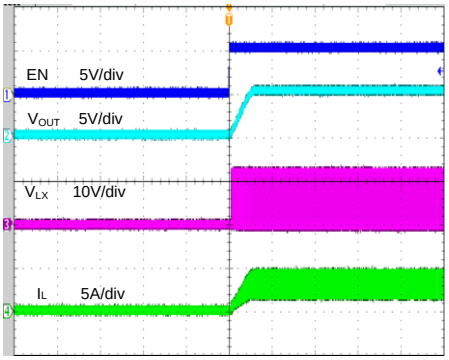


Shutdown from V_{IN}
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Startup from EN

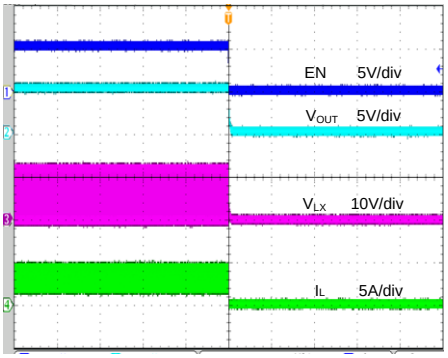
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from EN

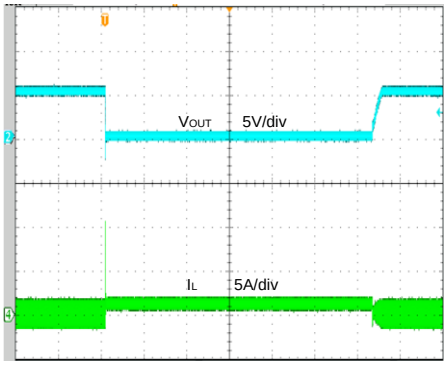
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (2ms/div)

Output Short Circuit

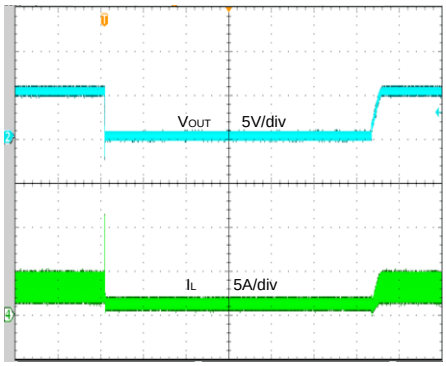
(V_{IN}=12V,V_{OUT}=5V, I_{OUT}=0A to short)



Time (4ms/div)

Output Short Circuit

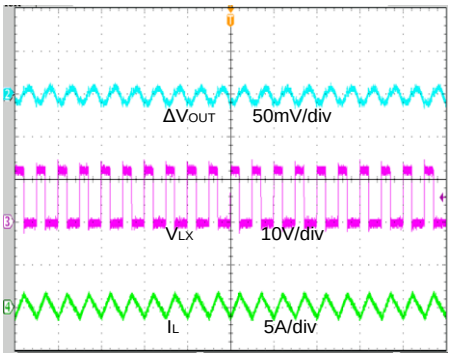
(V_{IN}=12V,V_{OUT}=5V, I_{OUT}=3A to short)



Time (4ms/div)

Output Ripple

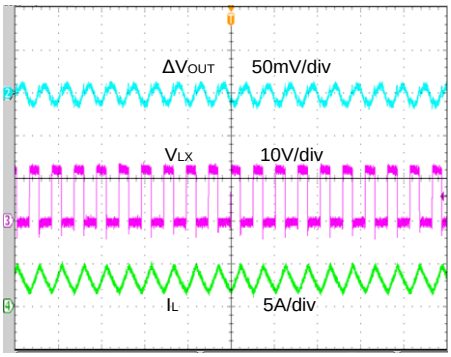
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



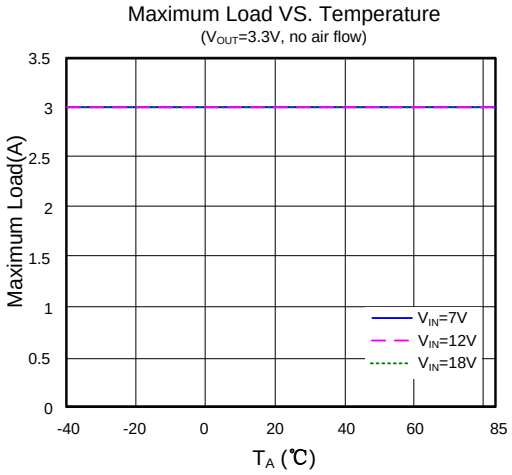
Time (2μs/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (2μs/div)



Operation

SY98103A is a high efficiency, 1MHz synchronous step-down DC/DC converter capable of delivering 3A current. The SY98103A operates over a wide input voltage range from 4.5V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY98103A features enable control. The device also provides cycle-by-cycle current limit, short circuit protection and thermal shutdown protection for reliable operation.

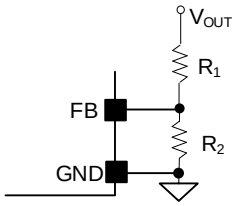
Applications Information

Because of the high integration in the SY98103A IC, the application circuit based on this regulator is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT} and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{SET} is 5V, R_1=100kΩ is chosen, then using following equation, R_2 can be calculated to be 13.7kΩ:

$$R_2 = \frac{0.6V}{V_{SET} - 0.6V} R_1 .$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)} .$$

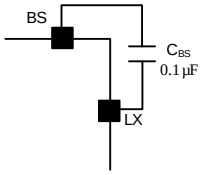
To minimize the potential noise problem, we place a typical X5R or a better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 4.7μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or a better grade ceramic capacitor greater than 22μF capacitance.

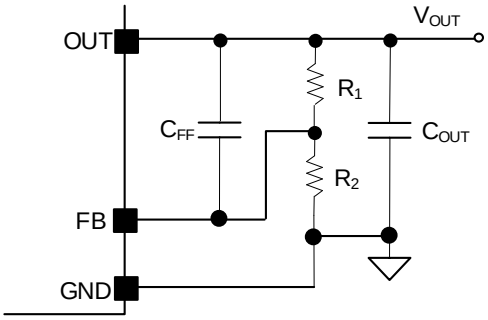
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A 0.1μF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations

The SY98103A integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor in parallel with R_1 may further speed up the load transient responses and it is recommended for applications with large load transient step requirements.



Layout Design

The layout design of SY98103A regulator is relatively simple. For the best efficiency and to minimize noise problem, we should place the following components close to the IC: C_{IN}, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board

space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2, and the trace connected to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

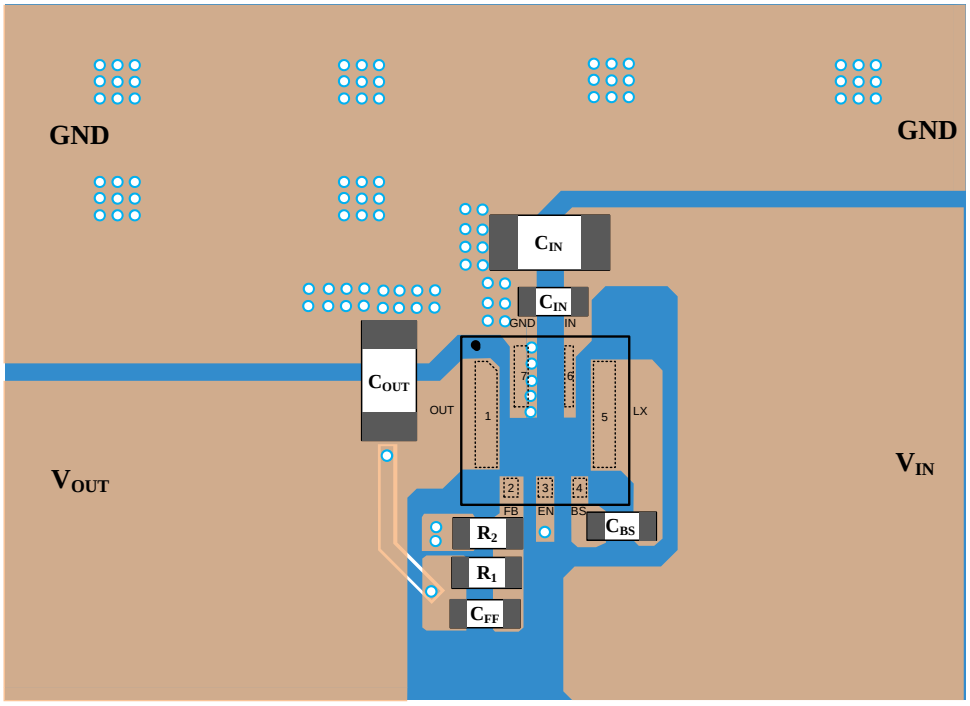
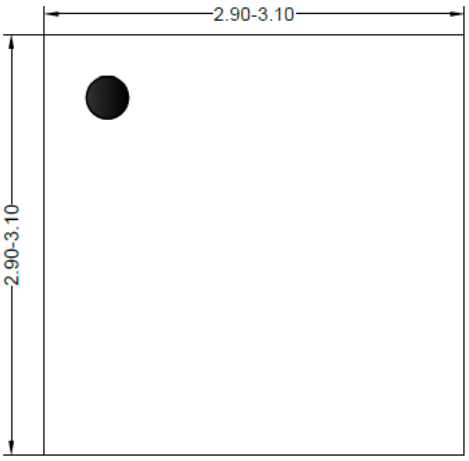
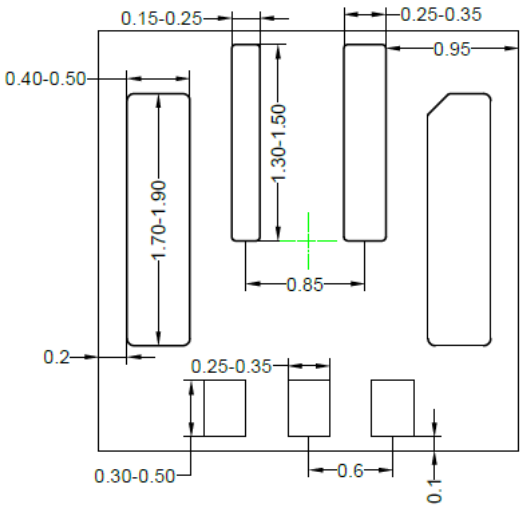


Figure4. PCB Layout Suggestion

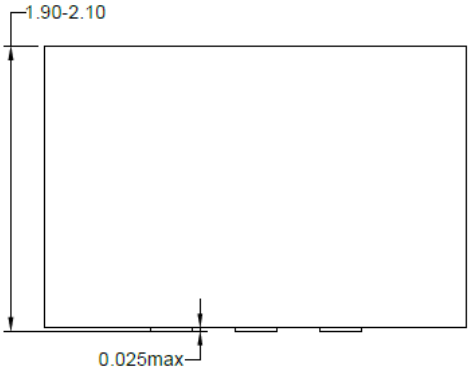
QFN3×3-7 Package Outline & PCB Layout



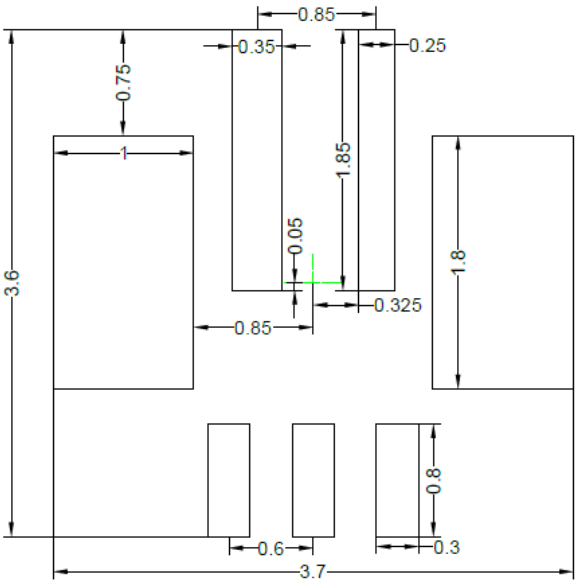
Top View



Bottom View



Front View



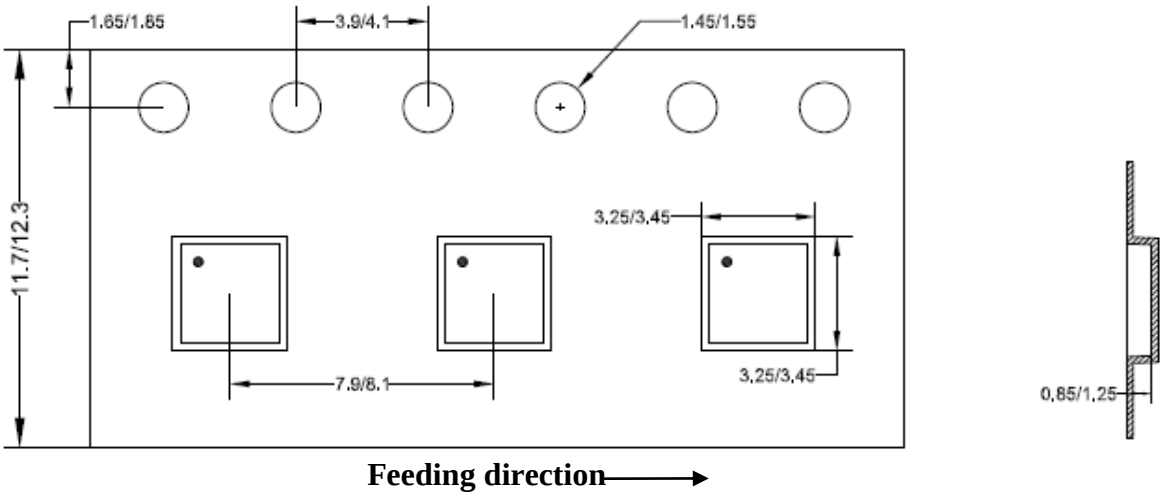
PCB Layout (Recommended)

Notes: 1，All dimension in millimeter and exclude mold flash & metal burr.
2，The center of PCB diagram refers to chip center.

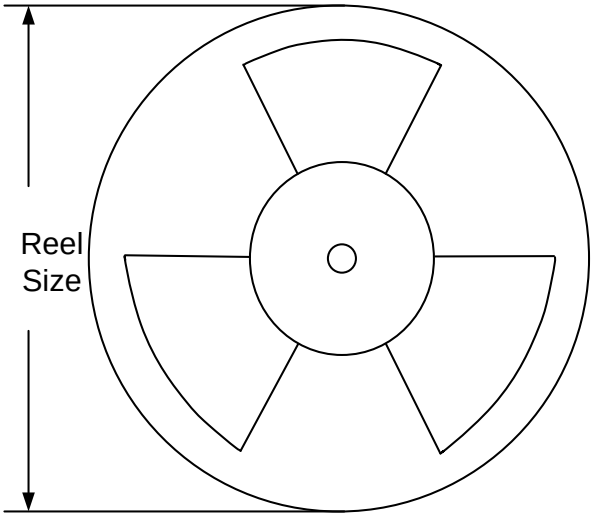
Taping & Reel Specification

1. Taping orientation

QFN3×3



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.,04, 2019	Revision 0.9B	Add output voltage range in the EC table. Add note 6 for output voltage range.
Oct.31, 2019	Revision 0.9A	Update in Taping & Reel Specification: Change the Qty per reel from 5000 to 3000
Dec 17, 2018	Revision 0.9	Initial Release

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