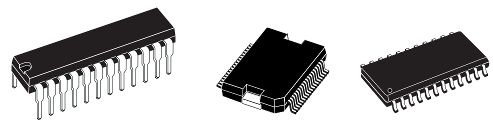
L6228

DMOS DRIVER FOR BIPOLAR STEPPER MOTOR

- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 2.8A OUTPUT PEAK CURRENT (1.4A RMS)
- $R_{DS(ON)}$ 0.73Ω TYP. VALUE @ T_j = 25°C
- OPERATING FREQUENCY UP TO 100KHz
- NON DISSIPATIVE OVERCURRENT PROTECTION
- DUAL INDEPENDENT CONSTANT t_{OFF} PWM CURRENT CONTROLLERS
- FAST/SLOW DECAY MODE SELECTION
- FAST DECAY QUASI-SYNCHRONOUS RECTIFICATION
- DECODING LOGIC FOR STEPPER MOTOR FULL AND HALF STEP DRIVE
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- UNDER VOLTAGE LOCKOUT
- INTEGRATED FAST FREE WHEELING DIODES



PowerDIP24 (20+2+2) **PowerSO36** **SO24 (20+2+2)**

ORDERING NUMBERS:
L6228N (PowerDIP24)
L6228PD (PowerSO36)
L6228D (SO24)

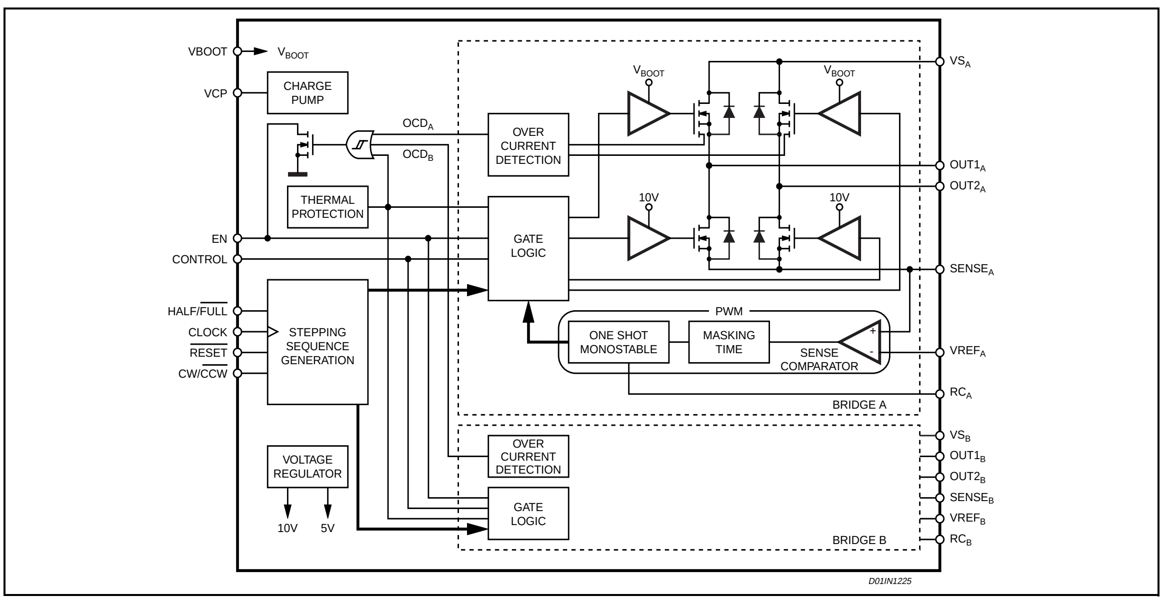
TYPICAL APPLICATIONS

- BIPOLAR STEPPER MOTOR

DESCRIPTION

The L6228 is a DMOS Fully Integrated Stepper Motor Driver with non-dissipative Overcurrent Protection, realized in MultiPower-BCD technology, which combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip. The device includes all the circuitry needed to drive a two-phase bipolar stepper motor including: a dual DMOS Full Bridge, the constant off time PWM Current Controller that performs the chopping regulation and the Phase Sequence Generator, that generates the stepping sequence. Available in PowerDIP24 (20+2+2), PowerSO36 and SO24 (20+2+2) packages, the L6228 features a non-dissipative overcurrent protection on the high side Power MOSFETs and thermal shutdown.

BLOCK DIAGRAM



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential Voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60V$; $V_{SENSEA} = V_{SENSEB} = GND$	60	V
V_{BOOT}	Bootstrap Peak Voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{REFA}, V_{REFB}	Voltage Range at pins V_{REFA} and V_{REFB}		-0.3 to +7	V
V_{RCA}, V_{RCB}	Voltage Range at pins RC_A and RC_B		-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$		-1 to +4	V
$I_{S(peak)}$	Pulsed Supply Current (for each V_S pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1ms$	3.55	A
I_S	RMS Supply Current (for each V_S pin)	$V_{SA} = V_{SB} = V_S$	1.4	A
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

RECOMMENDED OPERATING CONDITIONS

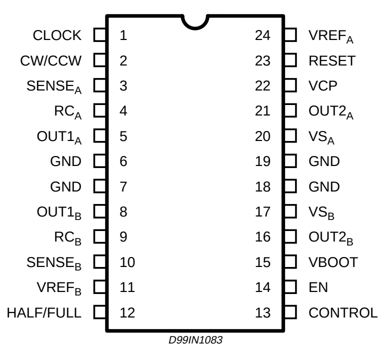
Symbol	Parameter	Test Conditions	MIN	MAX	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential Voltage Between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{REFA}, V_{REFB}	Voltage Range at pins V_{REFA} and V_{REFB}		-0.1	5	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	RMS Output Current			1.4	A
T_j	Operating Junction Temperature		-25	+125	°C
f_{sw}	Switching Frequency			100	KHz

THERMAL DATA

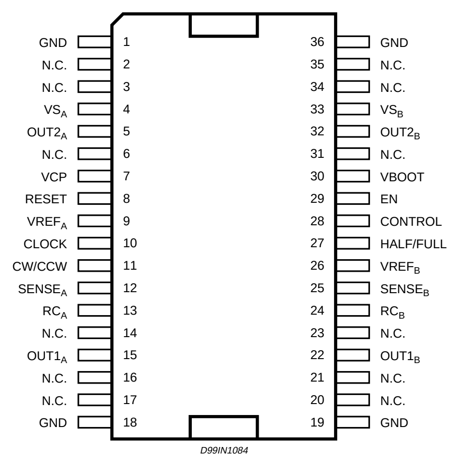
Symbol	Description	PowerDIP24	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	Maximum Thermal Resistance Junction-Pins	19	15	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	2	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient (1)	44	55	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient (2)	-	-	36	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient (3)	-	-	16	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient (4)	59	78	63	°C/W

(1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6cm^2 (with a thickness of 35µm).
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm^2 (with a thickness of 35µm).
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm^2 (with a thickness of 35µm), 16 via holes and a ground layer.
(4) Mounted on a multi-layer FR4 PCB without any heat sinking surface on the board.

PIN CONNECTIONS (Top View)



PowerDIP24/SO24



PowerSO36 (5)

(5) The slug is internally connected to pins 1,18,19 and 36 (GND pins).

PIN DESCRIPTION

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
1	10	CLOCK	Logic Input	Step Clock input. The state machine makes one step on each rising edge.
2	11	CW/CCW	Logic Input	Selects the direction of the rotation. HIGH logic level sets clockwise direction, whereas LOW logic level sets counterclockwise direction. If not used, it has to be connected to GND or +5V.
3	12	$SENSE_A$	Power Supply	Bridge A Source Pin. This pin must be connected to Power Ground through a sensing power resistor.
4	13	RC_A	RC Pin	RC Network Pin. A parallel RC network connected between this pin and ground sets the Current Controller OFF-Time of the Bridge A.
5	15	$OUT1_A$	Power Output	Bridge A Output 1.
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Ground terminals. In PowerDIP24 and SO24 packages, these pins are also used for heat dissipation toward the PCB. On PowerSO36 package the slug is connected to these pins.
8	22	$OUT1_B$	Power Output	Bridge B Output 1.
9	24	RC_B	RC Pin	RC Network Pin. A parallel RC network connected between this pin and ground sets the Current Controller OFF-Time of the Bridge B.
10	25	$SENSE_B$	Power Supply	Bridge B Source Pin. This pin must be connected to Power Ground through a sensing power resistor.
11	26	$VREF_B$	Analog Input	Bridge B Current Controller Reference Voltage. Do not leave this pin open or connected to GND.
12	27	HALF/FULL	Logic Input	Step Mode Selector. HIGH logic level sets HALF STEP Mode, LOW logic level sets FULL STEP Mode. If not used, it has to be connected to GND or +5V.
13	28	CONTROL	Logic Input	Decay Mode Selector. HIGH logic level sets SLOW DECAY Mode. LOW logic level sets FAST DECAY Mode. If not used, it has to be connected to GND or +5V.
14	29	EN	Logic Input (6)	Chip Enable. LOW logic level switches OFF all Power MOSFETs of both Bridge A and Bridge B. This pin is also connected to the collector of the Overcurrent and Thermal Protection to implement over current protection. If not used, it has to be connected to +5V through a resistor.
15	30	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper Power MOSFETs of both Bridge A and Bridge B.
16	32	$OUT2_B$	Power Output	Bridge B Output 2.
17	33	VS_B	Power Supply	Bridge B Power Supply Voltage. It must be connected to the Supply Voltage together with pin VS_A
20	4	VS_A	Power Supply	Bridge A Power Supply Voltage. It must be connected to the Supply Voltage together with pin VS_B

PIN DESCRIPTION (continued)

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
21	5	$OUT2_A$	Power Output	Bridge A Output 2.
22	7	VCP	Output	Charge Pump Oscillator Output.
23	8	RESET	Logic Input	Reset Pin. LOW logic level restores the *Home* State (State 1) on the Phase Sequence Generator State Machine. If not used, it has to be connected to +5V.
24	9	$VREF_A$	Analog Input	Bridge A Current Controller Reference Voltage. Do not leave this pin open or connected to GND.

(6) Also connected at the output drain of the Over current and Thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 2.2KΩ - 180KΩ, recommended 100KΩ.

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{Sth(ON)}$	Turn-on Threshold		5.8	6.3	6.8	V
$V_{Sth(OFF)}$	Turn-off Threshold		5	5.5	6	V
I_S	Quiescent Supply Current	All Bridges OFF; T_j = -25°C to 125°C (7)		5	10	mA
$T_{j(OFF)}$	Thermal Shutdown Temperature			165		°C
Output DMOS Transistors						
$R_{DS(ON)}$	High-Side + Low-Side Switch ON Resistance	T_j = 25 °C		1.47	1.69	Ω
		T_j =125 °C (7)		2.35	2.70	Ω
I_{DSS}	Leakage Current	EN = Low; OUT = V_S			2	mA
		EN = Low; OUT = GND	-0.3			mA
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 1.4A, EN = LOW		1.15	1.3	V
t_{rr}	Reverse Recovery Time	I_f = 1.4A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Logic Inputs (EN, CONTROL, HALF/FULL, CLOCK, RESET, CW/CCW)						
V_{IL}	Low level logic input voltage		-0.3		0.8	V
V_{IH}	High level logic input voltage		2		7	V
I_{IL}	Low Level Logic Input Current	GND Logic Input Voltage	-10			µA
I_{IH}	High Level Logic Input Current	7V Logic Input Voltage			10	µA

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{th(ON)}$	Turn-on Input Threshold			1.8	2.0	V
$V_{th(OFF)}$	Turn-off Input Threshold		0.8	1.3		V
$V_{th(HYS)}$	Input Threshold Hysteresis		0.25	0.5		V
Switching Characteristics						
$t_{D(ON)EN}$	Enable to Output Turn-on Delay Time (8)	I_{LOAD} =1.4A, Resistive Load	500	650	800	ns
$t_{D(OFF)EN}$	Enable to Output Turn-off Delay Time (8)	I_{LOAD} =1.4A, Resistive Load	500	800	1000	ns
t_{RISE}	Output Rise Time (8)	I_{LOAD} =1.4A, Resistive Load	40		250	ns
t_{FALL}	Output Fall Time (8)	I_{LOAD} =1.4A, Resistive Load	40		250	ns
t_{DCLK}	Clock to Output Delay Time (9)	I_{LOAD} =1.4A, Resistive Load		2		µs
$t_{CLK(min)L}$	Minimum Clock Time (10)				1	µs
$t_{CLK(min)H}$	Minimum Clock Time (10)				1	µs
f_{CLK}	Clock Frequency				100	KHz
$t_{S(MIN)}$	Minimum Set-up Time (11)				1	µs
$t_{H(MIN)}$	Minimum Hold Time (11)				1	µs
$t_{R(MIN)}$	Minimum Reset Time (11)				1	µs
$t_{RCLK(MIN)}$	Minimum Reset to Clock Delay Time (11)				1	µs
t_{DT}	Dead Time Protection		0.5	1		µs
f_{CP}	Charge Pump Frequency	T_j = -25°C to 125°C (7)		0.6	1	MHz
PWM Comparator and Monostable						
I_{RCA}, I_{RCB}	Source Current at pins RC_A and RC_B	$V_{RCA} = V_{RCB}$ = 2.5V	3.5	5.5		mA
V_{offset}	Offset Voltage on Sense Comparator	V_{REFA}, V_{REFB} = 0.5V		±5		mV
t_{PROP}	Turn OFF Propagation Delay (12)			500		ns
t_{BLANK}	Internal Blanking Time on SENSE pins			1		µs
$t_{ON(MIN)}$	Minimum On Time			2.5	3	µs
t_{OFF}	PWM Recirculation Time	R_{OFF} = 20KΩ; C_{OFF} = 1nF		13		µs
		R_{OFF} = 100KΩ; C_{OFF} = 1nF		61		µs

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{BIAS}	Input Bias Current at pins $VREF_A$ and $VREF_B$				10	µA
Over Current Protection						
I_{SOVER}	Input Supply Overcurrent Protection Threshold	T_j = -25°C to 125°C (7)	2	2.8	3.55	A
R_{OPDR}	Open Drain ON Resistance	I = 4mA		40	60	Ω
$t_{OCD(ON)}$	OCD Turn-on Delay Time (13)	I = 4mA; C_{EN} < 100pF		200		ns
$t_{OCD(OFF)}$	OCD Turn-off Delay Time (13)	I = 4mA; C_{EN} < 100pF		100		ns

(7) Tested at 25°C in a restricted range and guaranteed by characterization.
(8) See Fig. 1.
(9) See Fig. 2.
(10) See Fig. 3.
(11) See Fig. 4.
(12) Measured applying a voltage of 1V to pin SENSE and a voltage drop from 2V to 0V to pin VREF.
(13) See Fig. 5.

Figure 1. Switching Characteristic Definition

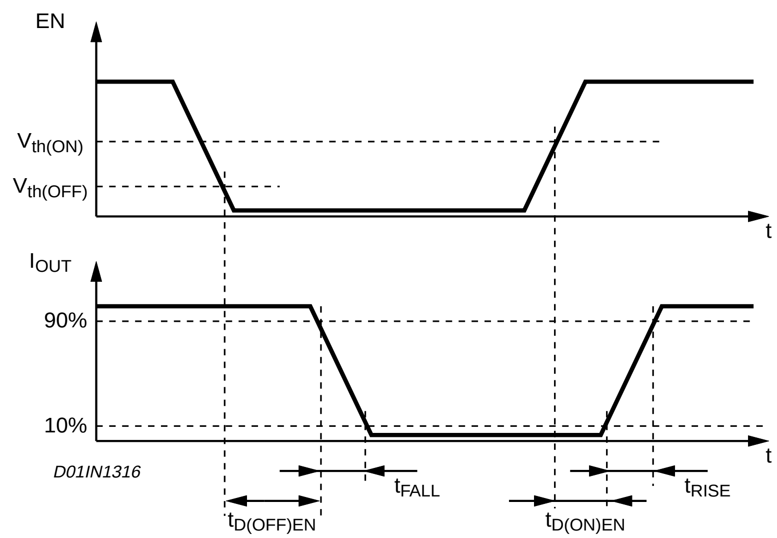


Figure 2. Clock to Output Delay Time

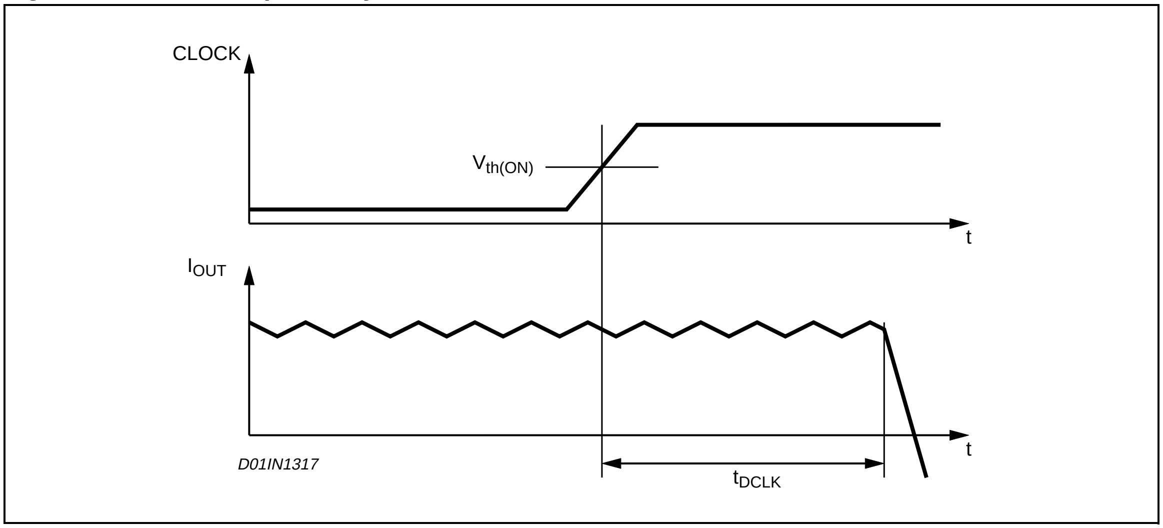


Figure 3. Minimum Timing Definition; Clock Input

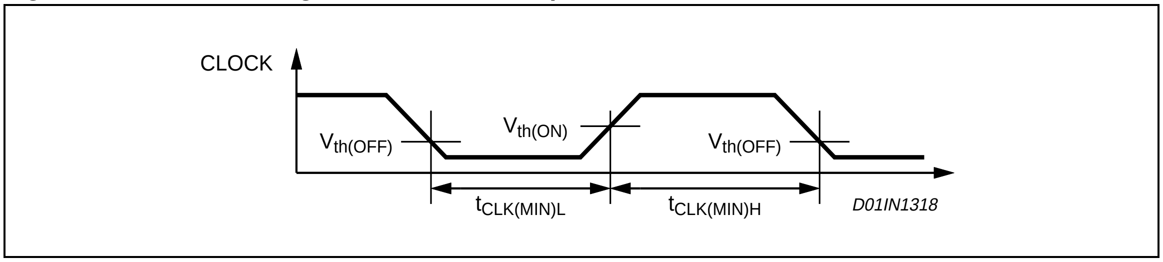


Figure 4. Minimum Timing Definition; Logic Inputs

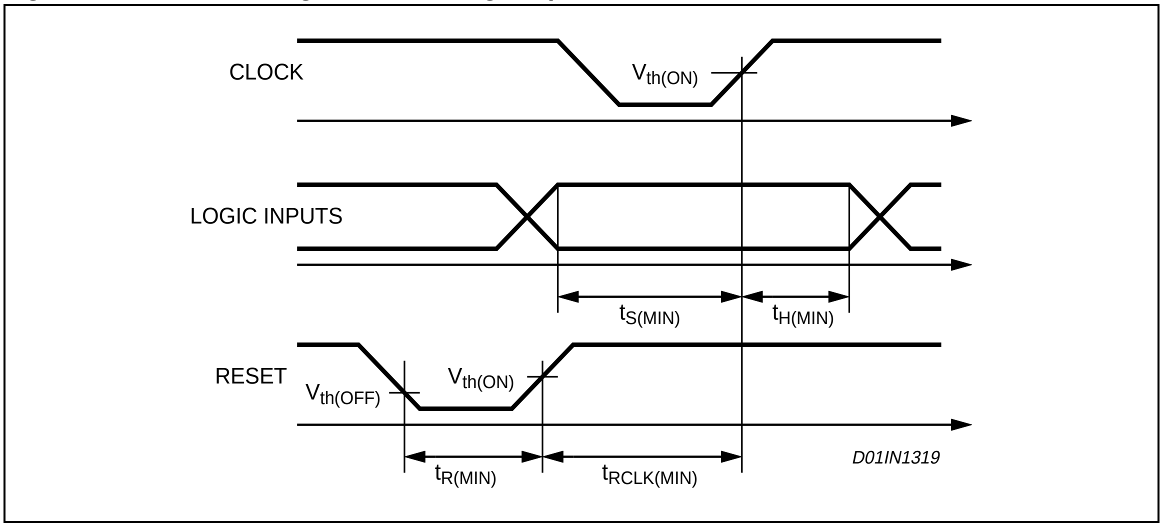
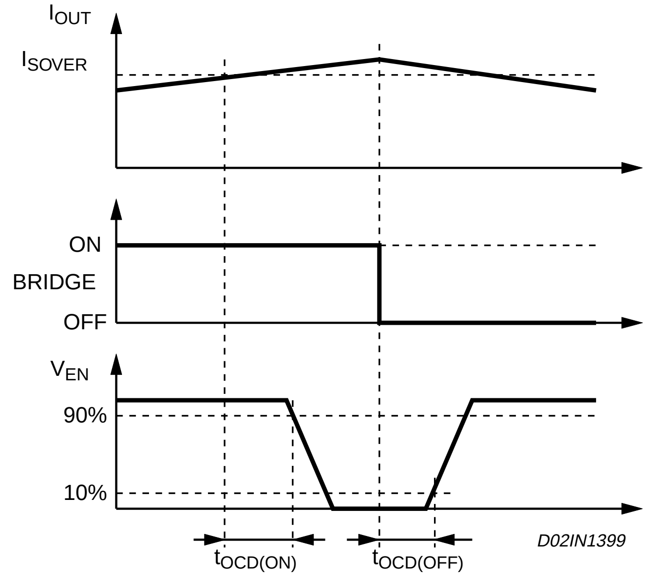


Figure 5. Overcurrent Detection Timing Definition



CIRCUIT DESCRIPTION

POWER STAGES and CHARGE PUMP

The L6228 integrates two independent Power MOS Full Bridges. Each Power MOS has an $R_{DS(ON)}$ = 0.73Ω (typical value @ 25°C), with intrinsic fast freewheeling diode. Switching patterns are generated by the PWM Current Controller and the Phase Sequence Generator (see below). Cross conduction protection is achieved using a dead time (t_{DT} = 1µs typical value) between the switch off and switch on of two Power MOSFETSs in one leg of a bridge.

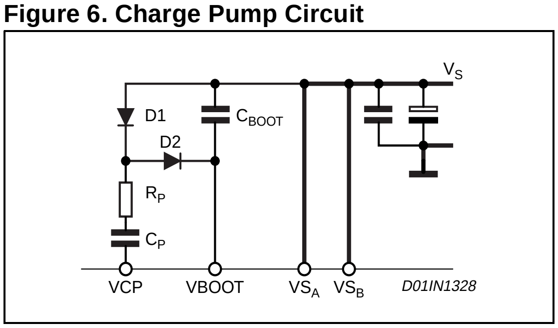
Pins VS_A and VS_B MUST be connected together to the supply voltage V_S. The device operates with a supply voltage in the range from 8V to 52V. It has to be noticed that the $R_{DS(ON)}$ increases of some percents when the supply voltage is in the range from 8V to 12V.

Using N-Channel Power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped supply voltage V_{BOOT} is obtained through an internal Oscillator and few external components to realize a charge pump circuit as shown in Figure 6. The oscillator output (VCP) is a square wave at 600KHz (typical) with 10V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table 1.

Table 1. Charge Pump External Components Values

C_{BOOT}	220nF
C_P	10nF
R_P	100Ω
D1	1N4148
D2	1N4148

Figure 6. Charge Pump Circuit



LOGIC INPUTS

Pins CONTROL, HALF/FULL, CLOCK, RESET and CW/CCW are TTL/CMOS and uC compatible logic inputs. The internal structure is shown in Fig. 7. Typical value for turn-on and turn-off thresholds are respectively $V_{th(ON)}$= 1.8V and $V_{th(OFF)}$= 1.3V.

Pin EN (Enable) has identical input structure with the exception that the drain of the Overcurrent and thermal protection MOSFET is also connected to this pin. Due to this connection some care needs to be taken in driving this pin. The EN input may be driven in one of two configurations as shown in Fig. 8 or 9. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in Fig. 8. If the driver is a standard Push-Pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in Fig. 9. The resistor R_{EN} should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF. More information on selecting the values is found in the Overcurrent Protection section.

Figure 7. Logic Inputs Internal Structure

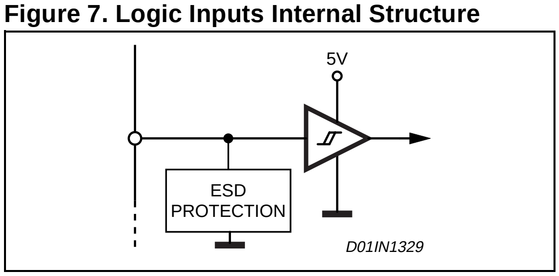


Figure 8. EN Pin Open Collector Driving

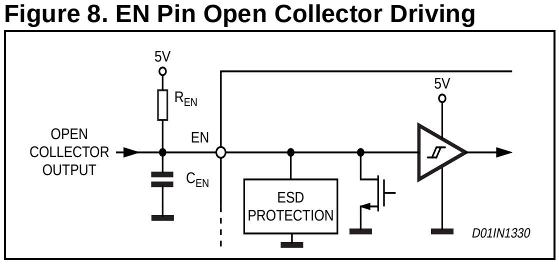
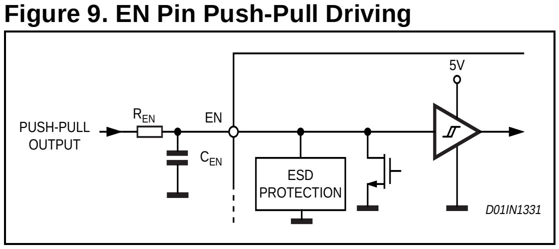


Figure 9. EN Pin Push-Pull Driving



PWM CURRENT CONTROL

The L6228 includes a constant off time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOS transistors and ground, as shown in Figure 10. As the current in the motor builds up the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$) the sense comparator triggers the monostable switching the bridge off. The power MOS remain off for the time set by the monostable and the motor current recirculates as defined by the selected decay mode, described in the next section. When the monostable times out the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time is the sum of the monostable time plus the dead time.

Figure 10. PWM Current Controller Simplified Schematic

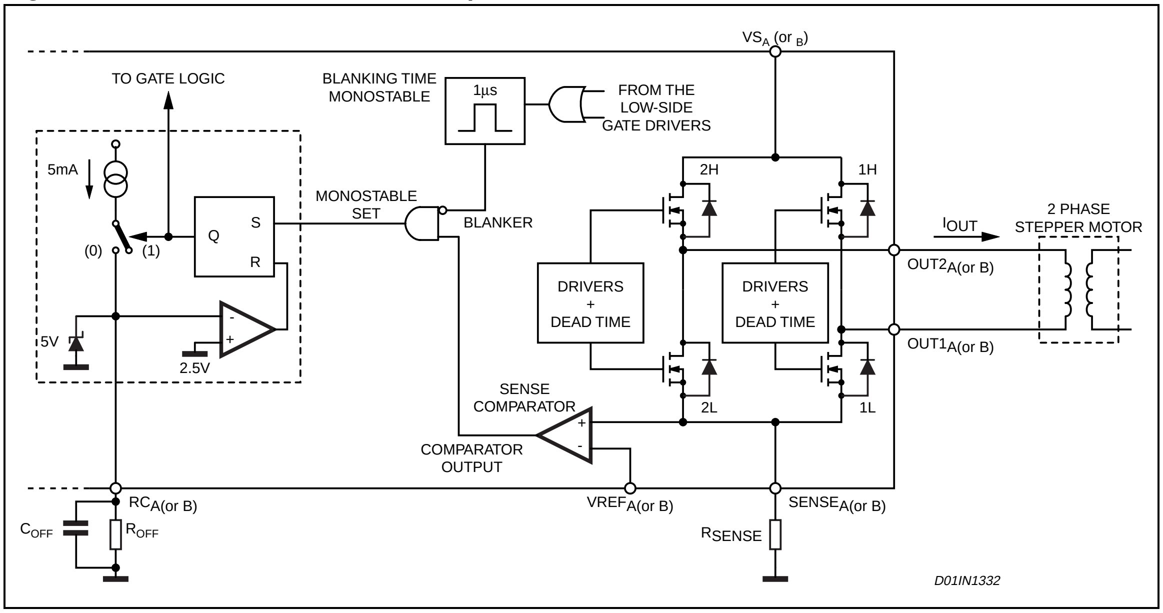


Figure 11 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. More details regarding the Synchronous Rectification and the output stage configuration are included in the next section.

Immediately after the Power MOS turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6228 provides a 1µs Blanking Time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 11. Output Current Regulation Waveforms

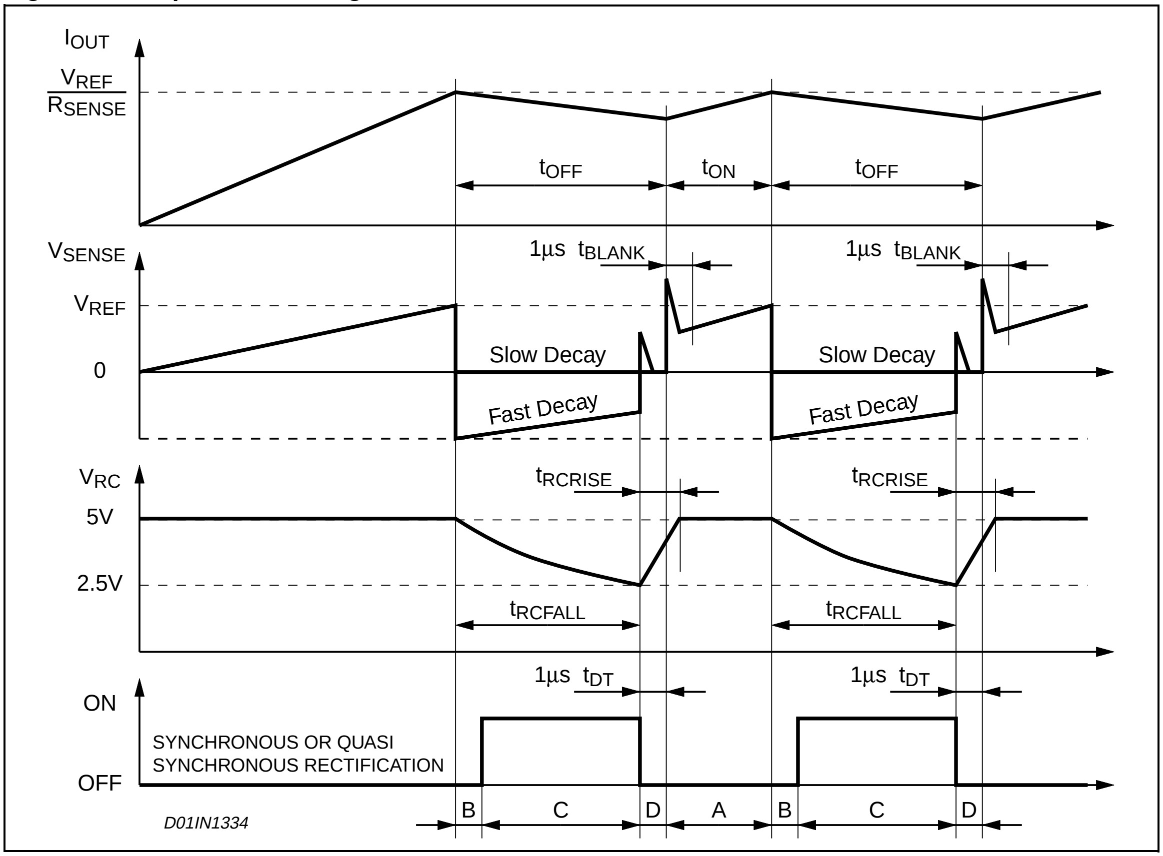


Figure 12 shows the magnitude of the Off Time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$$

$$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$20K\Omega \le R_{OFF} \le 100K\Omega$

$0.47nF \le C_{OFF} \le 100nF$

$t_{DT} = 1\mu s$ (typical value)

Therefore:

$t_{OFF(MIN)} = 6.6\mu s$

$t_{OFF(MAX)} = 6ms$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the Rise Time t_{RCRISE} of the voltage at the pin RCOFF. The Rise Time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON}, which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 2.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 13 shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the off time t_{OFF} is not more constant.
So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 12. t_{OFF} versus C_{OFF} and R_{OFF}

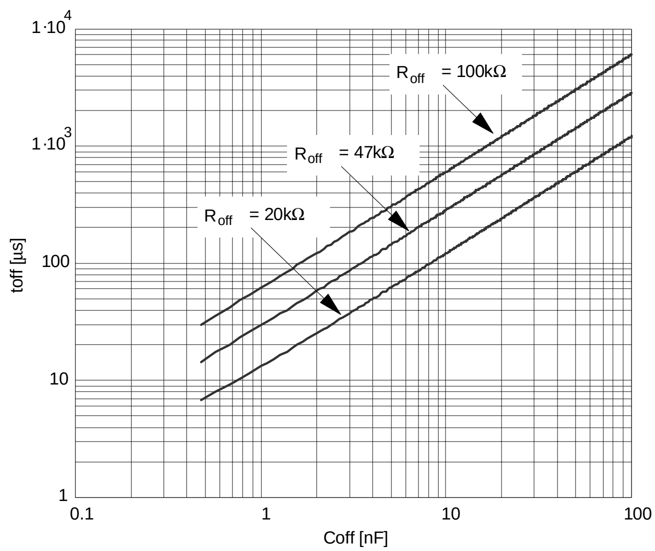
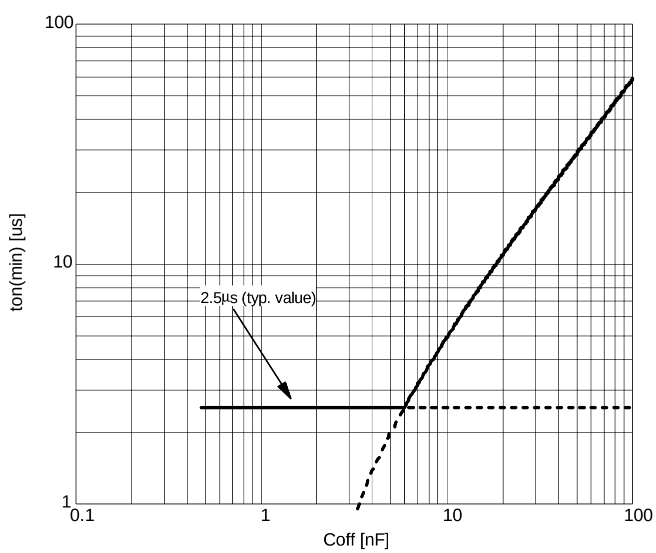


Figure 13. Area where t_{ON} can vary maintaining the PWM regulation.



DECAY MODES

The CONTROL input is used to select the behavior of the bridge during the off time. When the CONTROL pin is low, the Fast Decay mode is selected and both transistors in the bridge are switched off during the off time. When the CONTROL pin is high, the Slow Decay mode is selected and only the low side transistor of the bridge is switched off during the off time.

Figure 14 shows the operation of the bridge in the Fast Decay mode. At the start of the off time, both of the power MOS are switched off and the current recirculates through the two opposite free wheeling diodes. The current decays with a high di/dt since the voltage across the coil is essentially the power supply voltage. After the dead time, the lower power MOS in parallel with the conducting diode is turned on in synchronous rectification mode. In applications where the motor current is low it is possible that the current can decay completely to zero during the off time. At this point if both of the power MOS were operating in the synchronous rectification mode it would then be possible for the current to build in the opposite direction. To prevent this only the lower power MOS is operated in synchronous rectification mode. This operation is called Quasi-Synchronous Rectification Mode. When the monostable times out, the power MOS are turned on again after some delay set by the dead time to prevent cross conduction.

Figure 15 shows the operation of the bridge in the Slow Decay mode. At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the dead time the upper power MOS is operated in the synchronous rectification mode. When the monostable times out, the lower power MOS is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 14. Fast Decay Mode Output Stage Configurations

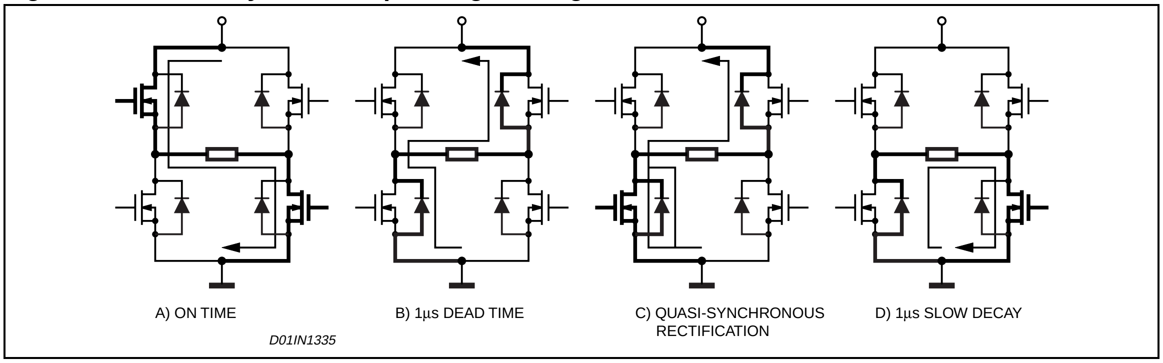
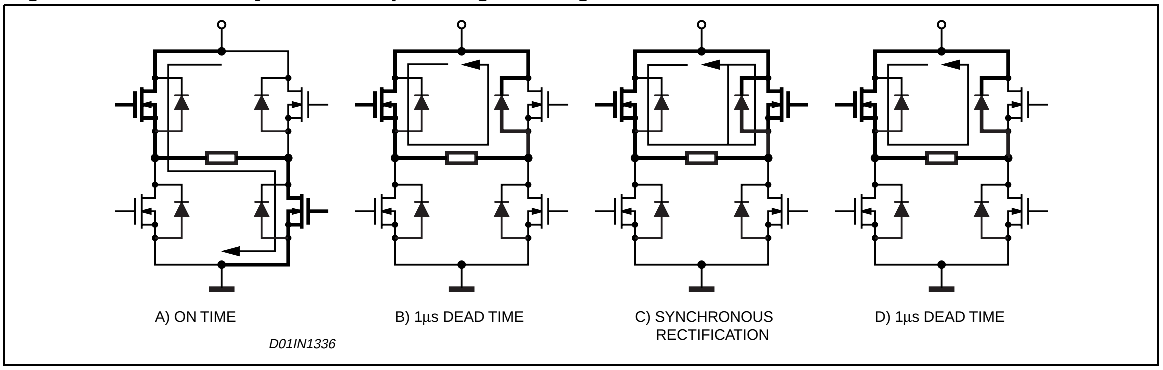


Figure 15. Slow Decay Mode Output Stage Configurations



STEPPING SEQUENCE GENERATION

The phase sequence generator is a state machine that provides the phase and enable inputs for the two bridges to drive a stepper motor in either full step or half step. Two full step modes are possible, the Normal Drive Mode where both phases are energized each step and the Wave Drive Mode where only one phase is energized at a time. The drive mode is selected by the HALF/FULL input and the current state of the sequence generator as described below. A rising edge of the CLOCK input advances the state machine to the next state. The direction of rotation is set by the CW/CCW input. The RESET input resets the state machine to state.

HALF STEP MODE

A HIGH logic level on the HALF/FULL input selects Half Step Mode. Figure 16 shows the motor current waveforms and the state diagram for the Phase Sequencer Generator. At Start-Up or after a RESET the Phase Sequencer is at state 1. After each clock pulse the state changes following the sequence 1,2,3,4,5,6,7,8,… if CW/CCW is high (Clockwise movement) or 1,8,7,6,5,4,3,2,… if CW/CCW is low (Counterclockwise movement).

NORMAL DRIVE MODE (Full-step two-phase-on)

A LOW level on the HALF/FULL input selects the Full Step mode. When the low level is applied when the state machine is at an ODD numbered state the Normal Drive Mode is selected. Figure Fig. 17 shows the motor current waveform state diagram for the state machine of the Phase Sequencer Generator. The Normal Drive Mode can easily be selected by holding the HALF/FULL input low and applying a RESET. AT start -up or after a RESET the State Machine is in state1. While the HALF/FULL input is kept low, state changes following the sequence 1,3,5,7,… if CW/CCW is high (Clockwise movement) or 1,7,5,3,… if CW/CCW is low (Counterclockwise movement).

WAVE DRIVE MODE (Full-step one-phase-on)

A LOW level on the pin HALF/FULL input selects the Full Step mode. When the low level is applied when the state machine is at an EVEN numbered state the Wave Drive Mode is selected. Figure 18 shows the motor current waveform and the state diagram for the state machine of the Phase Sequence Generator. To enter the Wave Drive Mode the state machine must be in an EVEN numbered state. The most direct method to select the Wave Drive Mode is to first apply a RESET, then while keeping the HALF/FULL input high apply one pulse to the clock input then take the HALF/FULL input low. This sequence first forces the state machine to sate 1. The clock pulse, with the HALF/FULL input high advances the state machine from state 1 to either state 2 or 8 depending on the CW/CCW input. Starting from this point, after each clock pulse (rising edge) will advance the state machine following the sequence 2,4,6,8,… if CW/CCW is high (Clockwise movement) or 8,6,4,2,… if CW/CCW is low (Counterclockwise movement).

Figure 16. Half Step Mode

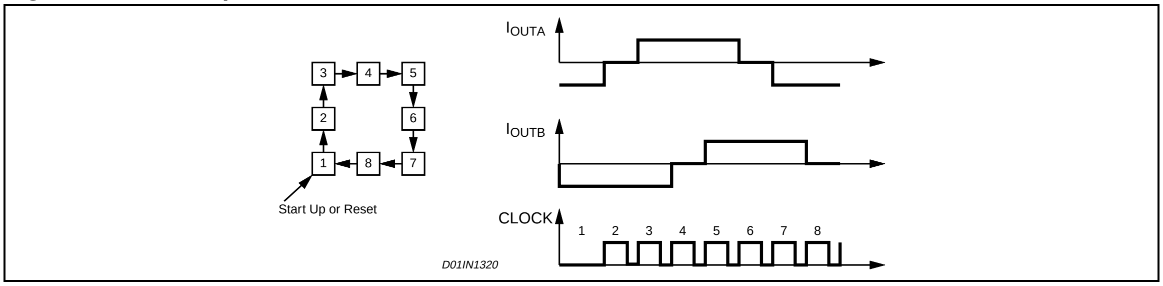


Figure 17. Normal Drive Mode

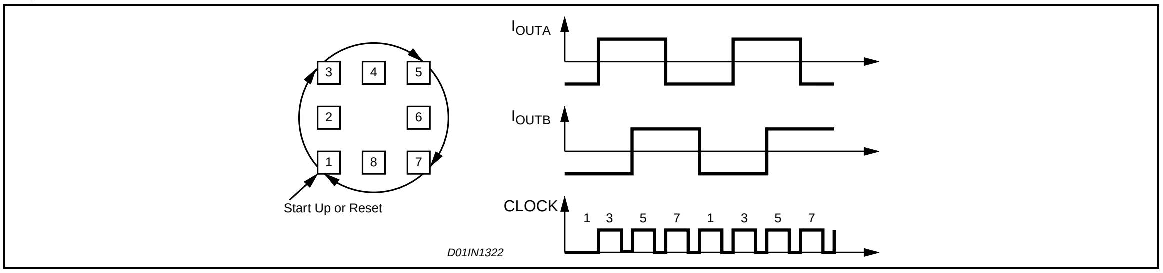
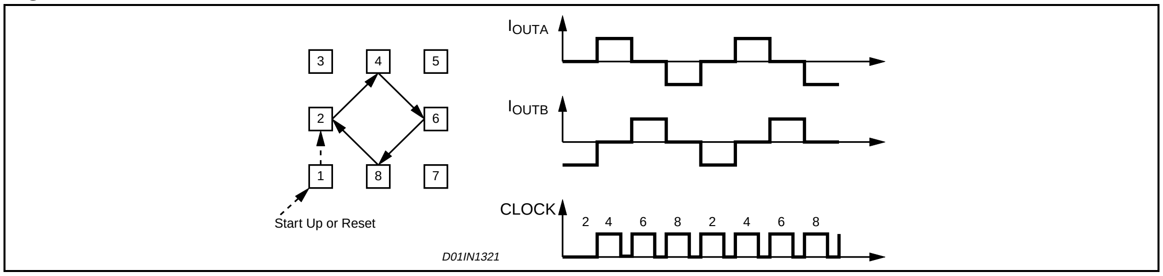


Figure 18. Wave Drive Mode



NON-DISSIPATIVE OVERCURRENT PROTECTION

The L6228 integrates an Overcurrent Detection Circuit (OCD) for full protection. This circuit provides protection against a short circuit to ground or between two phases of the bridge. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 19 shows a simplified schematic of the overcurrent detection circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically 2.8A) the OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3V typical) by an internal open drain MOS with a pull down capability of 4mA. By using an external R-C on the EN pin, the off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

Figure 19. Overcurrent Protection Simplified Schematic

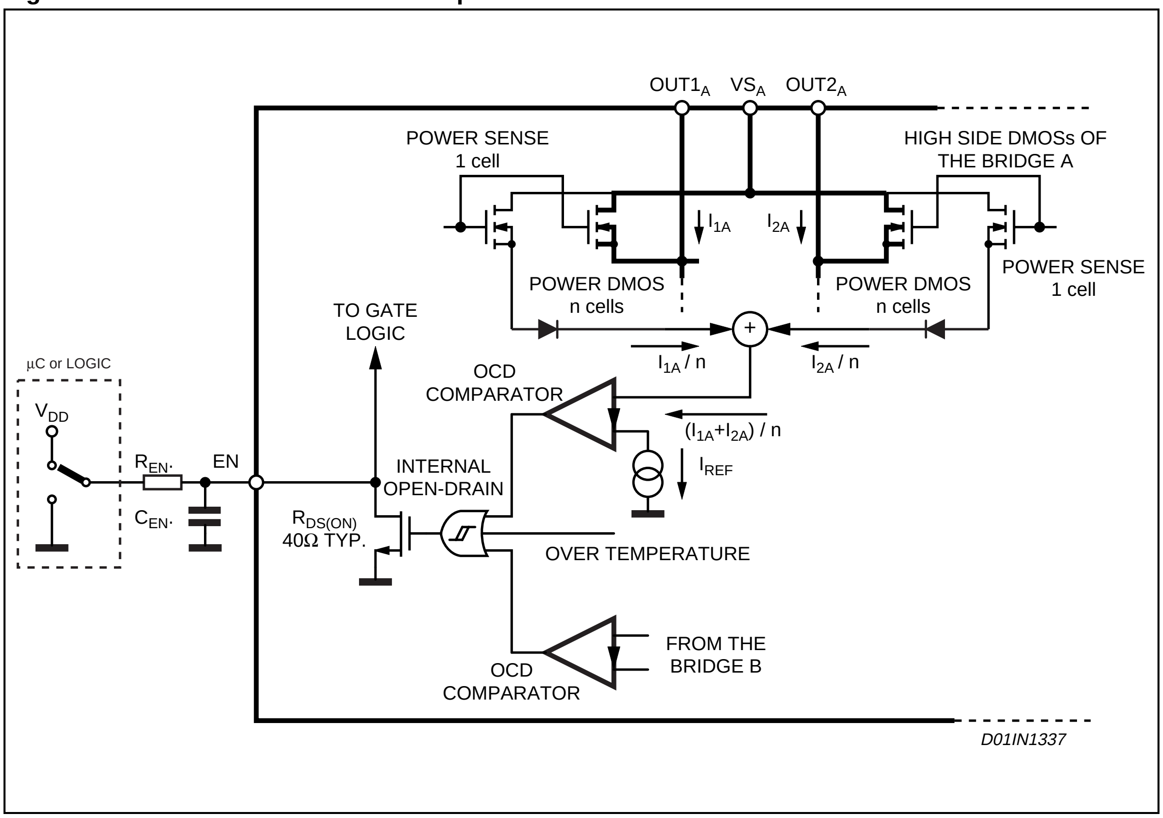


Figure 20 shows the Overcurrent Detection operation. The Disable Time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in Figure 21. The Delay Time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in Figure 22.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable Delay Time and the R_{EN} value should be chosen according to the desired Disable Time.

The resistor R_{EN} should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF that allow obtaining 200µs Disable Time.

Figure 20. Overcurrent Protection Waveforms

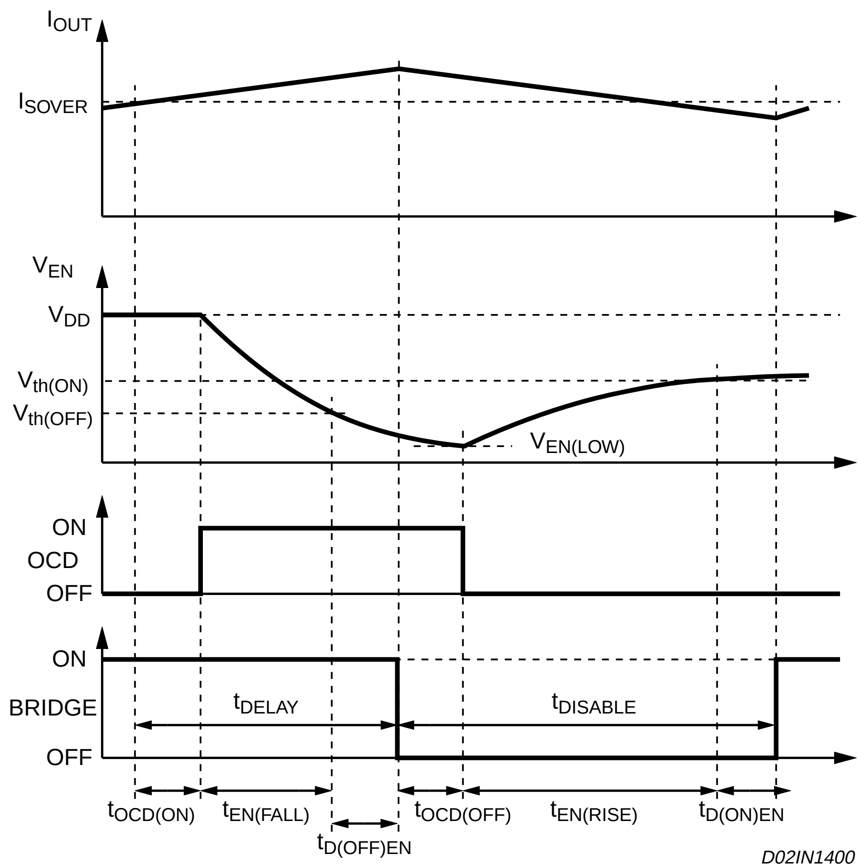


Figure 21. $t_{DISABLE}$ versus C_{EN} and R_{EN} (V_{DD} = 5V).

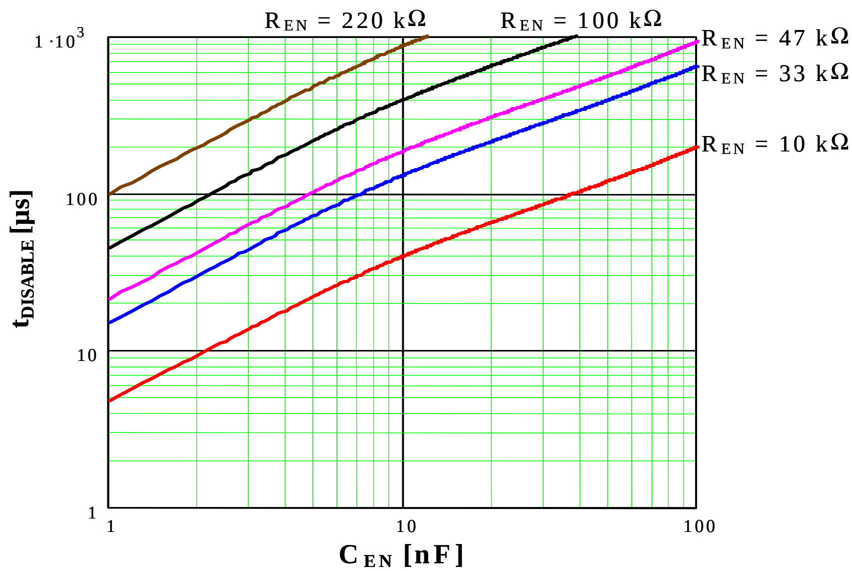
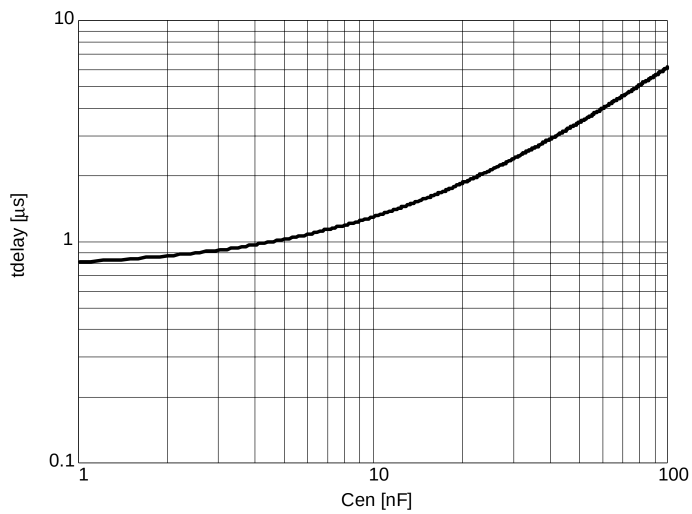


Figure 22. t_{DELAY} versus C_{EN} (V_{DD} = 5V).



THERMAL PROTECTION

In addition to the Overcurrent Protection, the L6228 integrates a Thermal Protection for preventing the device destruction in case of junction over temperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switch-off when the junction temperature reaches 165°C (typ. value) with 15°C hysteresis (typ. value).

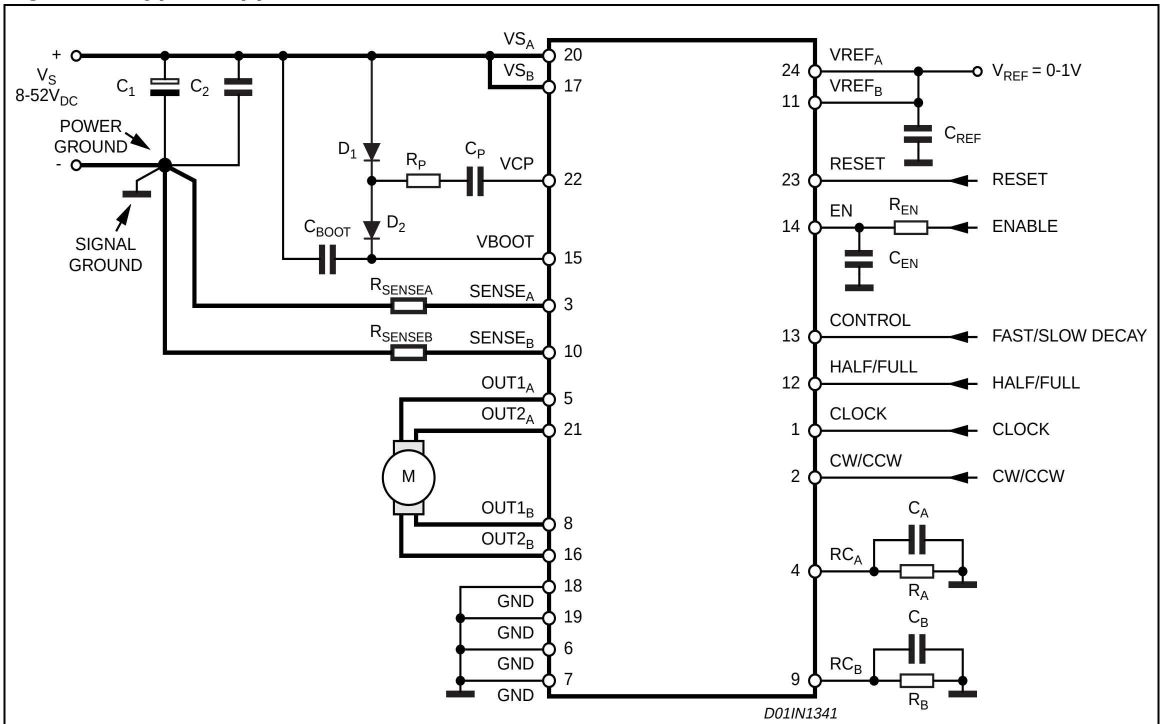
APPLICATION INFORMATION

A typical Bipolar Stepper Motor Driver application using L6228 is shown in Fig. 23. Typical component values for the application are shown in Table 2. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6228 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitor connected from the EN input to ground sets the shut down time when an over current is detected (see Overcurrent Protection). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistors with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins (except EN) are best connected to 5V (High Logic Level) or GND (Low Logic Level) (see pin description). It is recommended to keep Power Ground and Signal Ground separated on PCB.

Table 2. Component Values for Typical Application

C_1	100µF	D_1	1N4148
C_2	100nF	D_2	1N4148
C_A	1nF	R_A	39KΩ
C_B	1nF	R_B	39KΩ
C_{BOOT}	220nF	R_{EN}	100KΩ
C_P	10nF	R_P	100Ω
C_{EN}	5.6nF	R_{SENSEA}	0.6Ω
C_{REF}	68nF	R_{SENSEB}	0.6Ω

Figure 23. Typical Application



Output Current Capability and IC Power Dissipation

In Fig. 24, 25, 26 and 27 are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving a two-phase stepper motor, for different driving sequences:

– HALF STEP mode (Fig. 24) in which alternately one phase / two phases are energized.

– NORMAL DRIVE (FULL-STEP TWO PHASE ON) mode (Fig. 25) in which two phases are energized during each step.

– WAVE DRIVE (FULL-STEP ONE PHASE ON) mode (Fig. 26) in which only one phase is energized at each step.

– MICROSTEPPING mode (Fig. 27), in which the current follows a sine-wave profile, provided through the V_{ref} pins.

For a given output current and driving sequence the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125°C maximum).

Figure 24. IC Power Dissipation versus Output Current in HALF STEP Mode.

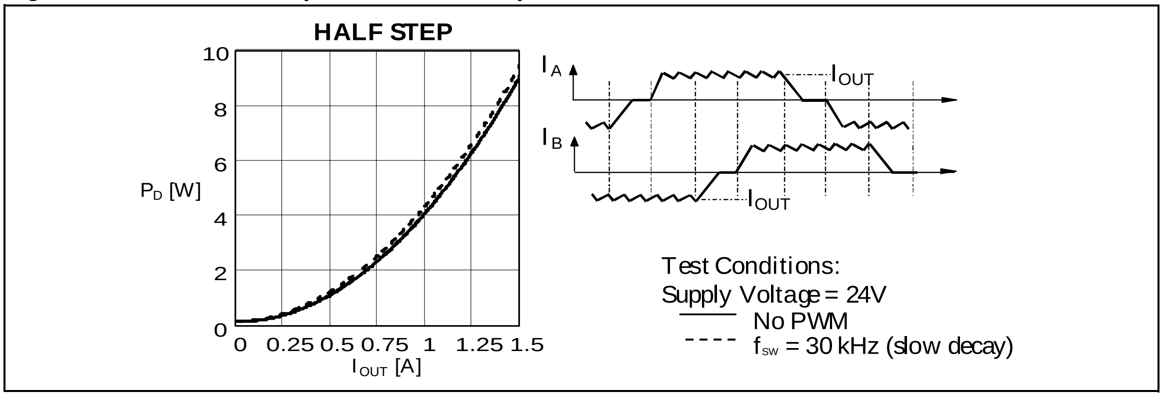


Figure 25. IC Power Dissipation versus Output Current in NORMAL Mode (full step two phase on).

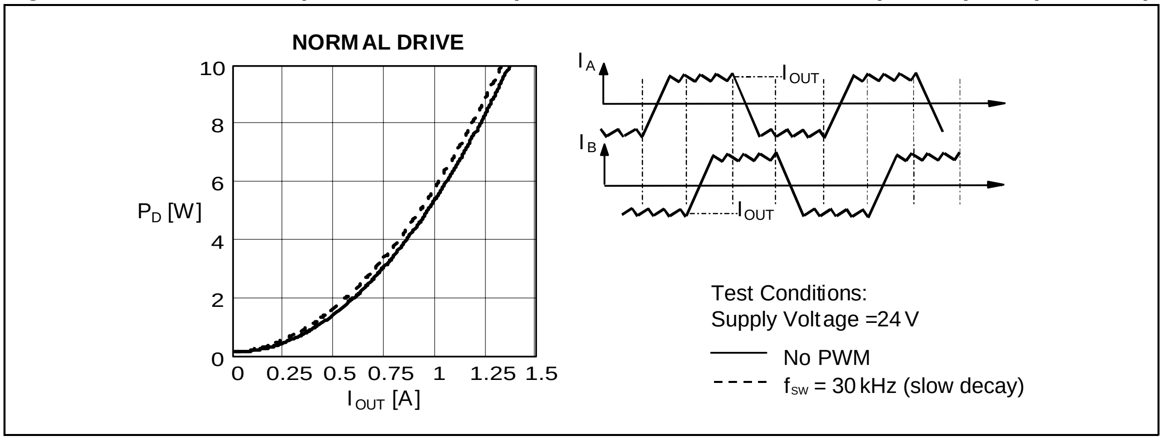


Figure 26. IC Power Dissipation versus Output Current in WAVE Mode (full step one phase on).

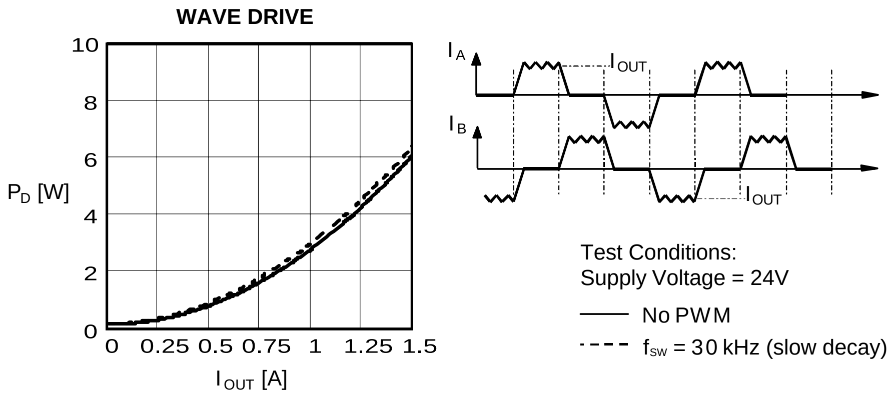
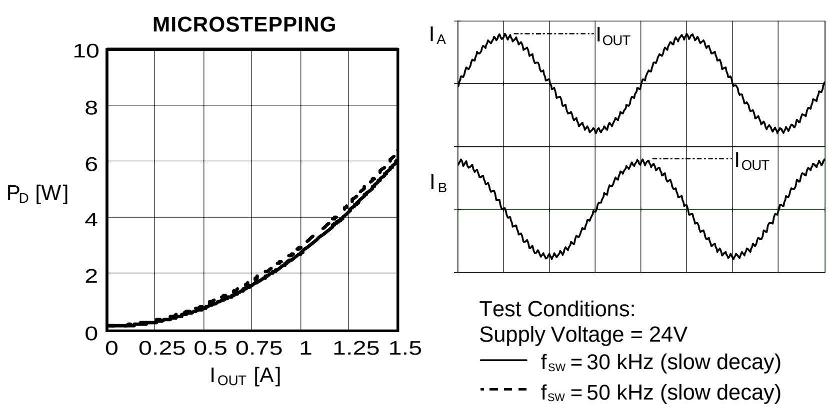


Figure 27. IC Power Dissipation versus Output Current in MICROSTEPPING Mode.



Thermal Management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Figures 28, 29 and 30 show the Junction-to-Ambient Thermal Resistance values for the PowerSO36, PowerDIP24 and SO24 packages.

For instance, using a PowerSO package with copper slug soldered on a 1.5mm copper thickness FR4 board with $6cm^2$ dissipating footprint (copper thickness of 35µm), the $R_{th(j\text{-}amb)}$ is about 35°C/W. Fig. 31 shows mounting methods for this package. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

Figure 28. PowerSO36 Junction-Ambient Thermal Resistance versus On-Board Copper Area.

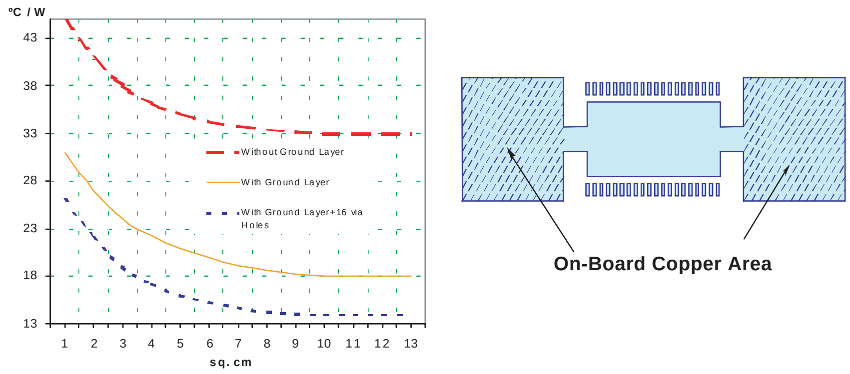


Figure 29. PowerDIP24 Junction-Ambient Thermal Resistance versus On-Board Copper Area.

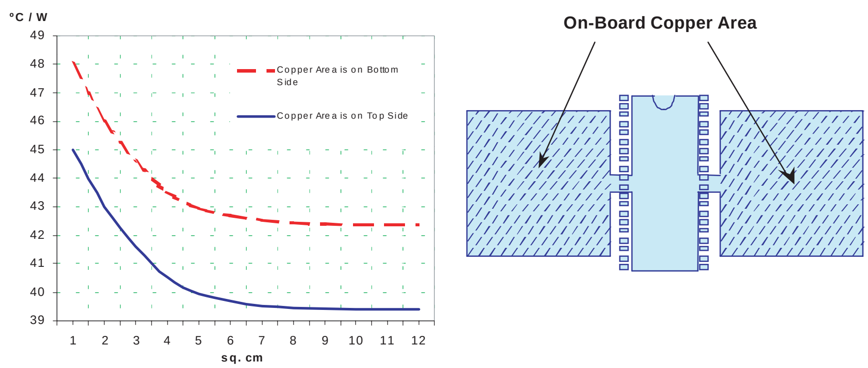


Figure 30. SO24 Junction-Ambient Thermal Resistance versus On-Board Copper Area.

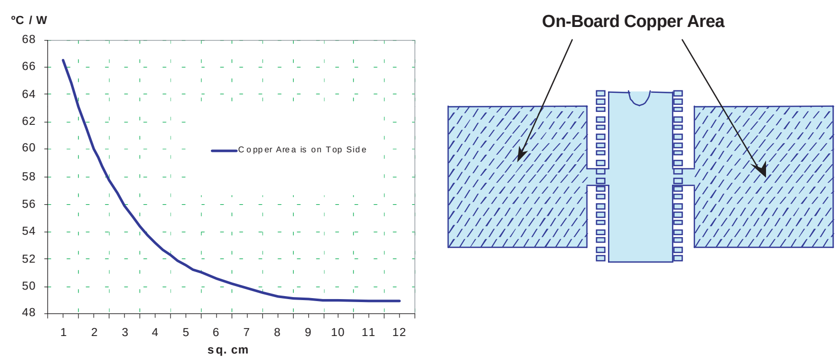
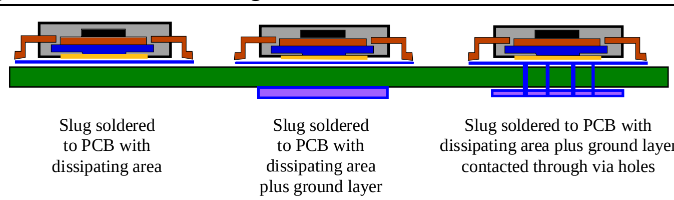


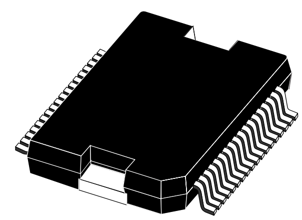
Figure 31. Mounting the PowerSO Package.



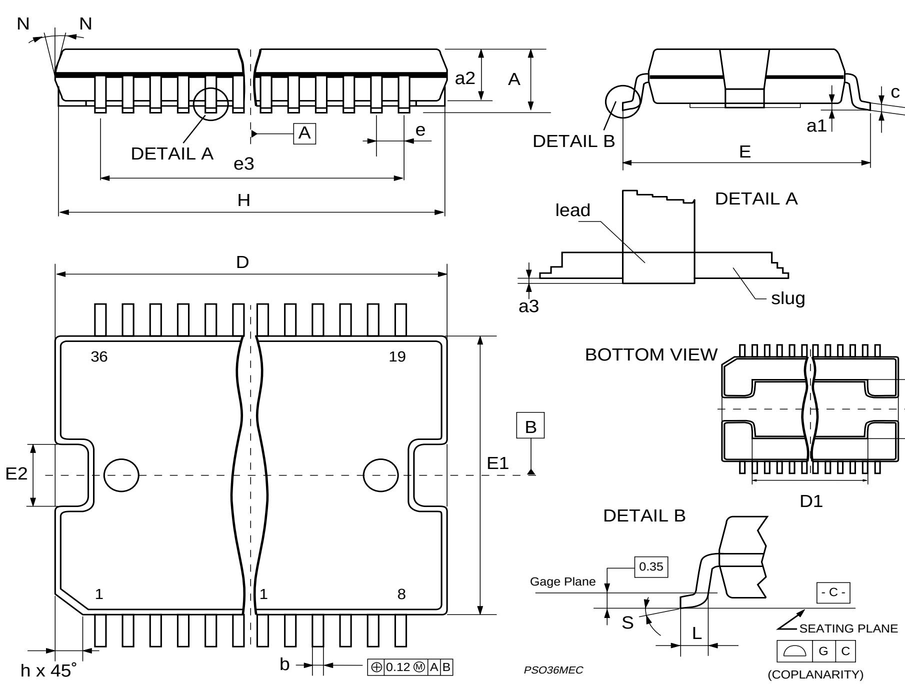
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA

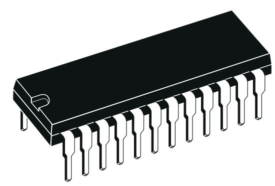


PowerSO36

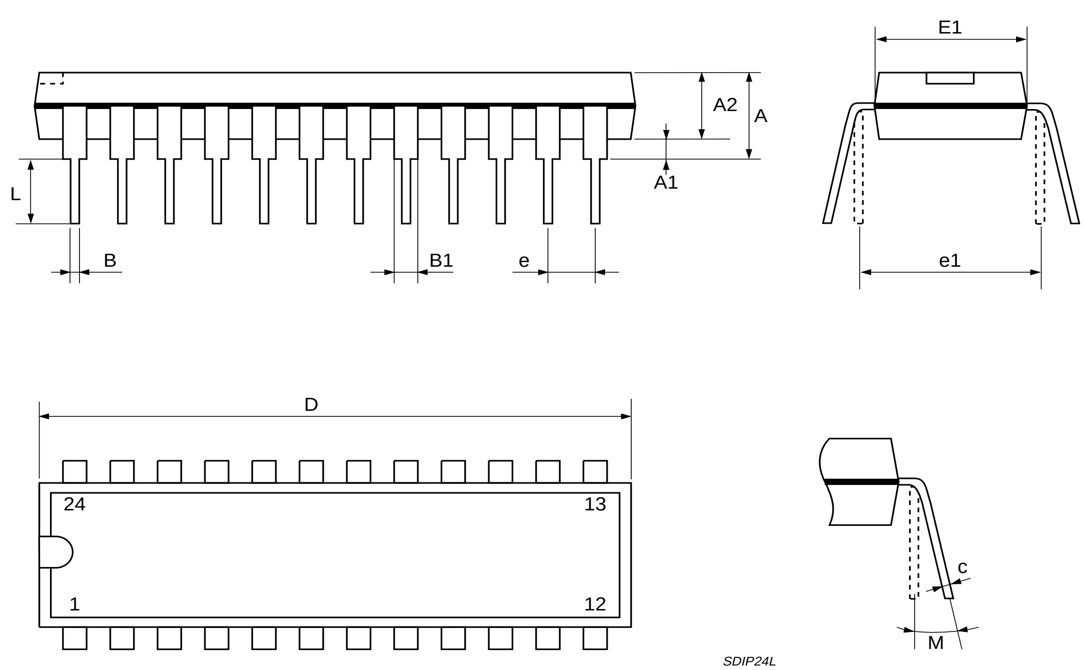


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

OUTLINE AND MECHANICAL DATA



Powerdip 24

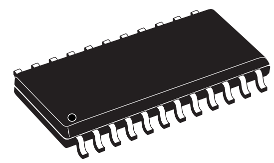


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0;75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0˚ (min.), 8˚ (max.)					
ddd			0.10			0.004

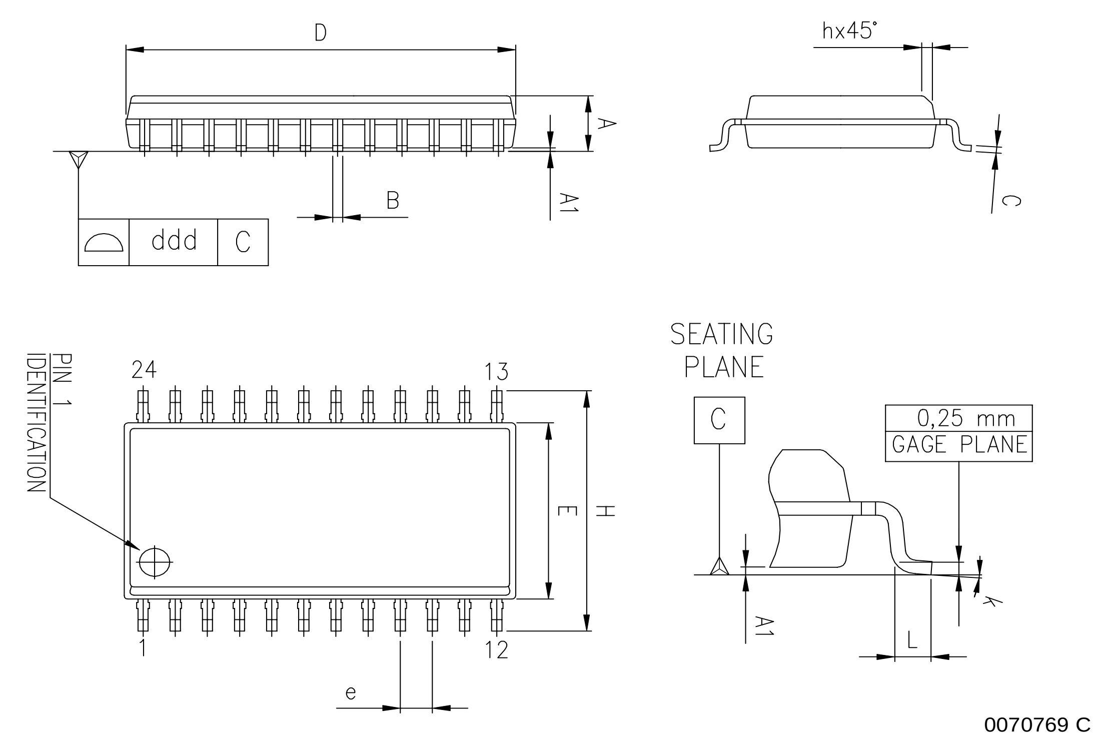
(1) “D” dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



SO24



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