12-Bit, 200kHz, *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **200kHz Sampling Rate**
- ***micro*Power:**
  1.6mW at 200kHz
  0.54mW at 75kHz
  0.06mW at 7.5kHz
- **Power Down: 3µA max**
- **Mini-DIP-8, SO-8, and MSOP-8 Packages**
- **Pseudo-Differential Input**
- **Serial Interface**

APPLICATIONS

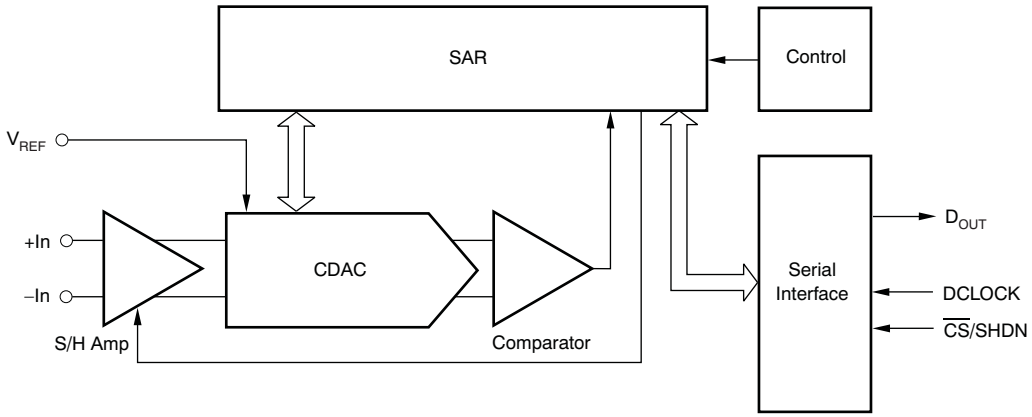
- **Battery-Operated Systems**
- **Remote Data Acquisition**
- **Isolated Data Acquisition**
- **Simultaneous Sampling, Multichannel Systems**

DESCRIPTION

The ADS7822 is a 12-bit sampling analog-to-digital (A/D) converter with ensured specifications over a 2.7V to 5.25V supply range. It requires very little power even when operating at the full 200kHz rate. At lower conversion rates, the high speed of the device enables it to spend most of its time in the power-down mode—the power dissipation is less than 60µW at 7.5kHz.

The ADS7822 also features operation from 2.0V to 5V, a synchronous serial interface, and a pseudo-differential input. The reference voltage can be set to any level within the range of 50mV to V_{CC}.

Ultra low power and small size make the ADS7822 ideal for battery-operated systems. It is also a perfect fit for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition. The ADS7822 is available in a plastic mini-DIP-8, an SO-8, or an MSOP-8 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7822E	±2	±2	MSOP-8	DGK	–40°C to +85°C	A22	ADS7822E/250	Tape and Reel, 250
							ADS7822E/2K5	Tape and Reel, 2500
ADS7822EB	±1	±1	MSOP-8	DGK	–40°C to +85°C	A22	ADS7822EB/250	Tape and Reel, 250
							ADS7822EB/2K5	Tape and Reel, 2500
ADS7822EC	±0.75	±0.75	MSOP-8	DGK	–40°C to +85°C	A22	ADS7822EC/250	Tape and Reel, 250
							ADS7822EC/2K5	Tape and Reel, 2500
ADS7822P	±2	±2	Plastic DIP-8	P	–40°C to +85°C	ADS7822P	ADS7822P	Rails, 50
ADS7822PB	±1	±1	Plastic DIP-8	P	–40°C to +85°C	ADS7822PB	ADS7822PB	Rails, 50
ADS7822PC	±0.75	±0.75	Plastic DIP-8	P	–40°C to +85°C	ADS7822PC	ADS7822PC	Rails, 50
ADS7822U	±2	±2	SO-8	D	–40°C to +85°C	ADS7822U	ADS7822U	Rails, 100
							ADS7822U/2K5	Tape and Reel, 2500
ADS7822UB	±1	±1	SO-8	D	–40°C to +85°C	ADS7822UB	ADS7822UB	Rails, 100
							ADS7822UB/2K5	Tape and Reel, 2500
ADS7822UC	±0.75	±0.75	SO-8	D	–40°C to +85°C	ADS7822UC	ADS7822UC	Rails, 100
							ADS7822UC/2K5	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.
(2) Performance grade information is marked on the reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	ADS7822	UNIT
V_{CC}	+6	V
Analog input	–0.3 to V_{CC} + 0.3	V
Logic input	–0.3 to 6	V
Case temperature	+100	°C
Junction temperature	+150	°C
Storage temperature	+125	°C
External reference voltage	+5.5	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS: $+V_{CC}$ = +2.7V

At –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, and $f_{CLK} = 16 \times f_{SAMPLE}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7822			ADS7822B			ADS7822C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT												
Full-scale input span		+In – (–In)	0		V_{REF}	0		V_{REF}	0		V_{REF}	V
Absolute input range		+In – GND	–0.2		V_{CC} + 0.2	–0.2		V_{CC} + 0.2	–0.2		V_{CC} + 0.2	V
		–In – GND	–0.2		+1.0	–0.2		+1.0	–0.2		+1.0	V
Capacitance				25			25			25		pF
Leakage current				±1			±1			±1		µA
SYSTEM PERFORMANCE												
Resolution				12			12			12		Bits
No missing codes			11			12			11			Bits
Integral linearity error			–2	±0.5	+2	–1	±0.5	+1	–0.75	±0.25	+0.75	LSB[1]
Differential linearity error			–2	±0.5	+2	–1	±0.5	+1	–0.75	±0.25	+0.75	LSB
Offset error			–3		+3	–3		+3	–1		+1	LSB
Gain error			–3		+3	–3		+3	–1		+1	LSB
Noise				33			33			33		µVrms
Power-supply rejection				82			82			82		dB
SAMPLING DYNAMICS												
Conversion time					12			12			12	Clk Cycles
Acquisition time			1.5			1.5			1.5			Clk Cycles
Throughput rate					75			75			75	kHz
DYNAMIC CHARACTERISTICS												
Total harmonic distortion		V_{IN} = 2.5V_{PP} at 1kHz		–82			–82			–82		dB
SINAD		V_{IN} = 2.5V_{PP} at 1kHz		71			71			71		dB
Spurious-free dynamic range		V_{IN} = 2.5V_{PP} at 1kHz		86			86			86		dB
REFERENCE OUTPUT												
Voltage range			0.05		V_{CC}	0.05		V_{CC}	0.05		V_{CC}	V
Resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5			5		GΩ
		$\overline{CS}$ = V_{CC}		5			5			5		GΩ
Current drain		At code 710h		8	40		8	40		8	40	µA
		f_{SAMPLE} = 7.5kHz		0.8			0.8			0.8		µA
		$\overline{CS}$ = V_{CC}		0.001	3		0.001	3		0.001	3	µA
DIGITAL INPUT/OUTPUT												
Logic family				CMOS			CMOS			CMOS		
Logic levels	V_{IH}	I_{IH} = +5µA	2.0		5.5	2.0		5.5	2.0		5.5	V
	V_{IL}	I_{IL} = +5µA	–0.3		0.8	–0.3		0.8	–0.3		0.8	V
	V_{OH}	I_{OH} = –250µA	2.1			2.1			2.1			V
	V_{OL}	I_{OL} = 250µA			0.4			0.4			0.4	V
Data format				Straight Binary			Straight Binary			Straight Binary		
POWER-SUPPLY REQUIREMENTS												
V_{CC}		Specified performance	2.7		3.6	2.7		3.6	2.7		3.6	V
		See Notes [2] and [3]	2.0		2.7	2.0		2.7	2.0		2.7	V
		See Note [3]	2.7		3.6	2.7		3.6	2.7		3.6	V
Quienscent current		f_{SAMPLE} = 7.5kHz[4][5]		20			20			20		µA
		f_{SAMPLE} = 75kHz[5]		200	325		200	325		200	325	µA
Power down		$\overline{CS}$ = V_{CC}			3			3			3	µA
TEMPERATURE RANGE												
Specified performance			–40		+85	–40		+85	–40		+85	°C

(1) LSB means least significant bit. With V_{REF} equal to +2.5V, one LSB is 0.61mV.
(2) The maximum clock rate of the ADS7822 is less than 1.2MHz in this power-supply range.
(3) See the Typical Characteristics for more information.
(4) f_{CLK} = 1.2MHz, $\overline{CS}$ = V_{CC} for 145 clock cycles out of every 160.
(5) See the Power Dissipation section for more information regarding lower sample rates.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 × f_{SAMPLE}, unless otherwise specified.

CHANGE IN OFFSET vs REFERENCE VOLTAGE

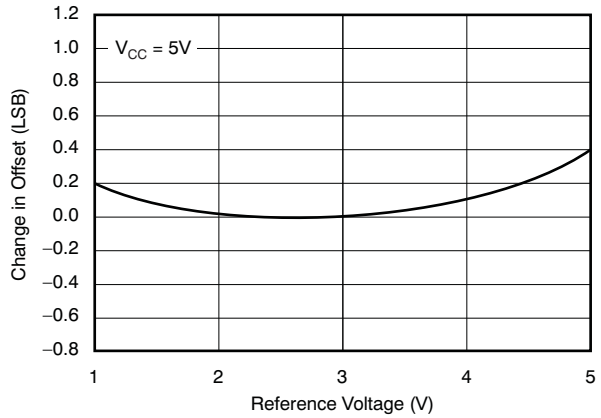

Figure 7.

CHANGE IN OFFSET vs TEMPERATURE

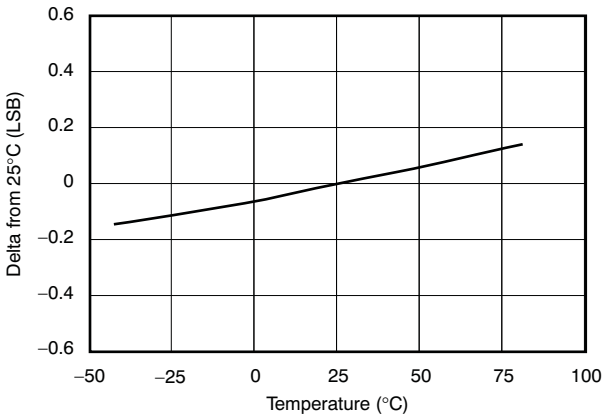

Figure 8.

CHANGE IN GAIN vs REFERENCE VOLTAGE

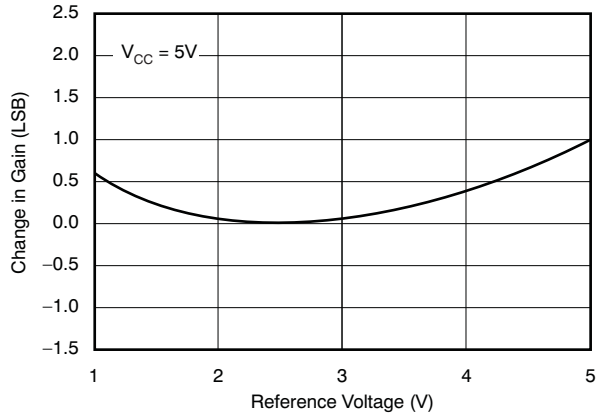

Figure 9.

CHANGE IN GAIN vs TEMPERATURE

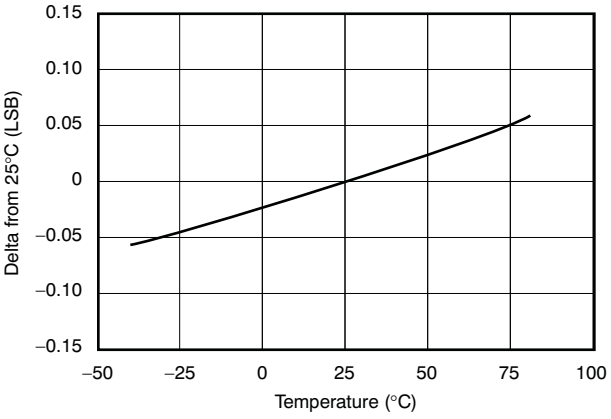

Figure 10.

EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE

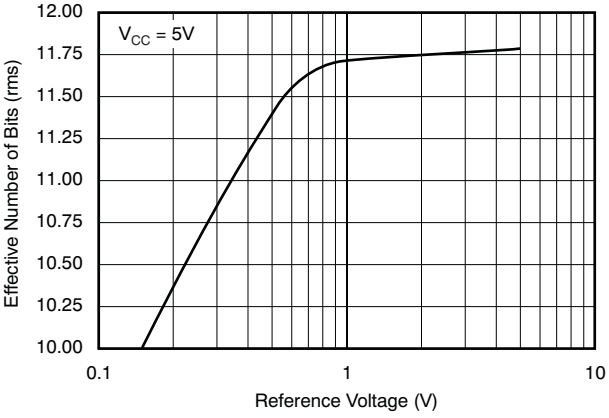

Figure 11.

PEAK-TO-PEAK NOISE vs REFERENCE VOLTAGE

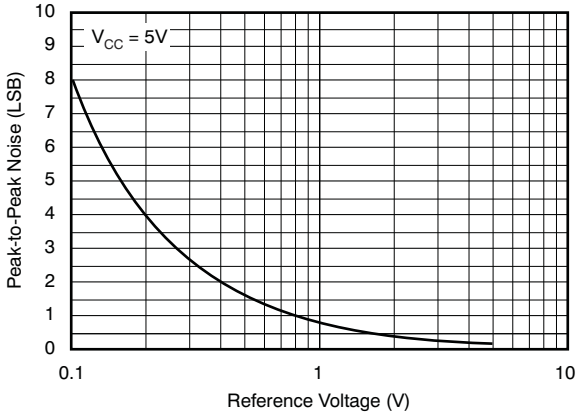

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 × f_{SAMPLE}, unless otherwise specified.

SPURIOUS FREE DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO vs FREQUENCY

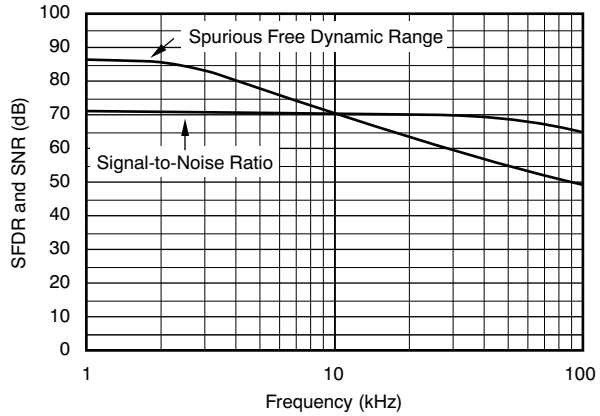

Figure 13.

TOTAL HARMONIC DISTORTION vs FREQUENCY

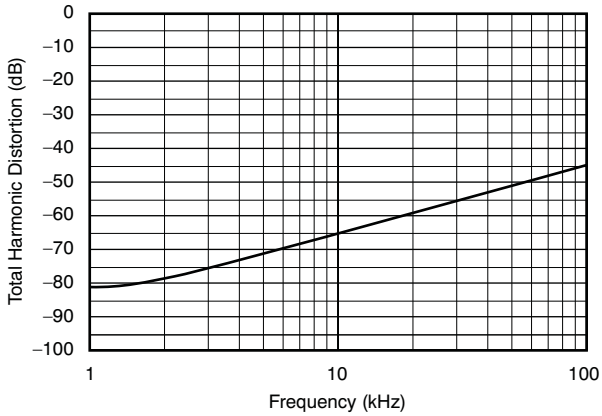

Figure 14.

SIGNAL-TO-(NOISE+DISTORTION) vs FREQUENCY

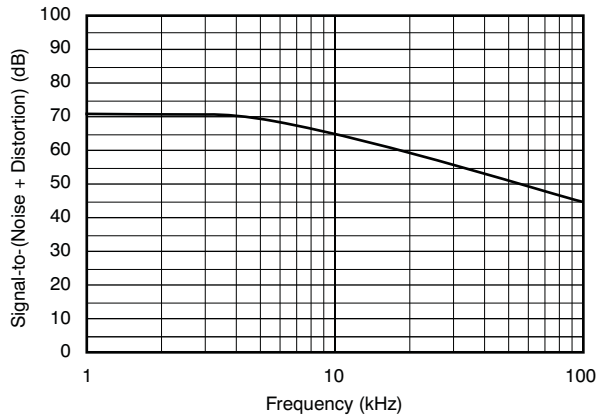

Figure 15.

SIGNAL-TO-(NOISE+DISTORTION) vs INPUT LEVEL

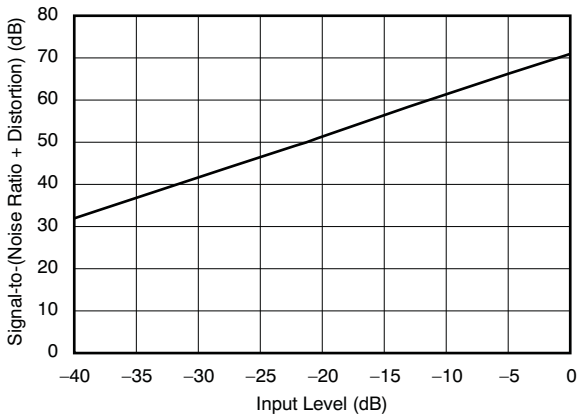

Figure 16.

REFERENCE CURRENT vs SAMPLE RATE

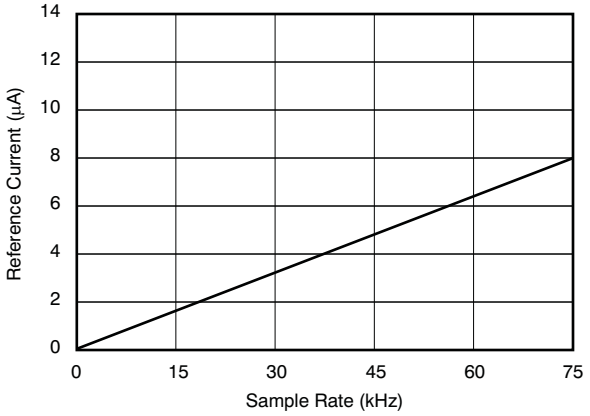

Figure 17.

REFERENCE CURRENT vs TEMPERATURE (Code = 710h)

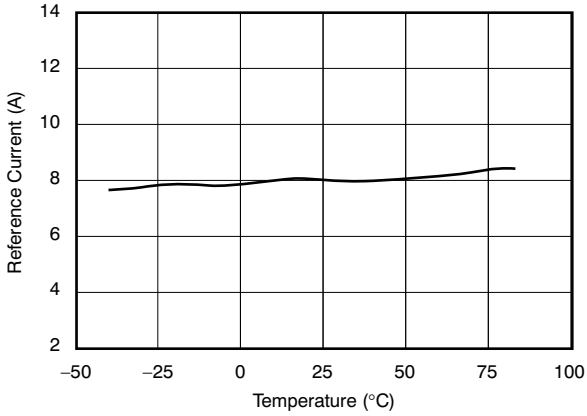

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 × f_{SAMPLE}, unless otherwise specified.

POWER-SUPPLY REJECTION vs RIPPLE FREQUENCY

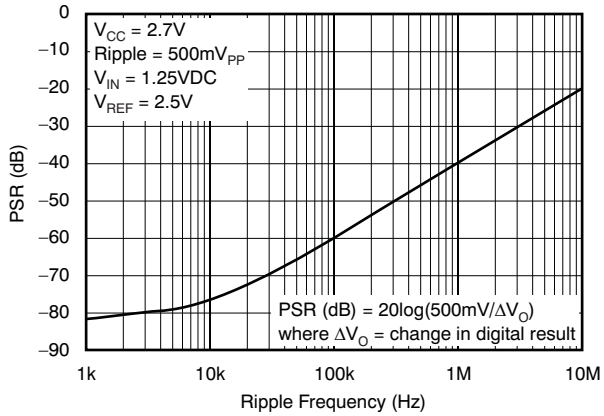

Figure 19.

POWER-SUPPLY REJECTION vs RIPPLE FREQUENCY

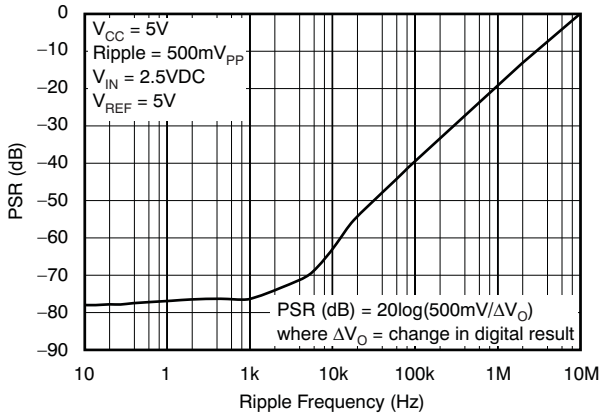

Figure 20.

CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE

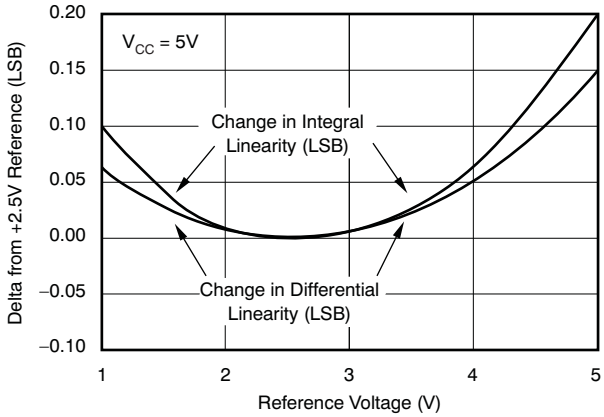

Figure 21.

THEORY OF OPERATION

The ADS7822 is a classic successive approximation register (SAR) A/D converter. The architecture is based on capacitive redistribution that inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS7822 to acquire and convert an analog signal at up to 200,000 conversions per second while consuming very little power.

The ADS7822 requires an external reference, an external clock, and a single power source (V_{CC}). The external reference can be any voltage between 50mV and V_{CC}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS7822.

The external clock can vary between 10kHz (625Hz throughput) and 3.2MHz (200kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 400ns for a supply range between 2.7V to 3.6V, or 125ns for a supply range between 4.75V to 5.25V. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7822.

The analog input is provided to two input pins: +In and –In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS7822 after the conversion is complete and to obtain the serial data least significant bit first. See the Digital Interface section for more information.

ANALOG INPUT

The +In and –In input pins allow for a pseudo-differential input signal. Unlike some converters of this type, the –In input is not resampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +In and –In is captured on the internal capacitor array.

The range of the –In input is limited to –0.2V to +1V. Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –In input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS7822 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 12-bit settling level within 1.5 clock cycles. When the converter goes into the hold mode or while it is in the power-down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –In input should not drop below GND – 200mV or exceed GND + 1V. The +In input should always remain within the range of GND – 200mV to V_{CC} + 200mV. Outside of these ranges, the converter linearity may not meet specifications.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7822 operates with a reference in the range of 50mV to V_{CC}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

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The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.32 LSB peak-to-peak of potential error to the output code. When the external reference is 50mV, the potential error contribution from the internal noise will be 50 times larger—16 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical characteristic curves Effective Number of Bits vs Reference Voltage and Peak-to-Peak Noise vs Reference Voltage. Note that the effective number of bits (ENOB) figure is calculated based on the converter signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows:

SINAD = 6.02 • ENOB + 1.76

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

DIGITAL INTERFACE

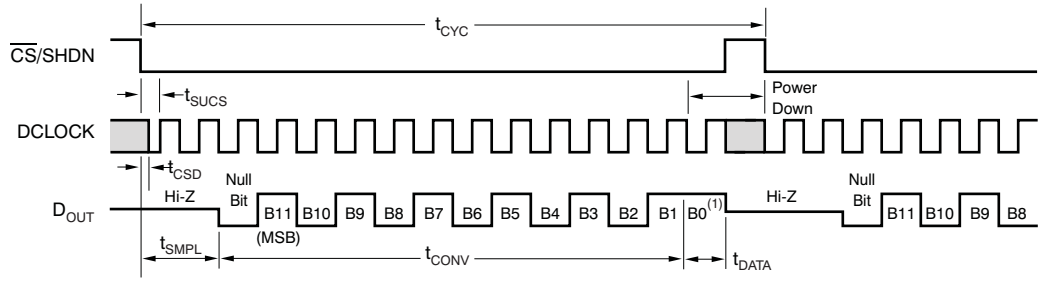
Signal Levels

The digital inputs of the ADS7822 can accommodate logic levels up to 6V regardless of the value of V_{CC}. Thus, the ADS7822 can be powered at 3V and still accept inputs from logic powered at 5V.

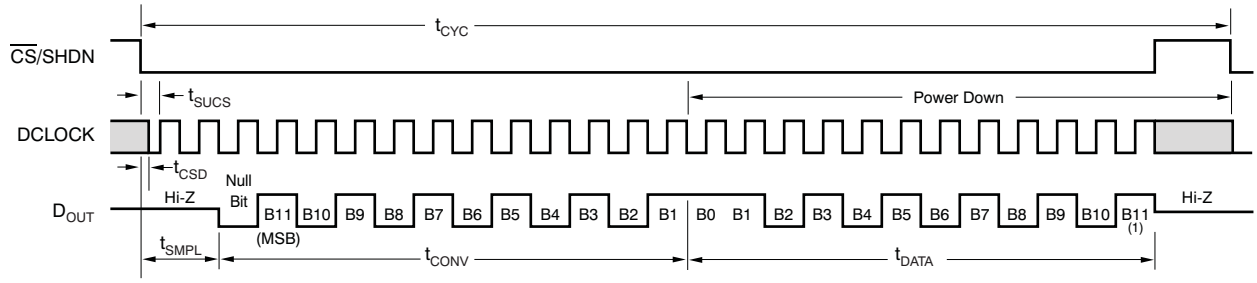
The CMOS digital output (D_{OUT}) will swing 0V to V_{CC}. If V_{CC} is 3V and this output is connected to a 5V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

Serial Interface

The ADS7822 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as shown in Figure 22 and Table 1. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.



Note: (1) After completing the data transfer, if further clocks are applied with $\overline{CS}$ LOW, the A/D will output LSB-First data then followed with zeroes indefinitely.



Note: (1) After completing the data transfer, if further clocks are applied with $\overline{CS}$ LOW, the A/D will output zeroes indefinitely.

t_{DATA}: During this time, the bias current and the comparator power down and the reference input becomes a high impedance node, leaving the CLK running to clock out LSB-first data or zeroes.

Figure 22. Basic Timing Diagrams

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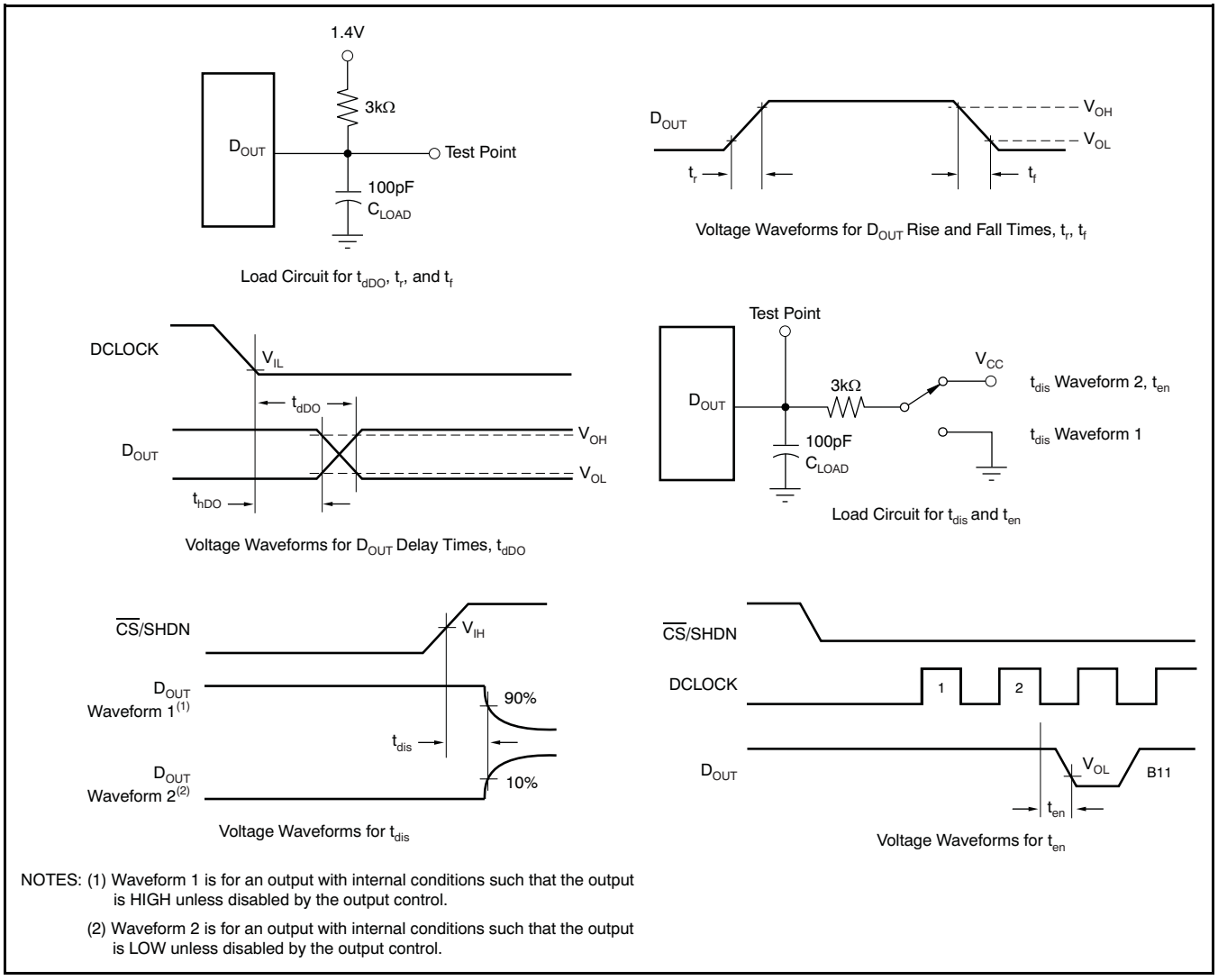
Table 1. Timing Specifications (–40°C to +85°C)

SYMBOL	DESCRIPTION	V_{CC} = 2.7V			V_{CC} = 5V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{SMPL}	Analog input sample time	1.5		2.0	1.5		2.0	Clk Cycles
t_{CONV}	Conversion time		12			12		Clk Cycles
t_{CYC}	Cycle time	16			16			Clk Cycles
t_{CSD}	$\overline{CS}$ falling to DCLOCK low			0			0	ns
t_{SUCS}	$\overline{CS}$ falling to DCLOCK rising	0.03		1000	0.03		1000	µs
t_{hDO}	DCLOCK falling to current D_{OUT} not valid	15			15			ns
t_{dDO}	DCLOCK falling to next D_{OUT} valid		130	200		85	150	ns
t_{dis}	$\overline{CS}$ rising to D_{OUT} tri-state		40	80		25	50	ns
t_{en}	DCLOCK falling to D_{OUT} enabled		75	175		50	100	ns
t_f	D_{OUT} fall time		90	200		70	100	ns
t_r	D_{OUT} rise time		110	200		60	100	ns



NOTES: (1) Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

Figure 23. Timing Diagrams and Test Circuits for the Parameters in Table 1

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A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 1.5 to 2.0 clock periods of the conversion cycle are used to sample the input signal. After the second falling DCLOCK edge, D_{OUT} is enabled and outputs a low value for one clock period. For the next 12 DCLOCK periods, D_{OUT} outputs the conversion result, most significant bit first.

After the least significant bit (B0) has been output, subsequent clocks repeat the output data, but in a least significant bit first format. After the most significant bit (B11) has been repeated, DOUT will tri-state. Subsequent clocks have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ is taken high and returned low.

Data Format

The output data from the ADS7822 is in straight binary format, as shown in Table 2. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

Table 2. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full-Scale range	V_{REF}		
Least significant bit (LSB)	$V_{REF}/4096$	BINARY CODE	HEX CODE
Full-Scale	V_{REF} – 1 LSB	1111 1111 1111	FFF
Midscale	$V_{REF}/2$	1000 0000 0000	800
Midscale – 1 LSB	$V_{REF}/2$ – 1 LSB	0111 1111 1111	7FF
Zero	0V	0000 0000 0000	000

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS7822 to convert at up to a 75kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS7822 scales directly with conversion rate. So, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS7822 goes into power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is high (see Figure 22). Ideally, each conversion should occur as quickly as possible; preferably, at a 1.2MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important since the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power-down mode is entered.

Figure 24 shows the current consumption of the ADS7822 versus sample rate. For this graph, the converter is clocked at 1.2MHz regardless of the sample rate—$\overline{CS}$ is high for the remaining sample period. Figure 25 also shows current consumption versus sample rate. However, in this case, the DCLOCK period is 1/16th of the sample period—$\overline{CS}$ is high for one DCLOCK cycle out of every 16.

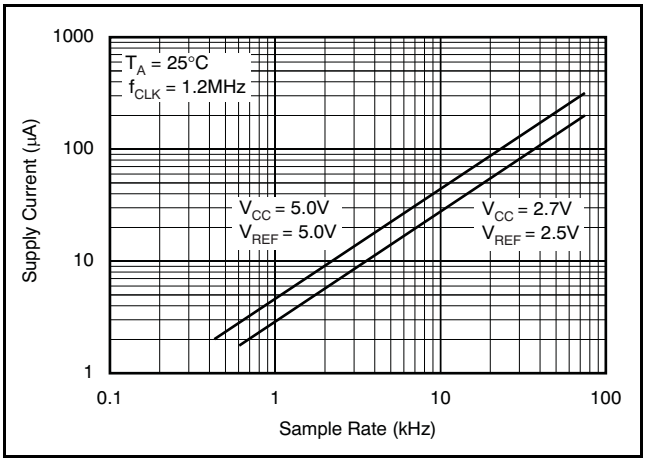

Figure 24. Maintaining f_{CLK} at the Highest Possible Rate Allows the Supply Current to Drop Linearly with the Sample Rate

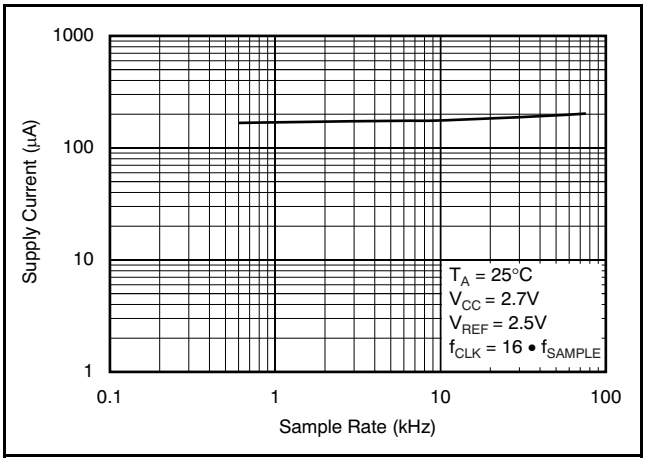

Figure 25. Scaling f_{CLK} Reduces the Supply Current Only Slightly with the Sample Rate

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There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode that is enabled when $\overline{CS}$ is high. While both shutdown the analog section, the digital section is completely shutdown only when $\overline{CS}$ is high. Thus, if $\overline{CS}$ is left low at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is high; see Figure 26 for more information.

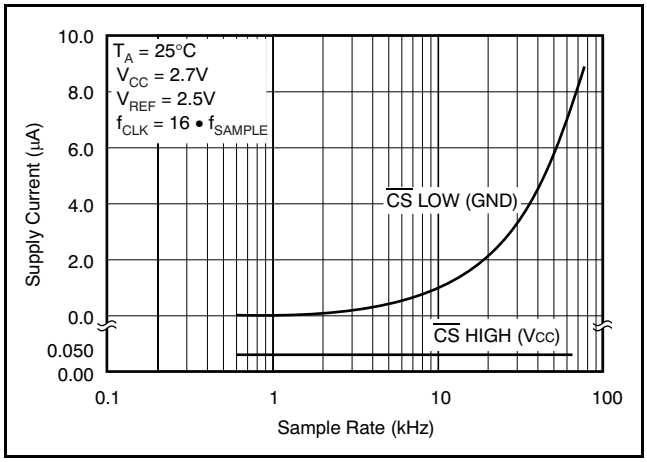

Figure 26. Shutdown Current with $\overline{CS}$ High is Typically 50nA, Regardless of the Clock. Shutdown Current with $\overline{CS}$ Low varies with Sample Rate.

Power dissipation can also be reduced by lowering the power-supply voltage and the reference voltage. The ADS7822 operates over a V_{CC} range of 2.0V to 5.25V. It will run up to a 200kHz throughput rate over a supply range of 4.75V to 5.25V; therefore, it can be clocked at up to 3.2MHz. However, at voltages below 2.7V, the converter does not run at a 75kHz sample rate. See the Typical Characteristic curves for more information regarding power-supply voltage and maximum sample rate.

Short Cycling

Another way of saving power is to use the $\overline{CS}$ signal to short-cycle the conversion. Because the ADS7822 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short-cycled. This term means that the conversion can be terminated at any time. For example, if only eight bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ high) after the eighth bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 12-bit conversion result may not be needed. If so, the conversion can be terminated after the first *n*-bits, where *n* might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, because they spend more time in the power-down mode.

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LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7822 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At a 75kHz conversion rate, the ADS7822 makes a bit decision every 830ns. If the supply range is limited to 4.75V to 5.25V, then up to a 200kHz conversion rate can be used, which reduces the bit decision time to 312ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 12-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high-power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter DCLOCK signal because the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS7822 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the ADS7822 package as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor can be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS7822 draws very little current from the reference on average, there are still instantaneous current demands placed on the external reference circuitry.

Also, keep in mind that the ADS7822 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz), can be difficult to remove.

The GND pin on the ADS7822 should be placed on a clean ground point. In many cases, this will be the analog ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figure 27 and Figure 28 show some typical application circuits for the ADS7822. Figure 27 uses an ADS7822 and a multiplexer to provide for a flexible data acquisition circuit. A resistor string provides for various voltages at the multiplexer input. The selected voltage is buffered and driven into V_{REF}. As shown in Figure 27, the input range of the ADS7822 is programmable to 100mV, 200mV, 300mV, or 400mV. The 100mV range would be useful for sensors such as the thermocouple shown.

Figure 28 shows a basic data acquisition system. The ADS7822 input range is 0V to V_{CC}, as the reference input is connected directly to the power supply. The 5Ω resistor and 1µF to 10µF capacitor filter the microcontroller noise on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

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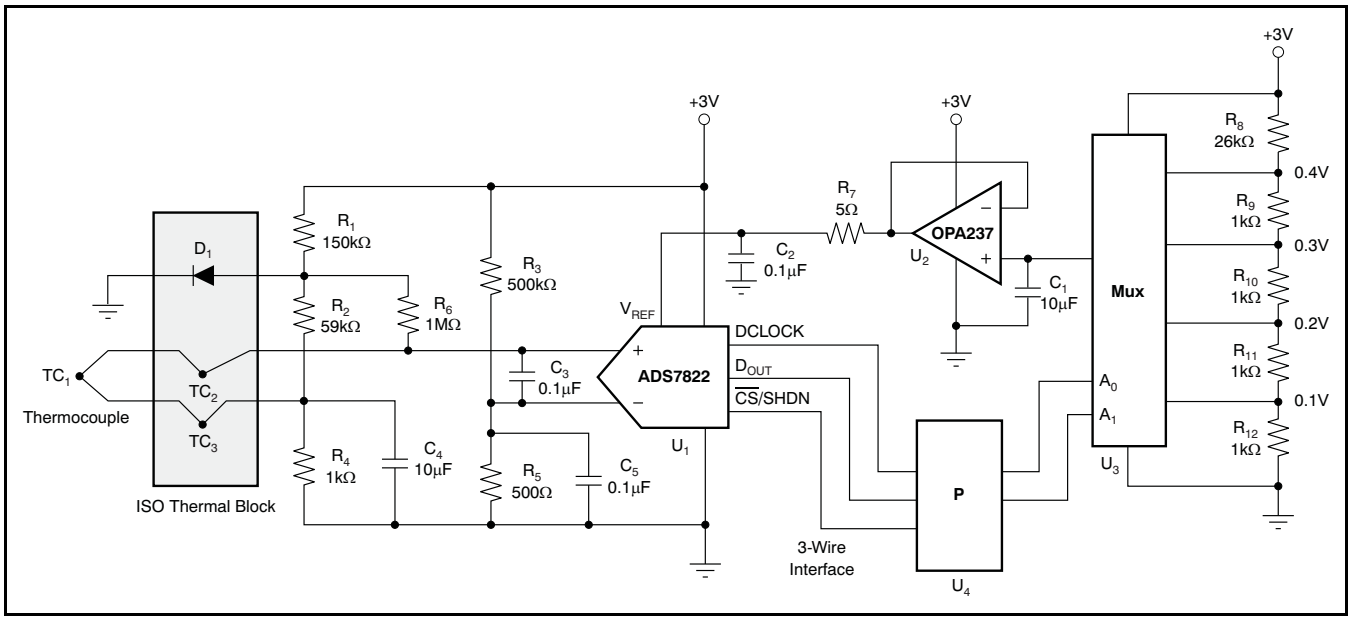

Figure 27. Thermocouple Application Using a Mux to Scale the Input Range of the ADS7822

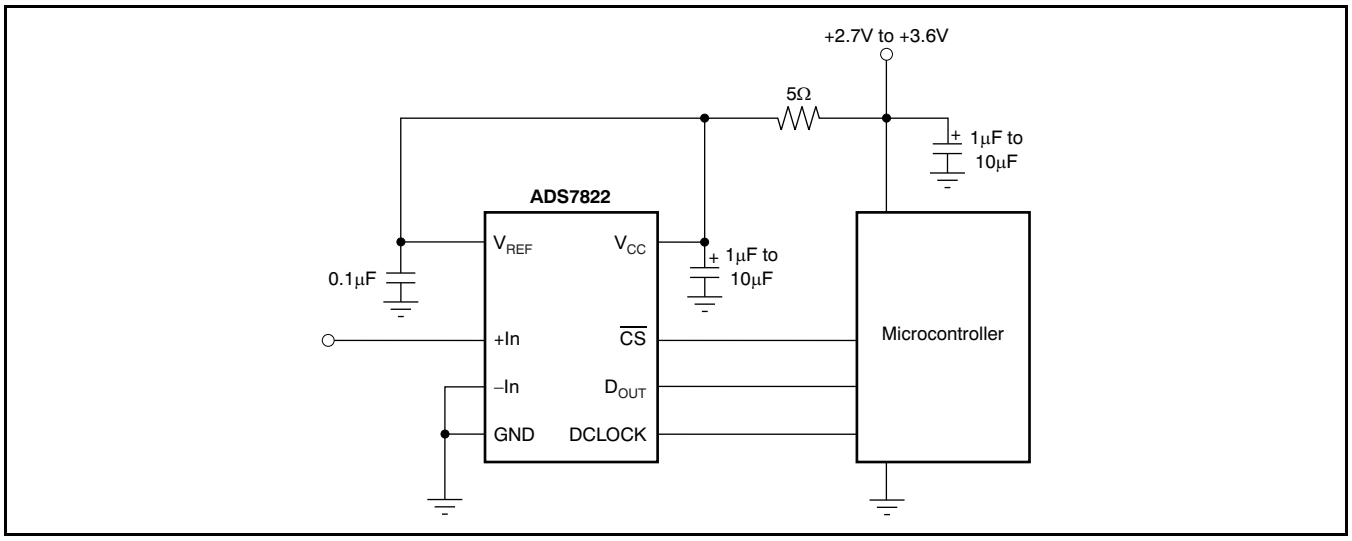

Figure 28. Basic Data Acquisition System

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Revision History

Changes from Revision B (May 2006) to Revision C **Page**

- Added – GND to absolute input range test conditions 3
- Added – GND to absolute input range test conditions 3
- Changed V_{CC} min from 3.6 V to 2.7 V 3
- Changed V_{CC} max from 5.25 V to 3.6 V 3
- Changed V_{CC} min from 3.6 V to 2.7 V 3
- Changed V_{CC} max from 5.25 V to 3.6 V 3
- Changed V_{CC} min from 3.6 V to 2.7 V 3
- Changed V_{CC} max from 5.25 V to 3.6 V 3
- Added – GND to absolute input range test conditions 4
- Added – GND to absolute input range test conditions 4

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7822E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EB/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EB/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EB/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EB/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EC/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EC/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EC/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822EC/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A22	Samples
ADS7822U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U	Samples
ADS7822U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U	Samples
ADS7822U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U	Samples
ADS7822UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7822UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U B	Samples
ADS7822UB/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U B	Samples
ADS7822UBG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U B	Samples
ADS7822UC	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U C	Samples
ADS7822UC/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U C	Samples
ADS7822UCG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7822U C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ADS7822 :

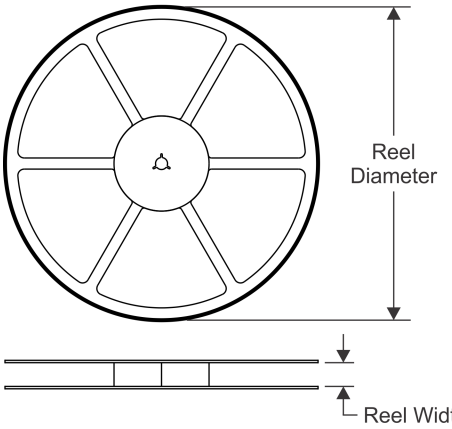
- Automotive: ADS7822-Q1

NOTE: Qualified Version Definitions:

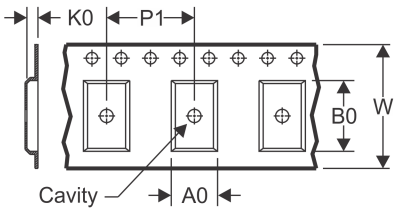
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

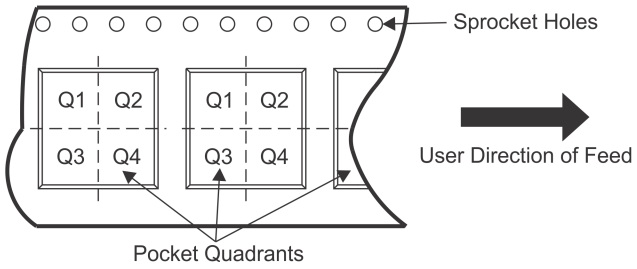


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

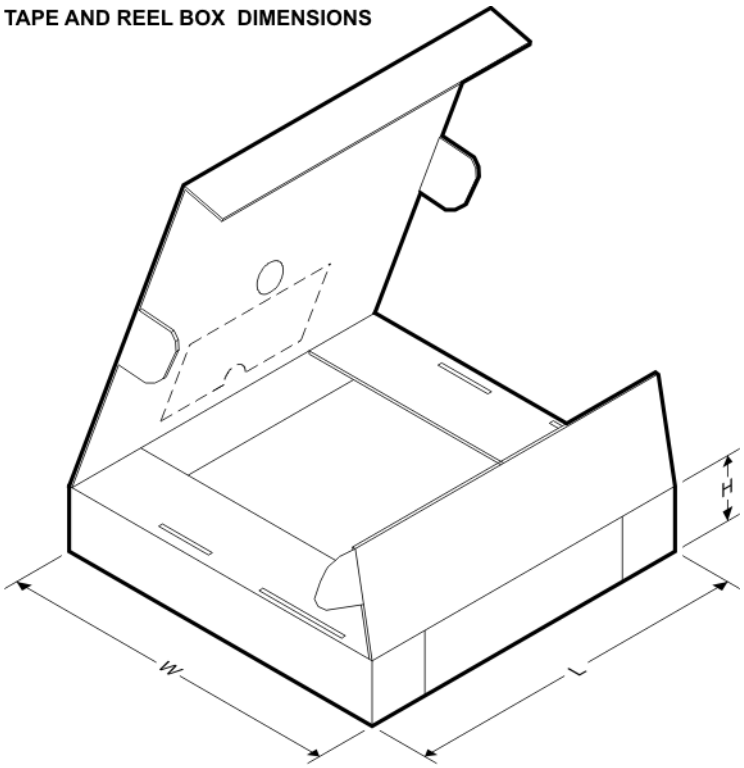
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7822E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7822E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7822EB/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7822EB/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7822EC/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7822EC/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7822U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7822UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7822UC/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

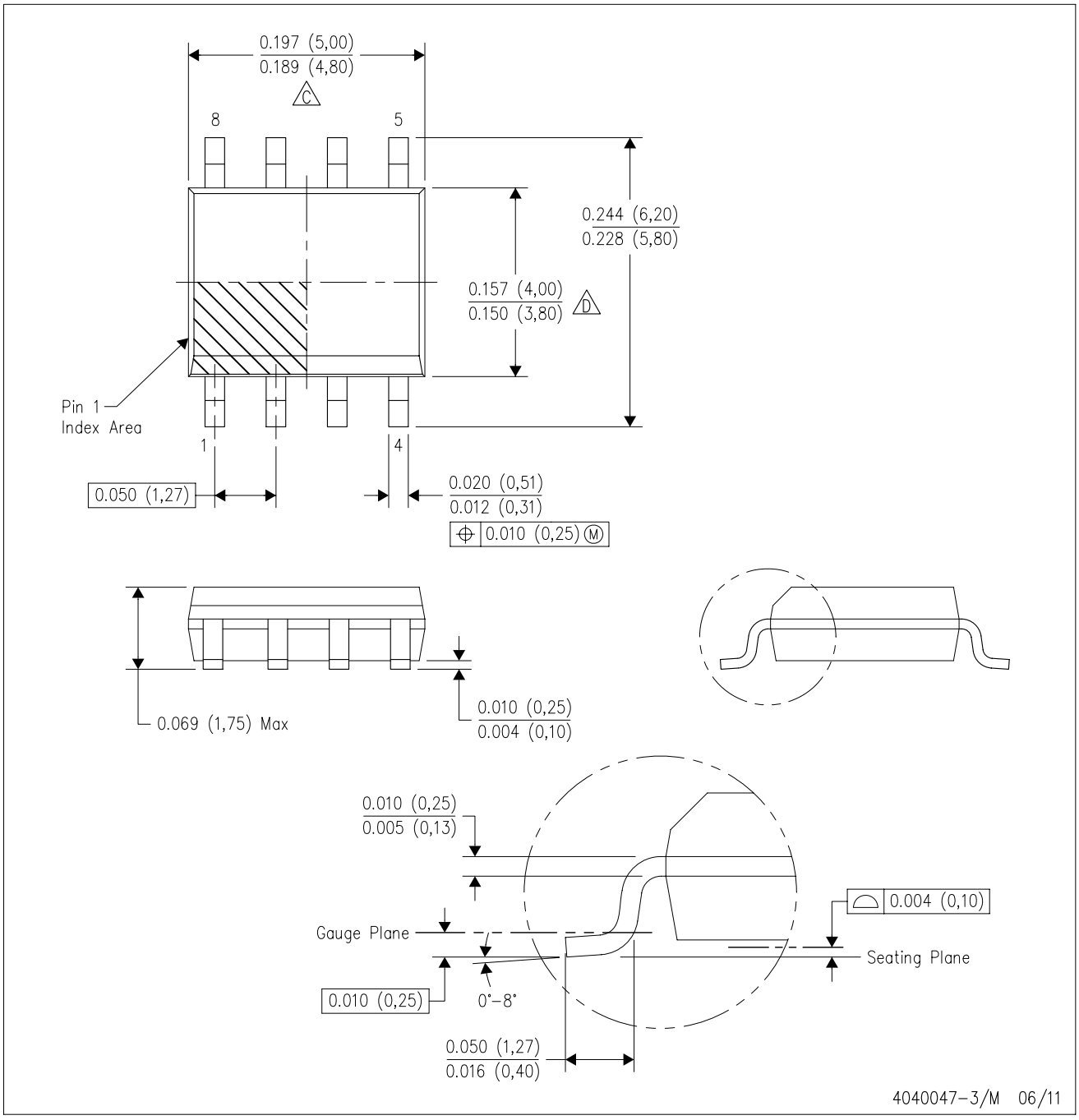
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

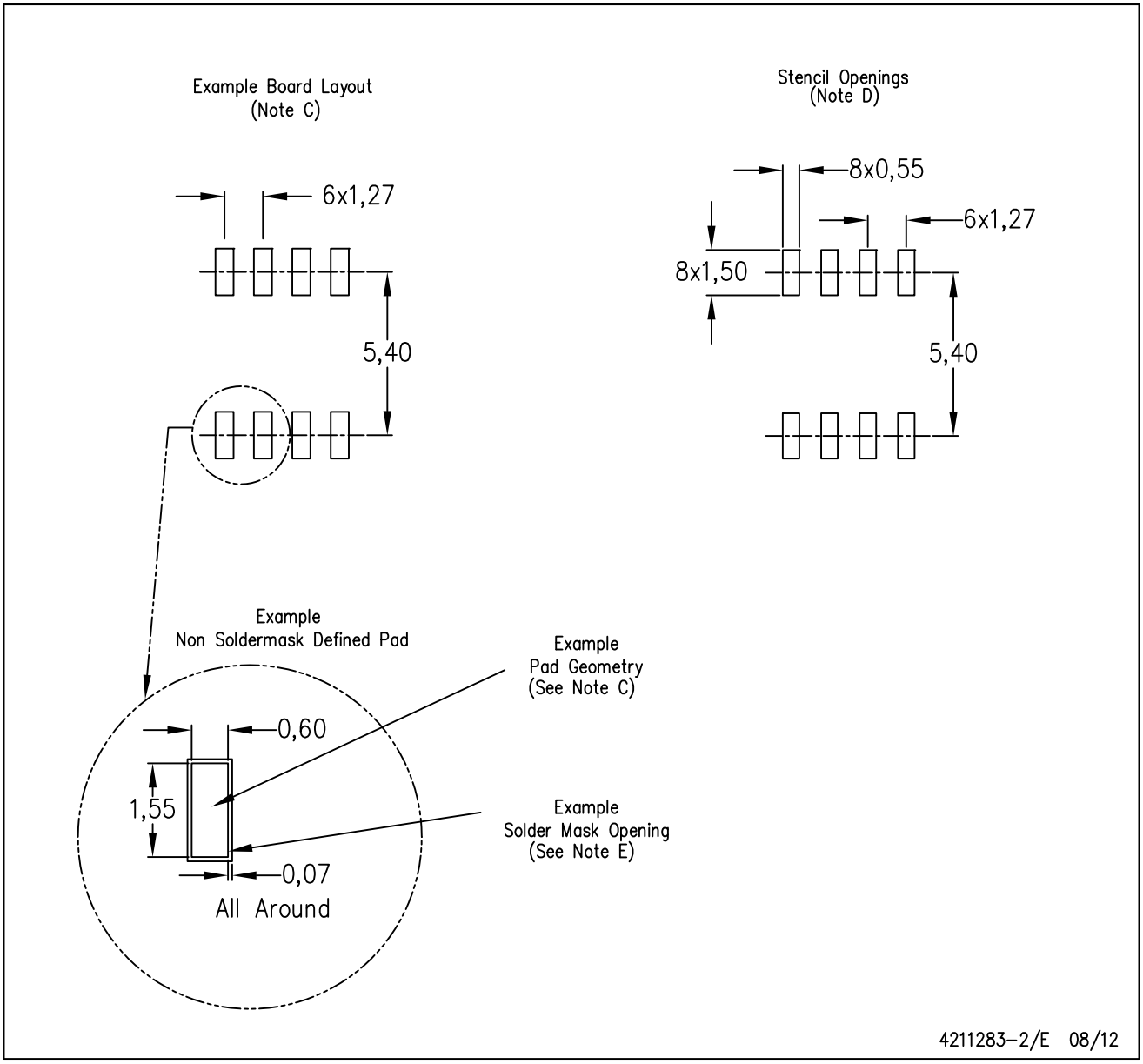
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7822E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7822E/2K5	VSSOP	DGK	8	2500	367.0	367.0	38.0
ADS7822EB/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7822EB/2K5	VSSOP	DGK	8	2500	367.0	367.0	38.0
ADS7822EC/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7822EC/2K5	VSSOP	DGK	8	2500	367.0	367.0	38.0
ADS7822U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
ADS7822UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0
ADS7822UC/2K5	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



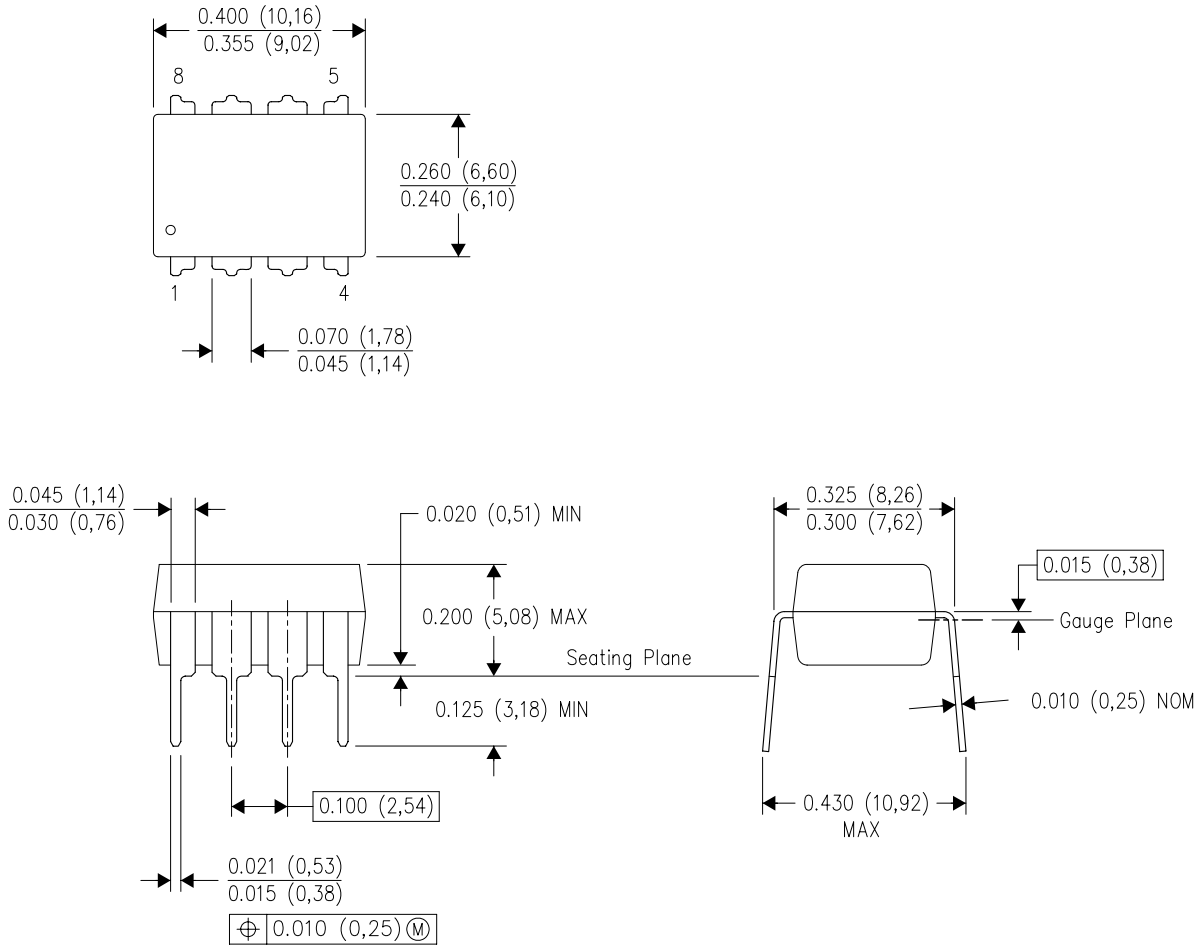
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



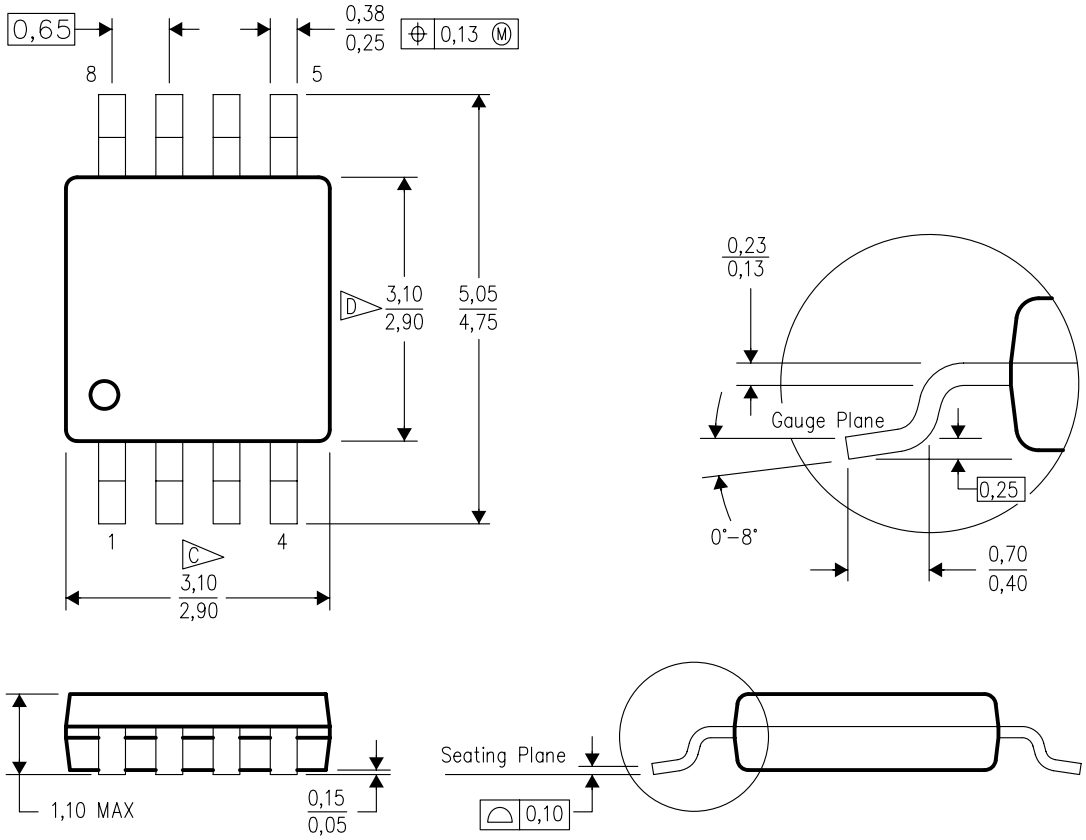
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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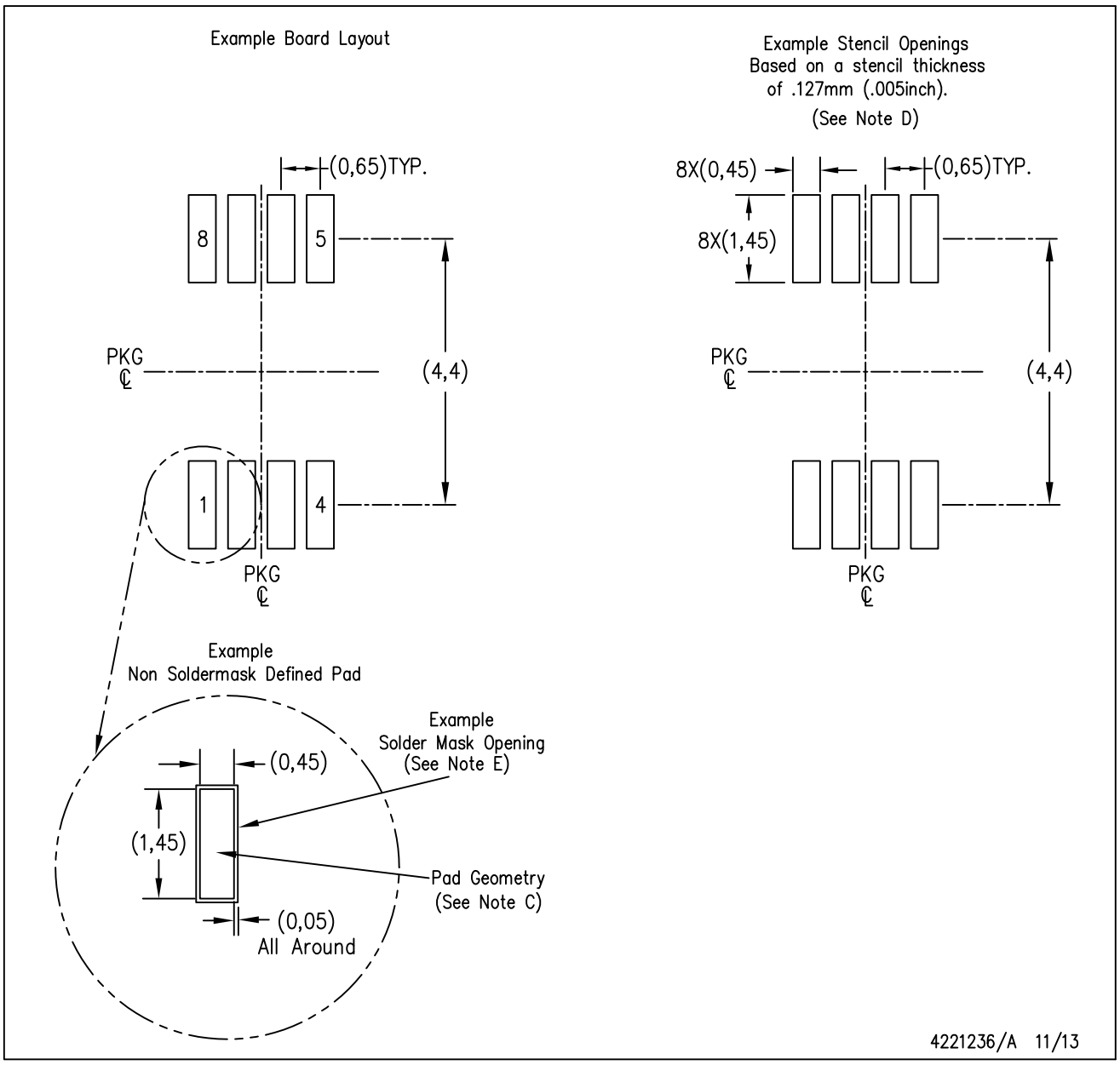
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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