AM26LV31 Low-Voltage High-Speed Quadruple Differential Line Drivers

1 Features

- Switching Rates up to 32 MHz
- Operate From a Single 3.3-V Supply
- Propagation Delay Time: 8 ns Typical
- Pulse Skew Time: 500 ps Typical
- High Output-Drive Current: ±30 mA
- Controlled Rise and Fall Times: 3 ns Typical
- Differential Output Voltage With 100-Ω Load: 1.5 V Typical
- Ultra-Low Power Dissipation
  - dc, 0.3 mW Maximum
  - 32 MHz All Channels (No Load), 385 mW Typical
- Accept 5-V Logic Inputs With 3.3-V Supply
- Low-Voltage Pin-to-Pin Compatible Replacement for AM26C31, AM26LS31, MB571
- High Output Impedance in Power-Off Condition
- Driver Output Short-Protection Circuit
- Package Options Include Plastic Small-Outline (D, NS) Packages

2 Applications

- Motor Control: Brushless DC and Brushed DC
- Field Transmitters: Temperature Sensors and Pressure Sensors
- Temperature Sensors or Controllers Using Modbus

3 Description

The AM26LV31C and AM26LV31I are BiCMOS quadruple differential line drivers with 3-state outputs. They are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply-voltage range.

The devices are optimized for balanced-bus transmission at switching rates up to 32 MHz. The outputs have very high current capability for driving balanced lines such as twisted-pair transmission lines and provide a high impedance in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable inputs. The AM26LV31C and AM26LV31I are designed using Texas Instruments proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed. These devices offer optimum performance when used with the AM26LV32 quadruple line receivers.

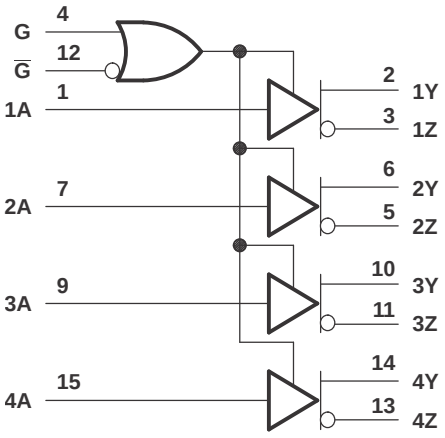
The AM26LV31C is characterized for operation from 0°C to 70°C. The AM26LV31I is characterized for operation from –45°C to 85°.C

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AM26LV31C	SOIC (D) 16	9.90 mm x 3.91 mm
AM26LV31I	SOIC (D) 16	9.90 mm x 3.91 mm
	SO (NS) 16	10.3 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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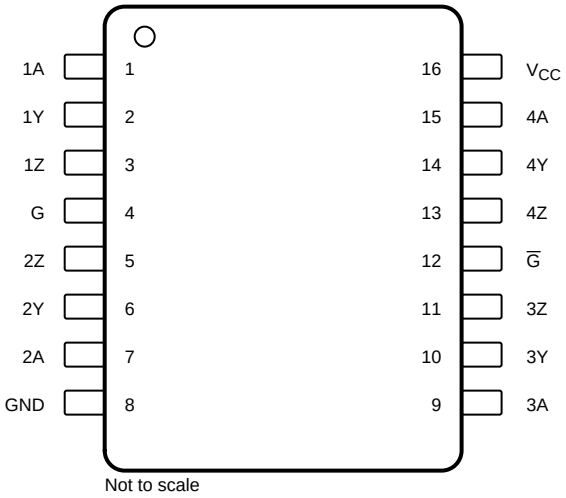
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2005) to Revision H	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed the t_{PLH} and t_{PHL} MAX value From: 12 ns To: 20 ns in the *Switching Characteristics*	5
• Changed the $t_{sk(p)}$ and $t_{sk(o)}$ MAX value From: 1.5 ns To: 3 ns in the *Switching Characteristics*	5

5 Pin Configuration and Functions

D or NS Package
SOIC 16 Pins
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Driver 1 input
2	1Y	O	Driver 1 output
3	1Z	O	Driver 1 inverted output
4	G	I	Active high enable
5	2Z	O	Driver 2 inverted output
6	2Y	O	Driver 2 output
7	2A	I	Driver 2 input
8	GND	—	Ground pin
9	3A	I	Driver 3 input
10	3Y	O	Driver 3 output
11	3Z	O	Driver 3 inverted output
12	$\overline{G}$	I	Active low enable
13	4Z	O	Driver 4 inverted output
14	4Y	O	Driver 4 output
15	4A	I	Driver 4 input
16	V_{CC}	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage range, V_{CC}(2)	–0.3	6	V
Input voltage range, V_I	–0.3	6	V
Output voltage range, V_O	–0.3	6	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–30	mA
I_{OL}	Low-level output current				30	mA
T_A	Operating free-air temperature	AM26LV31C	0		70	°C
		AM26LV31I	–45		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	NS (SO) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.9	76.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.1	37.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	4.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.8	37.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over recommended operating supply-voltage and free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = 18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = –12 mA	1.85	2.3		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OH} = 12 mA		0.8	1.05	V
$\|V_{OD}\|$	Differential output voltage(2)	R_L = 100 Ω		0.95	1.5		V
V_{OC}	Common-mode output voltage			1.3	1.55	1.8	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)					±0.2	V
I_O	Output current with power off	V_O = –0.25 V or 6 V,	V_{CC} = 0			±100	µA
I_{OZ}	Off-state (high-impedance state) output current	V_O = –0.25 V or 6 V,	G = 0.8 V or $\overline{G}$ = 2 V			±100	µA
I_H	High-level input current	V_{CC} = 0 or 3 V,	V_I = 5.5 V			10	µA
I_L	Low-level input current	V_{CC} = 3.6 V,	V_I = 0			–10	µA
I_{OS}	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0			–200	mA
I_{CC}	Supply current (all drivers)	V_I = V_{CC} or GND,	No load			100	µA
C_{pd}	Power-dissipation capacitance (all drivers)(3)	No load			160		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

6.6 Switching Characteristics

V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 3		4	8	20	ns
t_{PHL}	Propagation delay time, high- to low-level output			4	8	20	ns
t_t	Transition time (t_r or t_f)				3		ns
SR	Slew rate, single-ended output voltage	See Note (2) and Figure 3			0.3	1	V/ns
t_{PZH}	Output-enable time to high level	See Figure 4			10	20	ns
t_{PZL}	Output-enable time to low level	See Figure 5			10	20	ns
t_{PHZ}	Output-disable time from high level	See Figure 4			10	20	ns
t_{PLZ}	Output-disable time from low level	See Figure 5			10	20	ns
$t_{sk(p)}$	Pulse skew	f = 32 MHz,	See Note (3)		0.5	3	ns
$t_{sk(o)}$	Skew limit	f = 32 MHz				3	ns
$t_{sk(lim)}$	Skew limit (device to device)	f = 32 MHz,	See Note (4)			3	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Slew rate is defined by Equation 1
(3) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(4) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

$$SR = \frac{90\%(V_{OH} - V_{OL}) - 10\% (V_{OH} - V_{OL})}{t_r}$$, the differential slew rate of V_{CC} is 2 x SR. (1)

6.7 Typical Characteristics

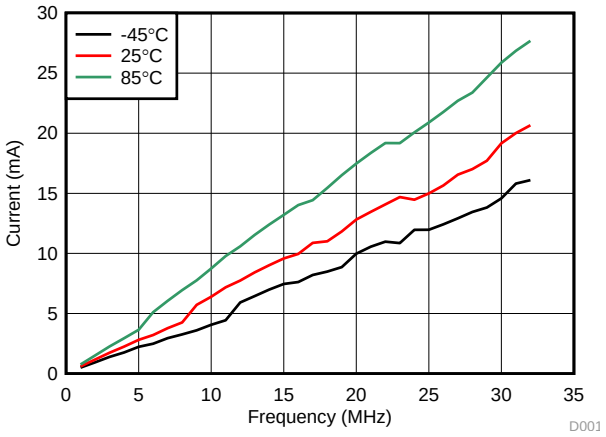


Figure 1. Current vs Frequency

7 Parameter Measurement Information

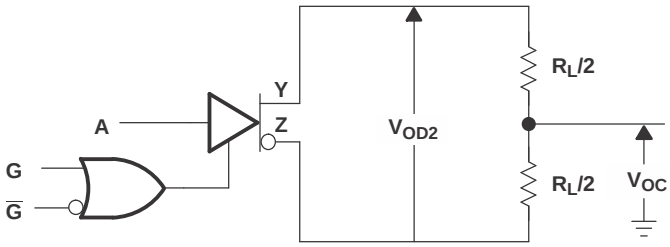
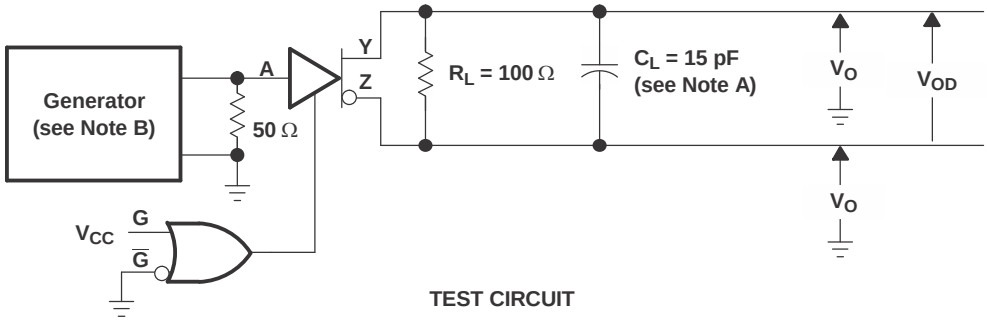
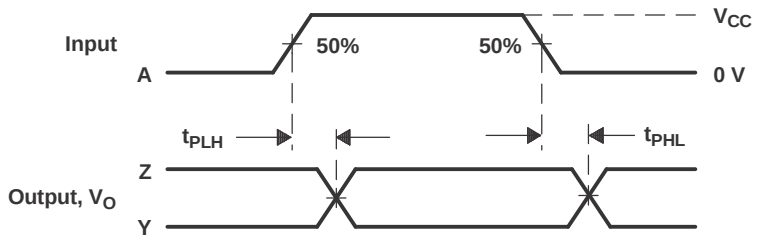


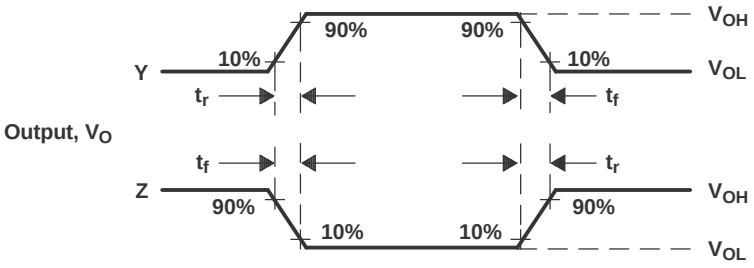
Figure 2. Differential and Common-Mode Output Voltages



TEST CIRCUIT



PROPAGATION DELAY TIMES



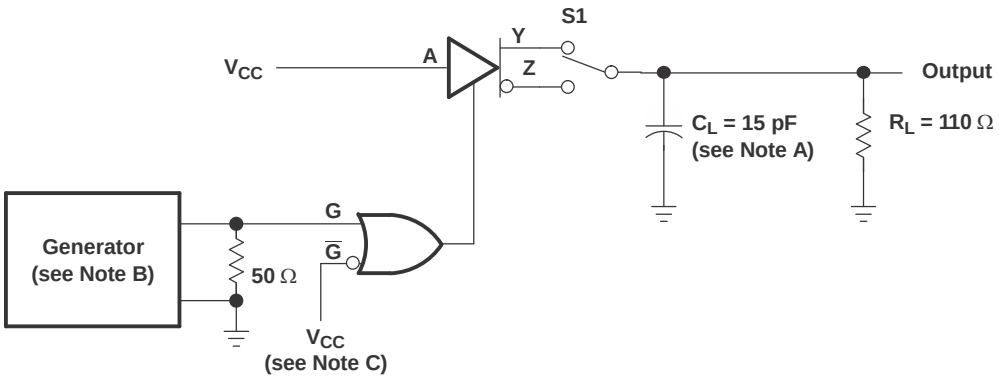
RISE AND FALL TIMES

A. C_L includes probe and jig capacitance.

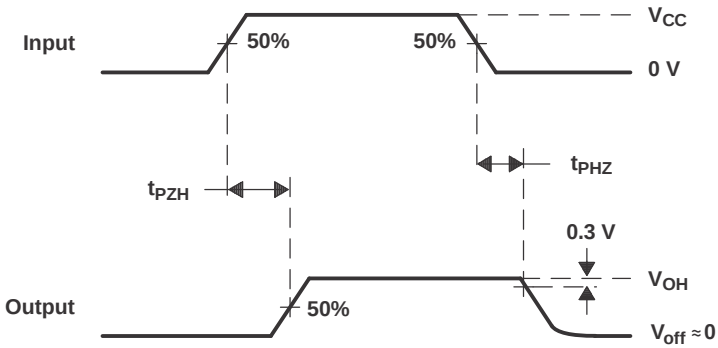
B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, Z_O = 50 Ω, 50%v duty cycle, t_r and t_f ≤ 2 ns.

Figure 3. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

Parameter Measurement Information (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

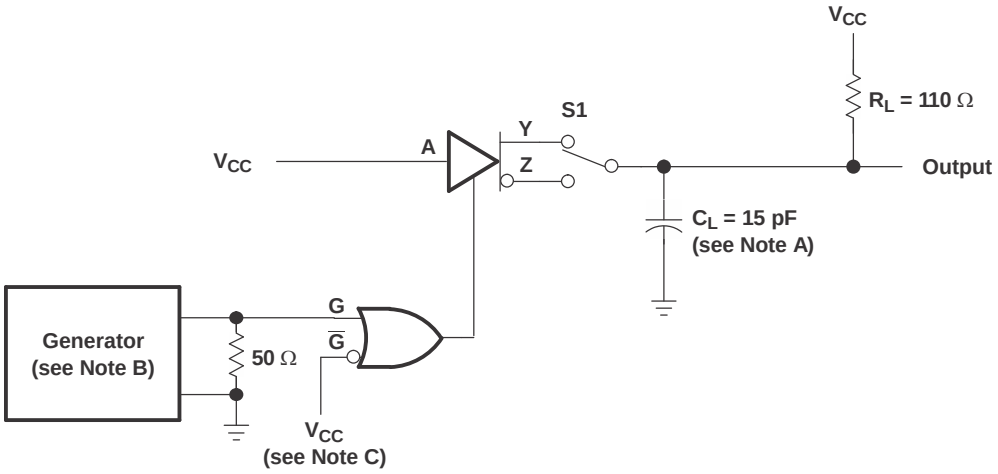
A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.

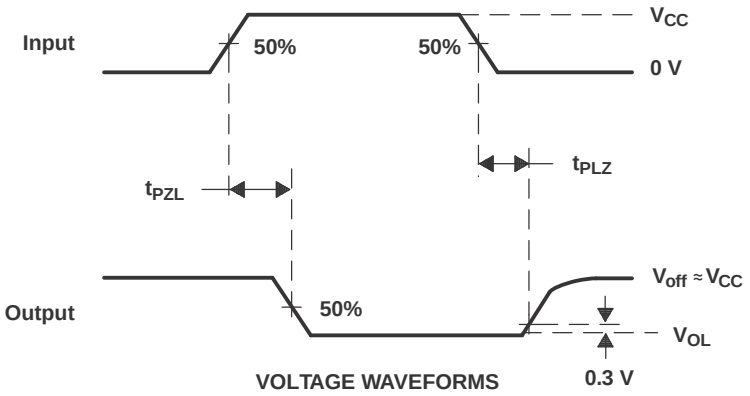
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

Parameter Measurement Information (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

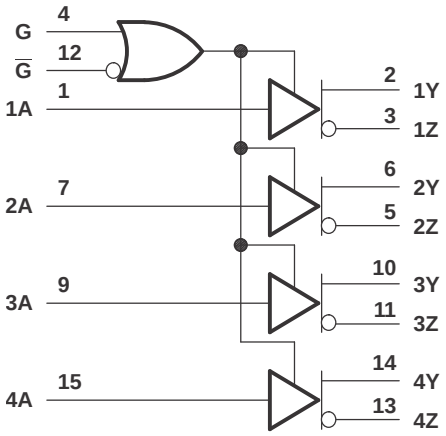
Figure 5. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

8 Detailed Description

8.1 Overview

The AM26LV31C and AM26LV31I are BiCMOS quadruple differential line drivers with 3-state outputs. The devices are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with a single 3.3-V power supply. The drivers also integrate active-high and active-low enables for precise device control.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Active high and active low

The devices can be configured using the G and G logic inputs to select transmitter output. A logic high on the G pin or a logic low on the G pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.3.2 Operates from a 3.3-V Supply with up to 5-V Logic

While the transmitters operate from a single 3.3-V rail, the logic can operate off the same rail or another 5-V rail, making designs much more flexible to communicate to controllers.

8.3.3 High Speed Transmission

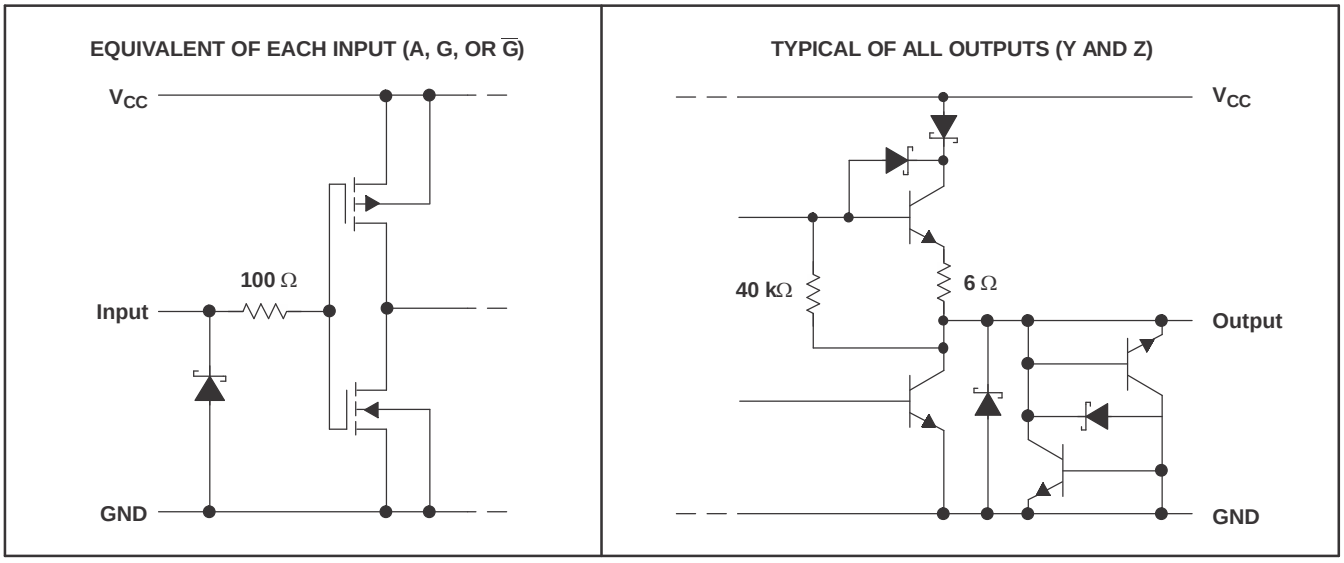
The AM26LV31C and AM26LV31I are optimized for balanced-bus transmission at switching rates up to 32 MHz. The devices are designed using Texas Instruments proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

8.4 Device Functional Modes

Table 1. Function Table(1)

INPUT A	ENABLES G	ENABLES $\overline{G}$	OUTPUTS Y	OUTPUTS Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)



ll resistor values are nominal.

Figure 6. Schematic (Each Driver)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. If termination is used, it can be placed at the end of the cable near the last receiver. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31C and AM26LV32C, respectively, were tested at room temperature with a 3.3-V supply voltage. The first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

9.2 Typical Application

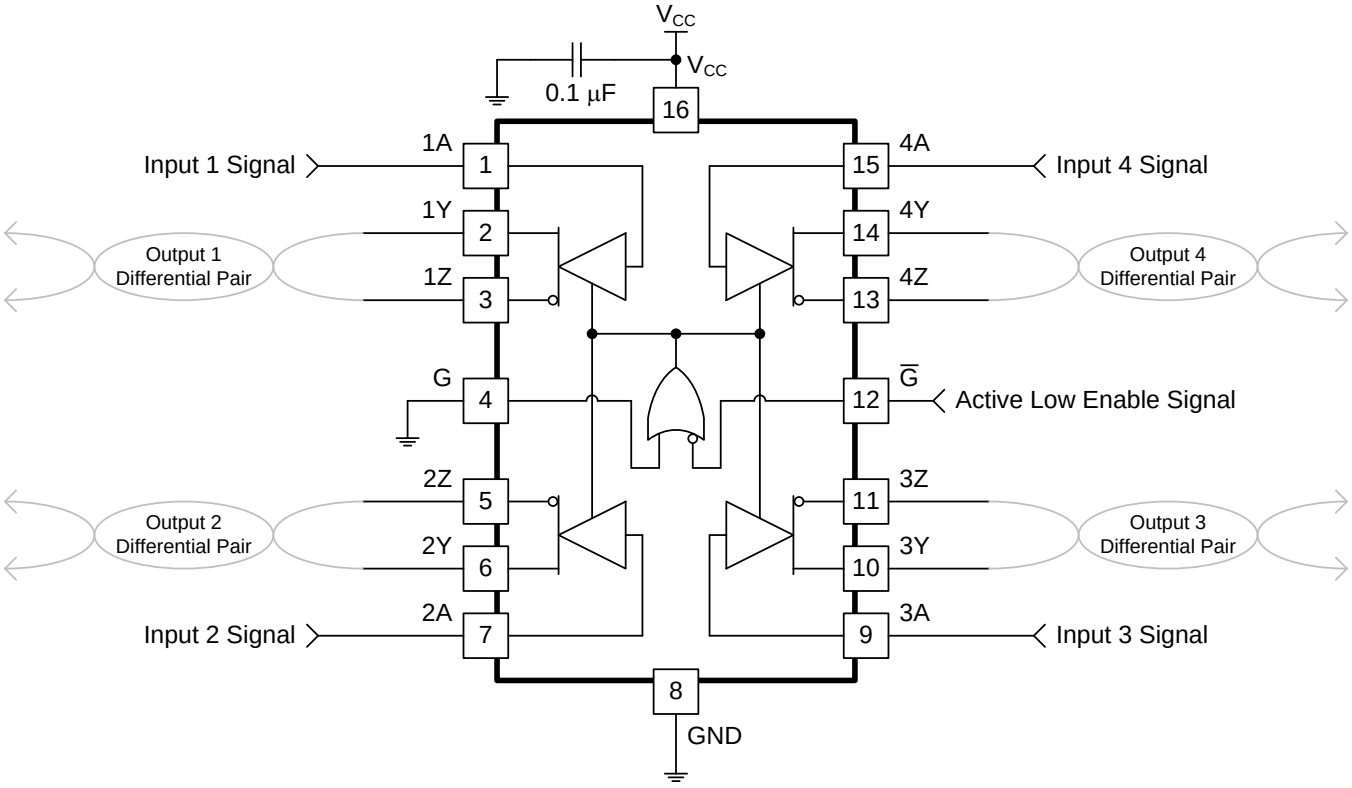


Figure 7. Differential Terminated Configuration With All Channels and Active Low Enable Used

Typical Application (continued)

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, RT, must be within 20% of the characteristic impedance, Zo, of the cable and can vary from about 80 Ω to 120 Ω.

This example requires the following:

- 3.3-V power source
- RS-485 bus operating at 32 MHz or less
- Connector that ensures the correct polarity for port pins

9.2.2 Detailed Design Procedure

Ensure values in Absolute Maximum Ratings are not exceeded. Supply voltage, V_{IH}, and V_{IL} must comply with Recommended Operating Conditions.

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see Failsafe in RS-485 data buses).

9.2.3 Application Curves

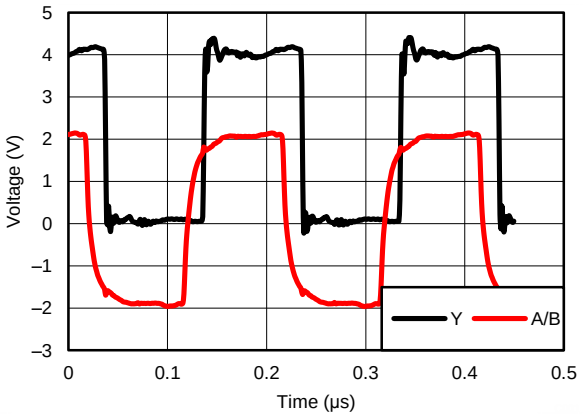


Figure 8. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

10 Power Supply Recommendations

Place a 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-μF ceramic bypass capacitors between supply pin and ground, placed as close to the device as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

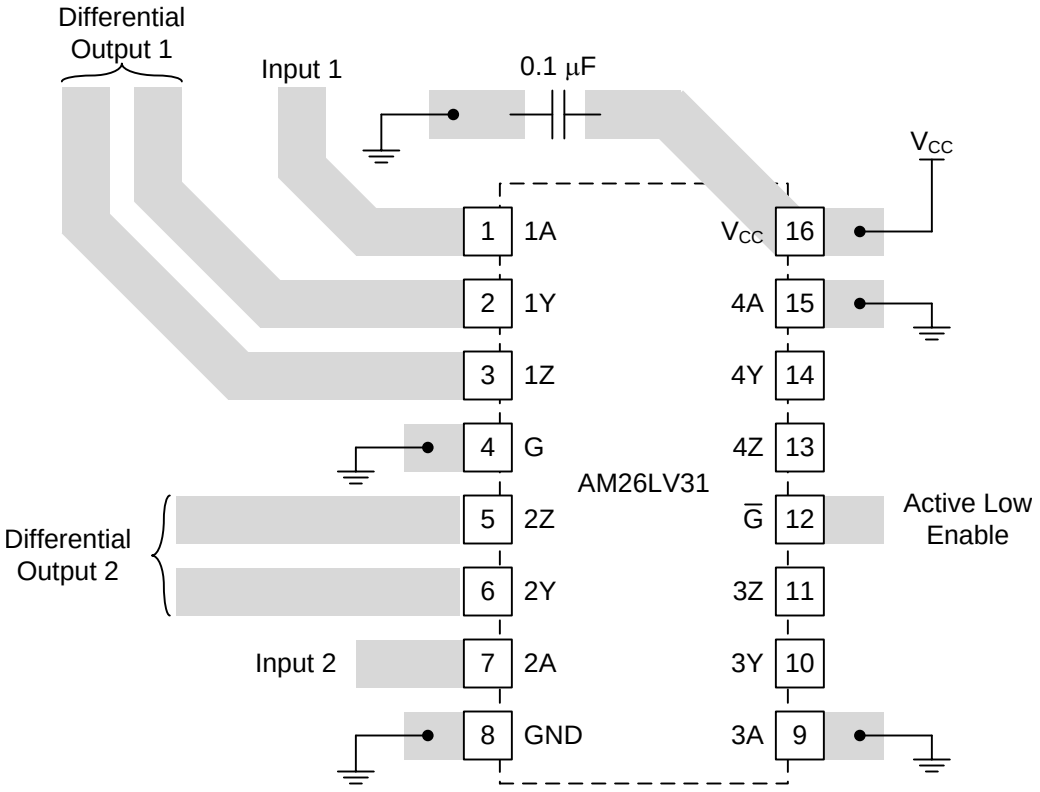


Figure 9. Trace Layout on PCB and Recommendations

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

LinIMPACT-C60, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV31CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	Samples
AM26LV31CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	Samples
AM26LV31CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	Samples
AM26LV31CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	AM26LV31C	Samples
AM26LV31CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	Samples
AM26LV31CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	Samples
AM26LV31CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26LV31	Samples
AM26LV31ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV31I	Samples
AM26LV31IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV31I	Samples
AM26LV31IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV31I	Samples
AM26LV31INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-45 to 85	26LV31I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

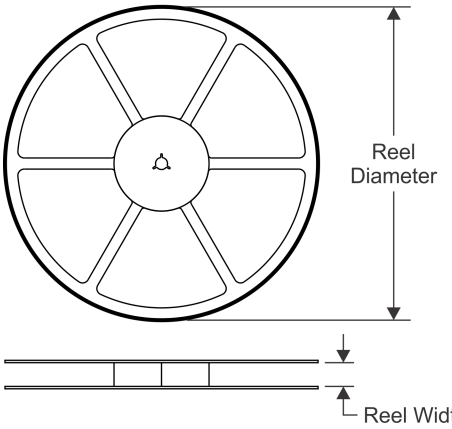
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

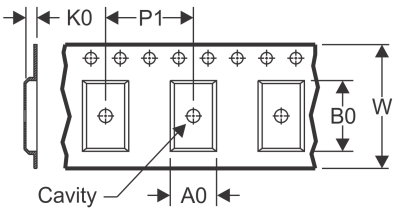
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

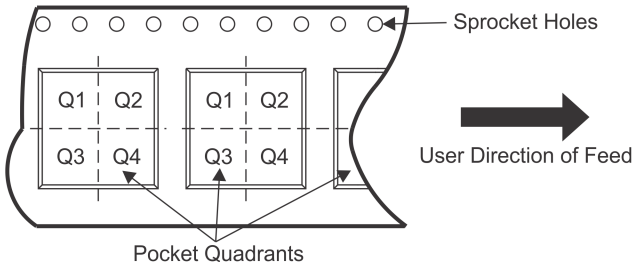


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

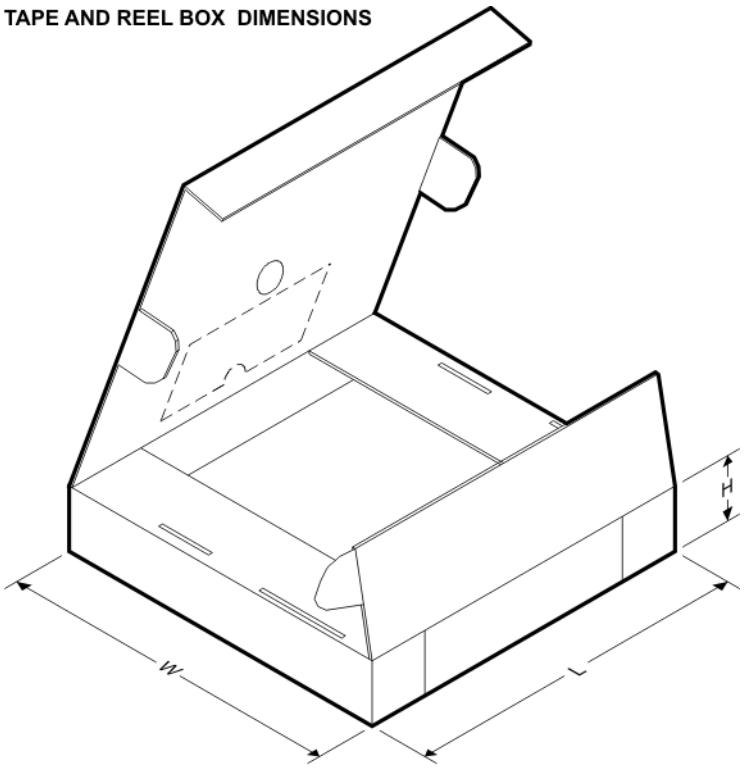
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31CDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

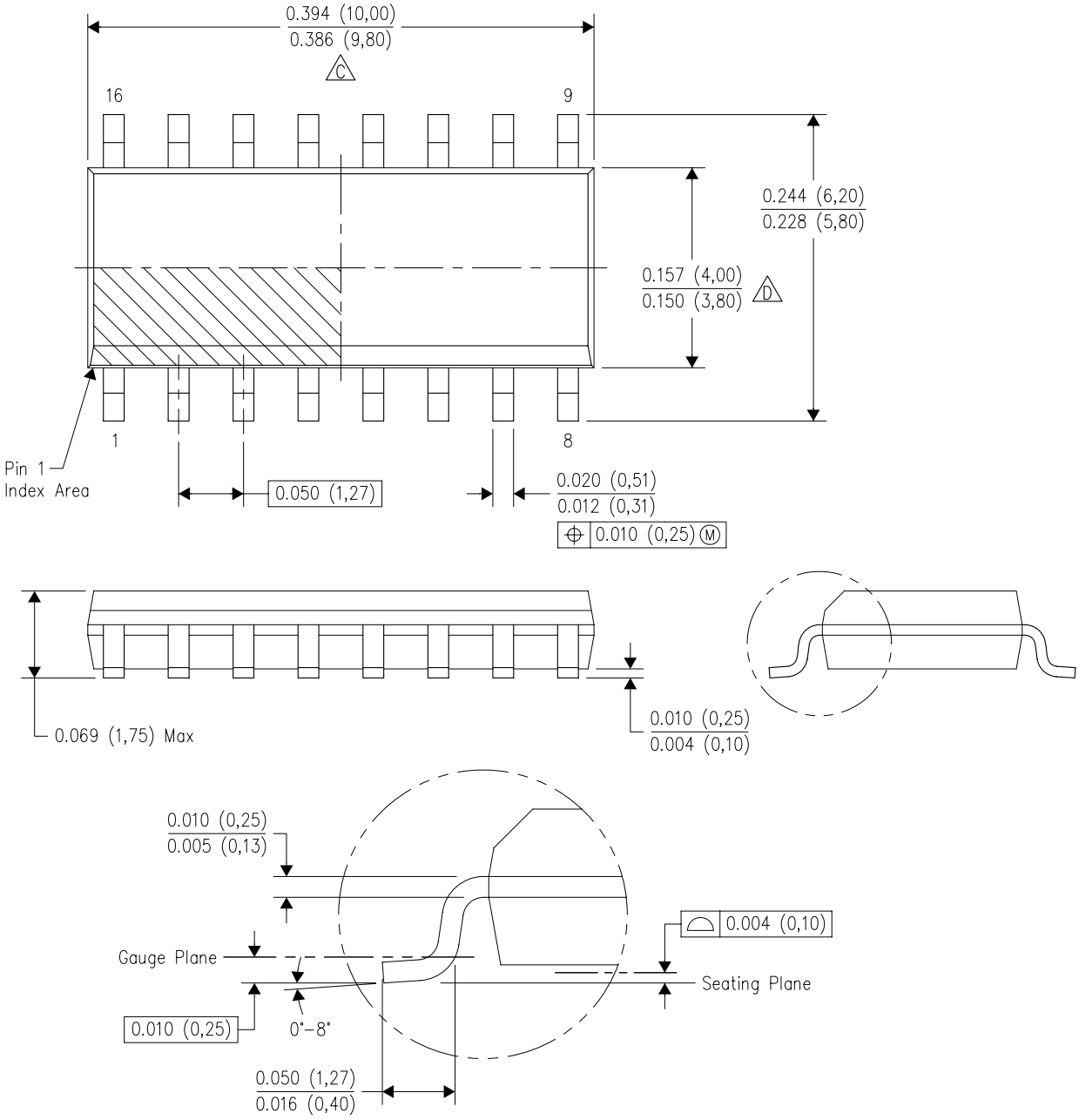
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

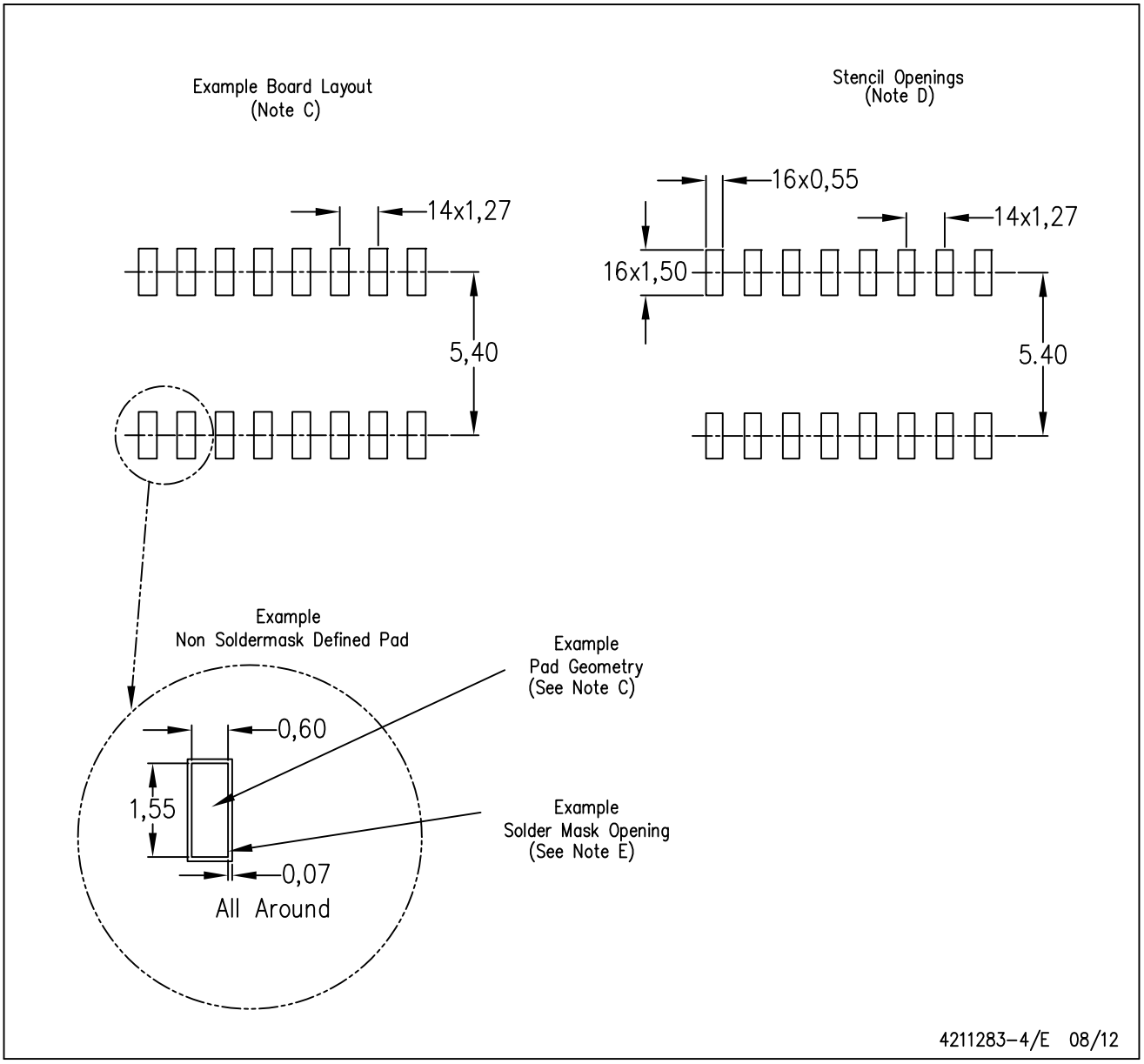
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31CDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26LV31CDR	SOIC	D	16	2500	364.0	364.0	27.0
AM26LV31CDRG4	SOIC	D	16	2500	333.2	345.9	28.6
AM26LV31IDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26LV31INSR	SO	NS	16	2000	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

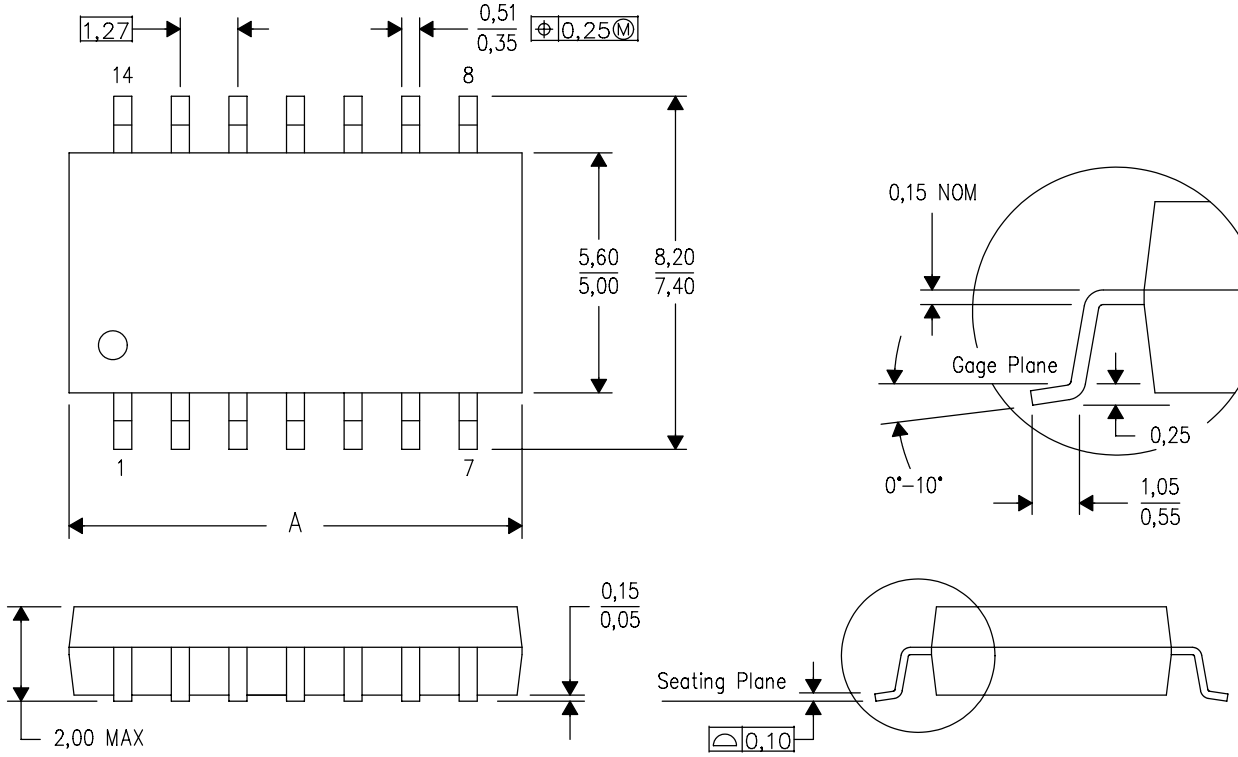


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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