CSD18535KTT 60 V N-Channel NexFET™ Power MOSFET

1 Features

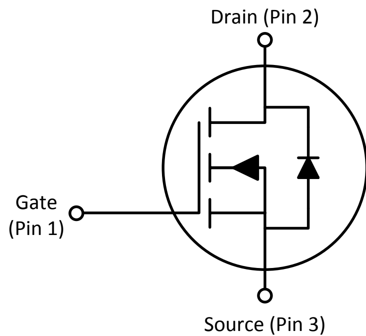
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- D^2PAK Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 60-V, 1.6-mΩ, D^2PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T_A = 25°C			TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage		60	V
Q_g	Gate Charge Total (10 V)		63	nC
Q_{gd}	Gate Charge Gate-to-Drain		10.4	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	2.3	mΩ
		V_{GS} = 10 V	1.6	mΩ
$V_{GS(th)}$	Threshold Voltage		1.9	V

Ordering Information[(1)]

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18535KTT	500	13-Inch Reel	D^2PAK Plastic Package	Tape & Reel
CSD18535KTTT	50			

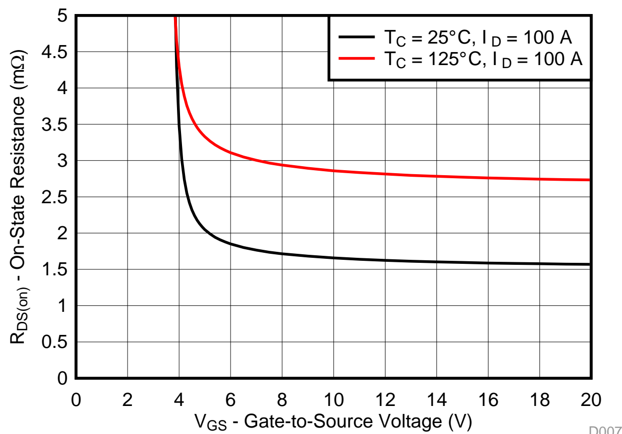
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

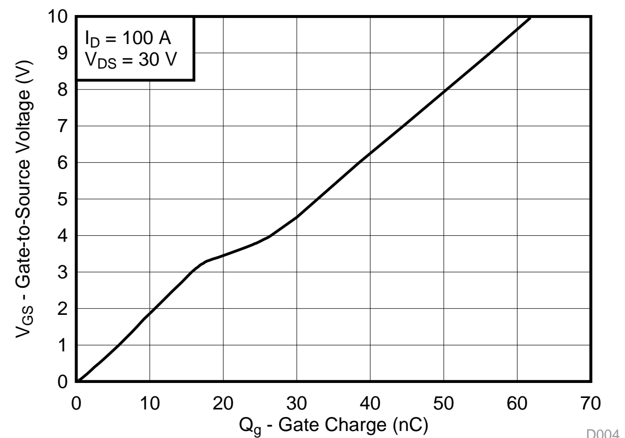
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	200	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	279	A
	Continuous Drain Current (Silicon limited), T_C = 100°C	197	A
I_{DM}	Pulsed Drain Current [(1)]	400	A
P_D	Power Dissipation	300	W
T_J, T_{stg}	Operating Junction and Storage Temperature	–55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 111 A, L = 0.1 mH, R_G = 25 Ω	616	mJ

(1) Max $R_{θJC}$ = 0.5°C/W, pulse duration ≤100 μs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Revision History 2
5 Specifications 3
5.1 Electrical Characteristics 3
5.2 Thermal Information 3
5.3 Typical MOSFET Characteristics 4
6 Device and Documentation Support 7
6.1 Community Resources 7
6.2 Trademarks 7
6.3 Electrostatic Discharge Caution 7
6.4 Glossary 7
7 Mechanical, Packaging, and Orderable Information 8
7.1 KTT Package Dimensions 8
7.2 Recommended PCB Pattern 9
7.3 Recommended Stencil Opening (0.125 mm Stencil Thickness) 9

4 Revision History

DATE	REVISION	NOTES
March 2016	*	Initial release.

Copyright © 2016, Texas Instruments Incorporated

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 48 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.4	1.9	2.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 100 A		2.3	2.9	mΩ
		V_{GS} = 10 V, I_D = 100 A		1.6	2.0	mΩ
g_{fs}	Transconductance	V_{DS} = 6 V, I_D = 100 A		263		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		5090	6620	pF
C_{oss}	Output capacitance			890	1150	pF
C_{rss}	Reverse transfer capacitance			24	31	pF
R_G	Series gate resistance			0.8	1.6	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 30 V, I_D = 100 A		63	81	nC
Q_{gd}	Gate charge gate-to-drain			10.4		nC
Q_{gs}	Gate charge gate-to-source			15.7		nC
$Q_{g(th)}$	Gate charge at V_{th}			9.4		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		140		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		9		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turn off delay time			19		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 30 V, I_F = 100 A, di/dt = 300 A/μs		214		nC
t_{rr}	Reverse recovery time			63		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-case thermal resistance			0.5	°C/W
$R_{θJA}$	Junction-to-ambient thermal resistance			62	°C/W

Copyright © 2016, Texas Instruments Incorporated

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

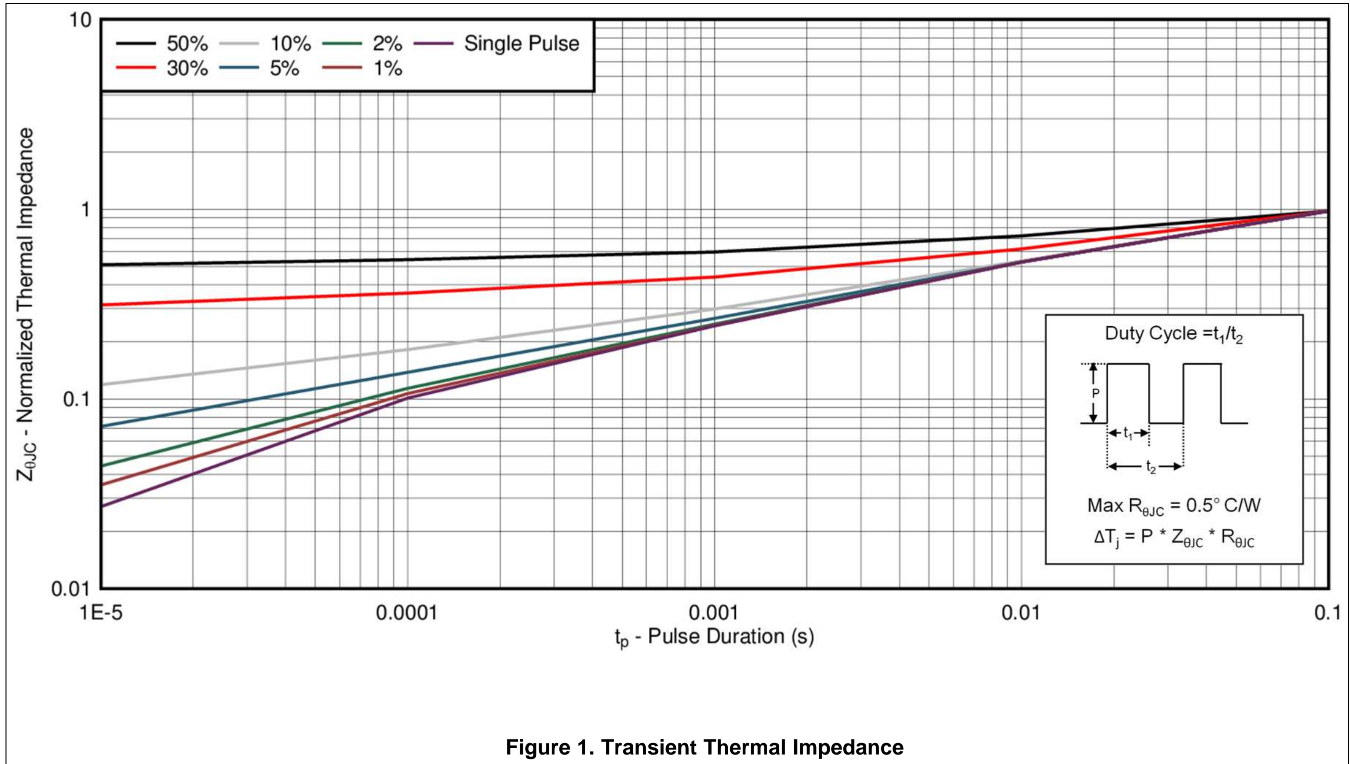


Figure 1. Transient Thermal Impedance

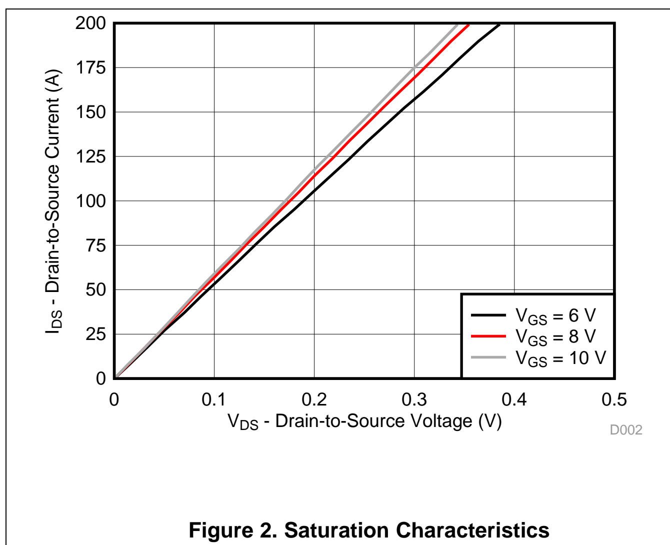


Figure 2. Saturation Characteristics

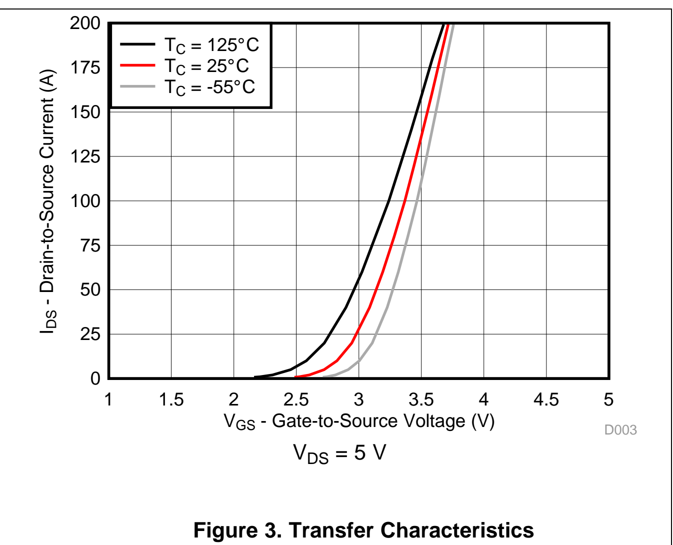


Figure 3. Transfer Characteristics

Copyright © 2016, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

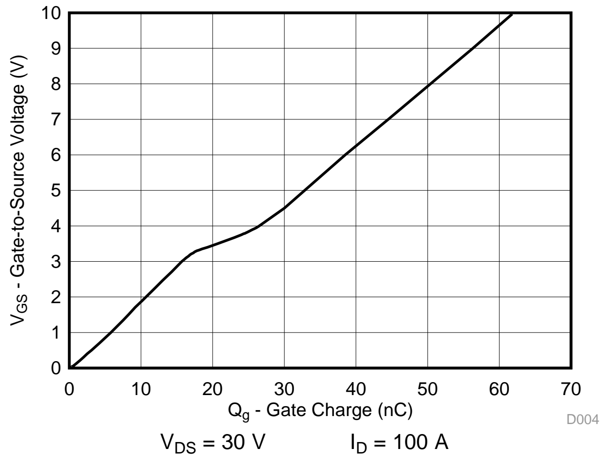


Figure 4. Gate Charge

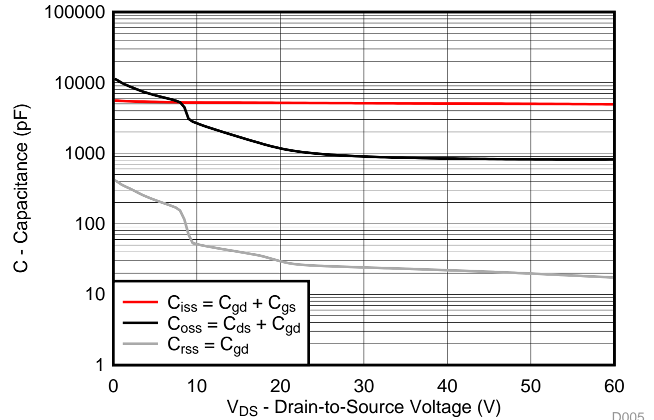


Figure 5. Capacitance

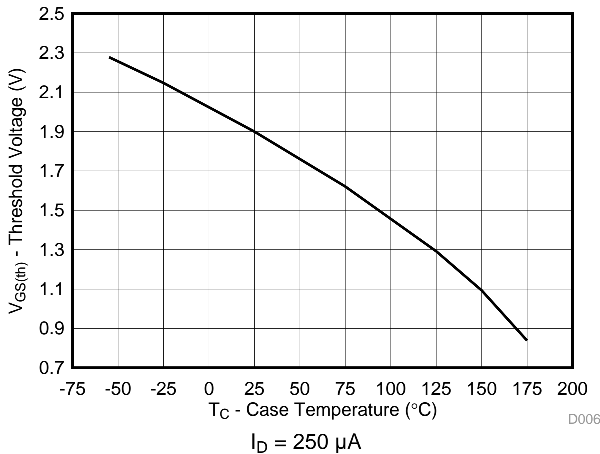


Figure 6. Threshold Voltage vs Temperature

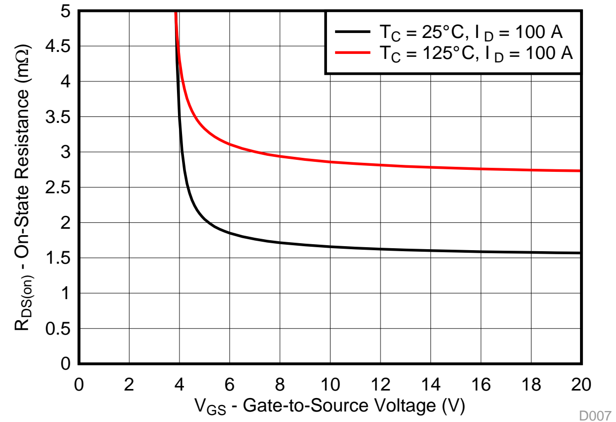


Figure 7. On-State Resistance vs Gate-to-Source Voltage

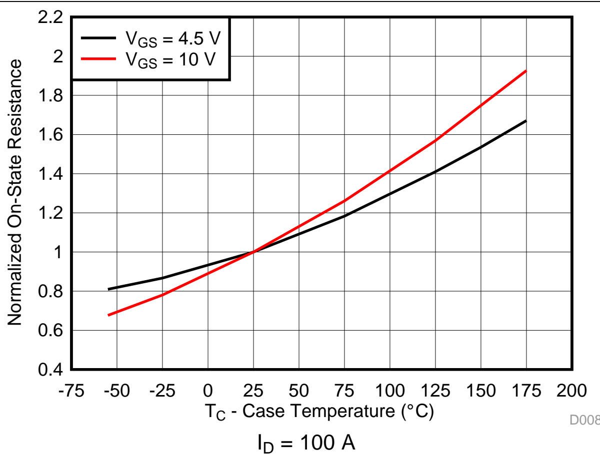


Figure 8. Normalized On-State Resistance vs Temperature

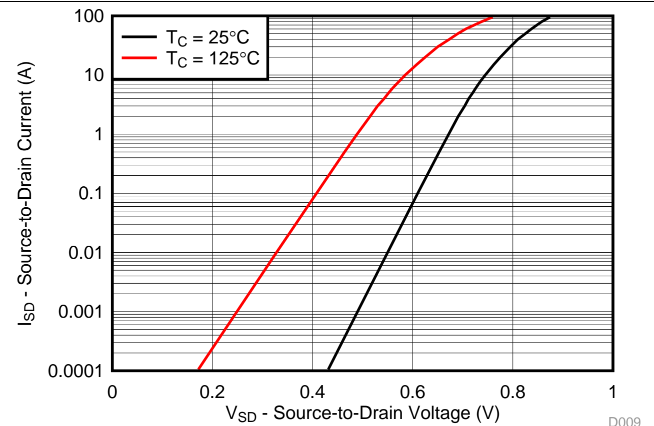
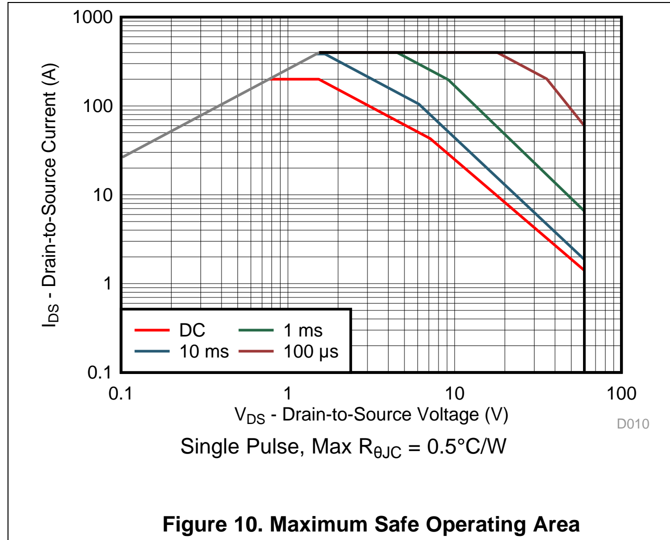


Figure 9. Typical Diode Forward Voltage

Copyright © 2016, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



Single Pulse, Max $R_{\theta JC}$ = 0.5°C/W

Figure 10. Maximum Safe Operating Area

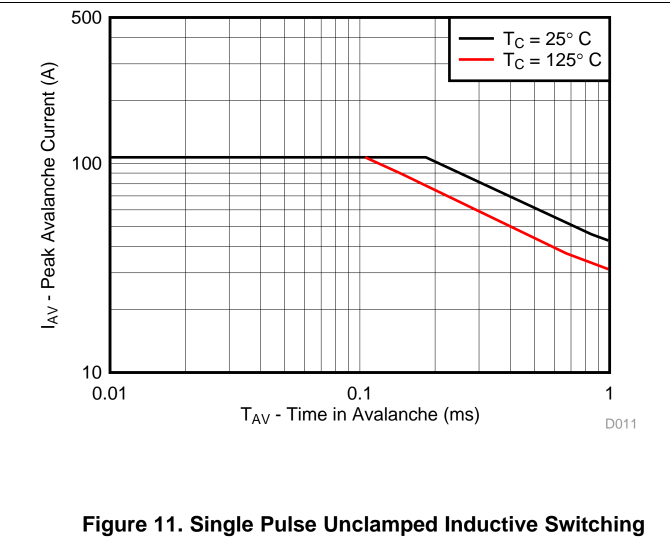


Figure 11. Single Pulse Unclamped Inductive Switching

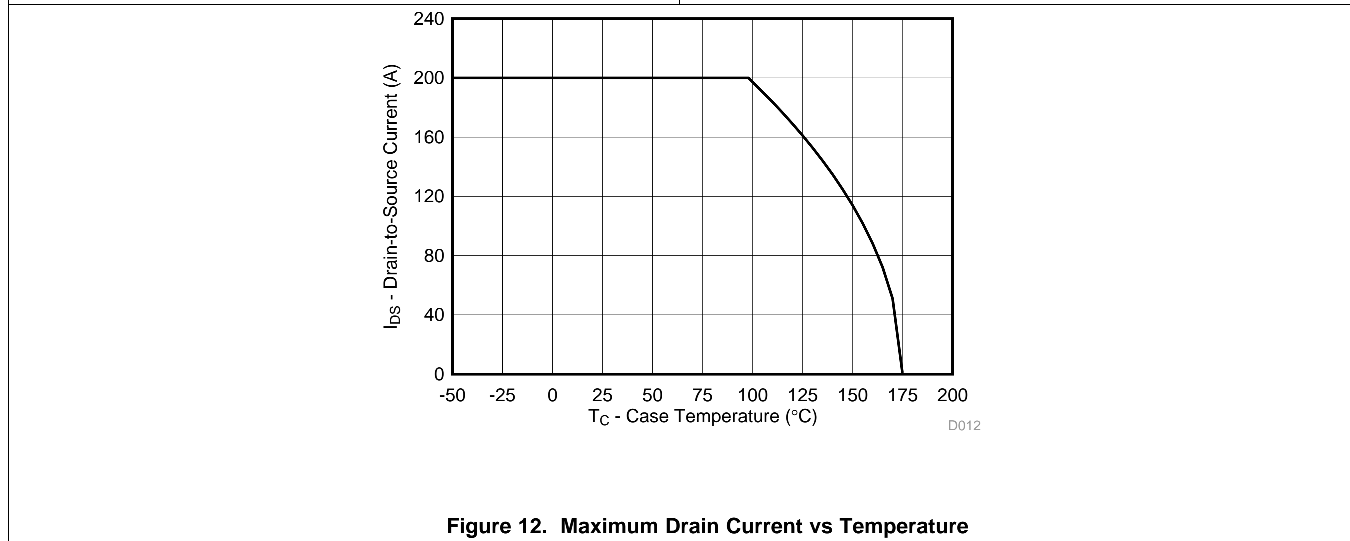


Figure 12. Maximum Drain Current vs Temperature

Copyright © 2016, Texas Instruments Incorporated

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — *TI Glossary*.

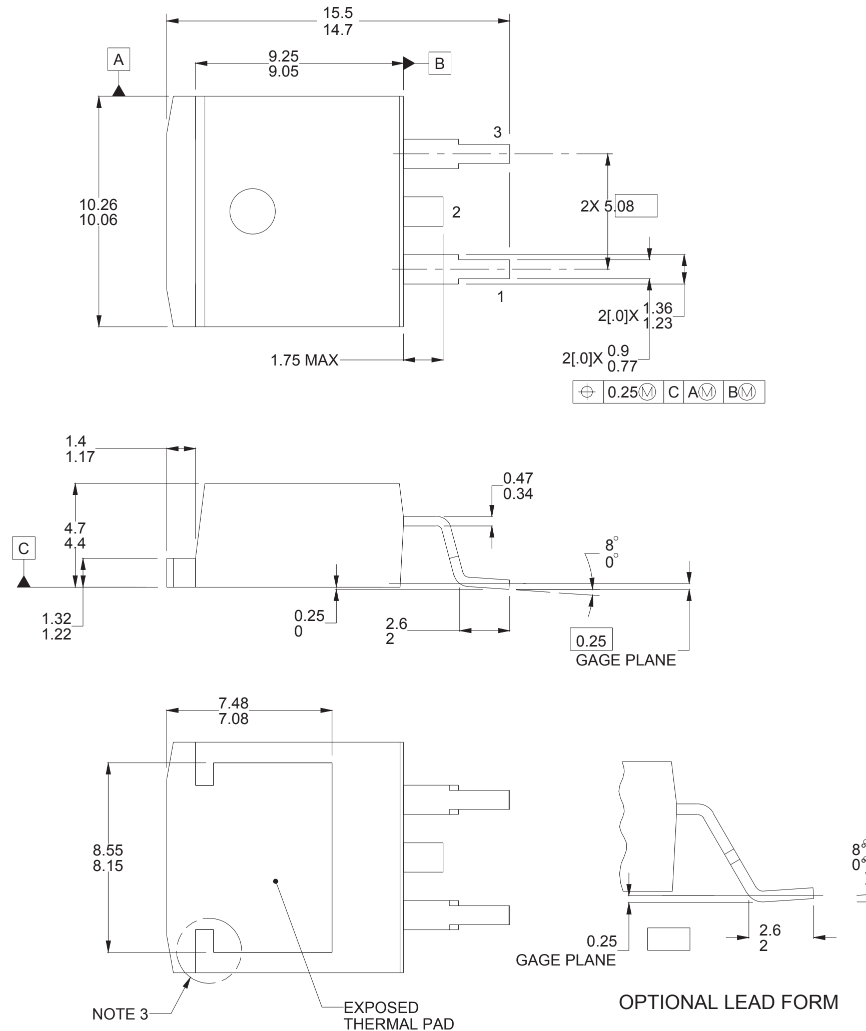
This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2016, Texas Instruments Incorporated

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KTT Package Dimensions



Notes:

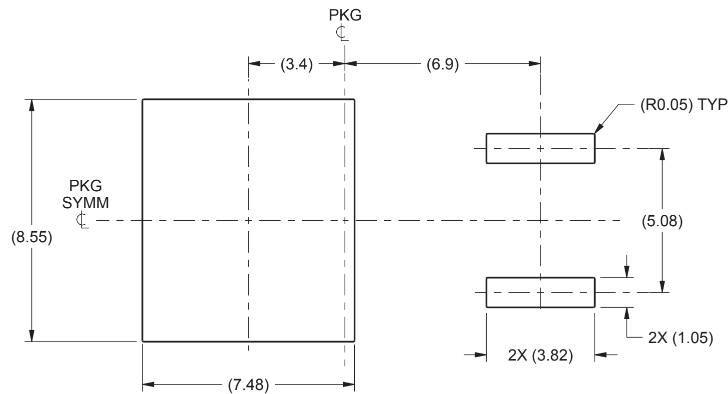
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.

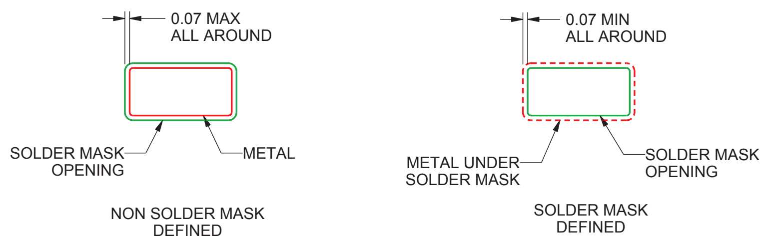
Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

Copyright © 2016, Texas Instruments Incorporated

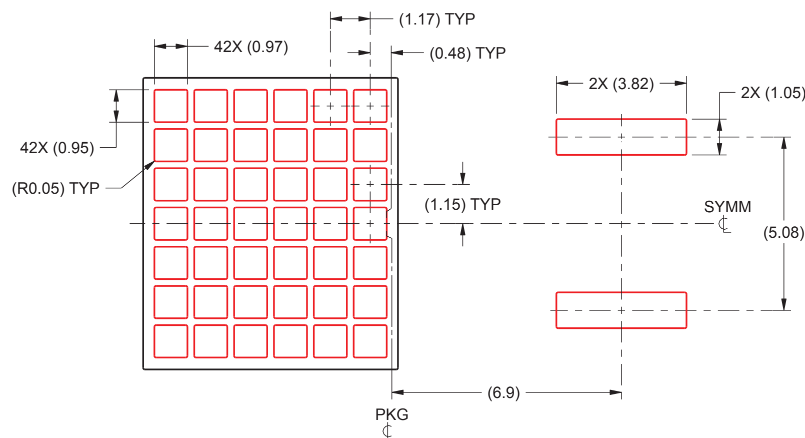
7.2 Recommended PCB Pattern





For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening (0.125 mm Stencil Thickness)



Notes:

1. This package is designed to be soldered to a thermal pad on the board. See application notes, *PowerPAD Thermally Enhanced Package* (SLMA002) and *PowerPAD Made Easy* (SLMA004) for more information.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
3. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18535KTT	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	-55 to 175	CSD18535KTT	Samples
CSD18535KTTT	ACTIVE	DDPAK/ TO-263	KTT	3	50	TBD	Call TI	Call TI	-55 to 175		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

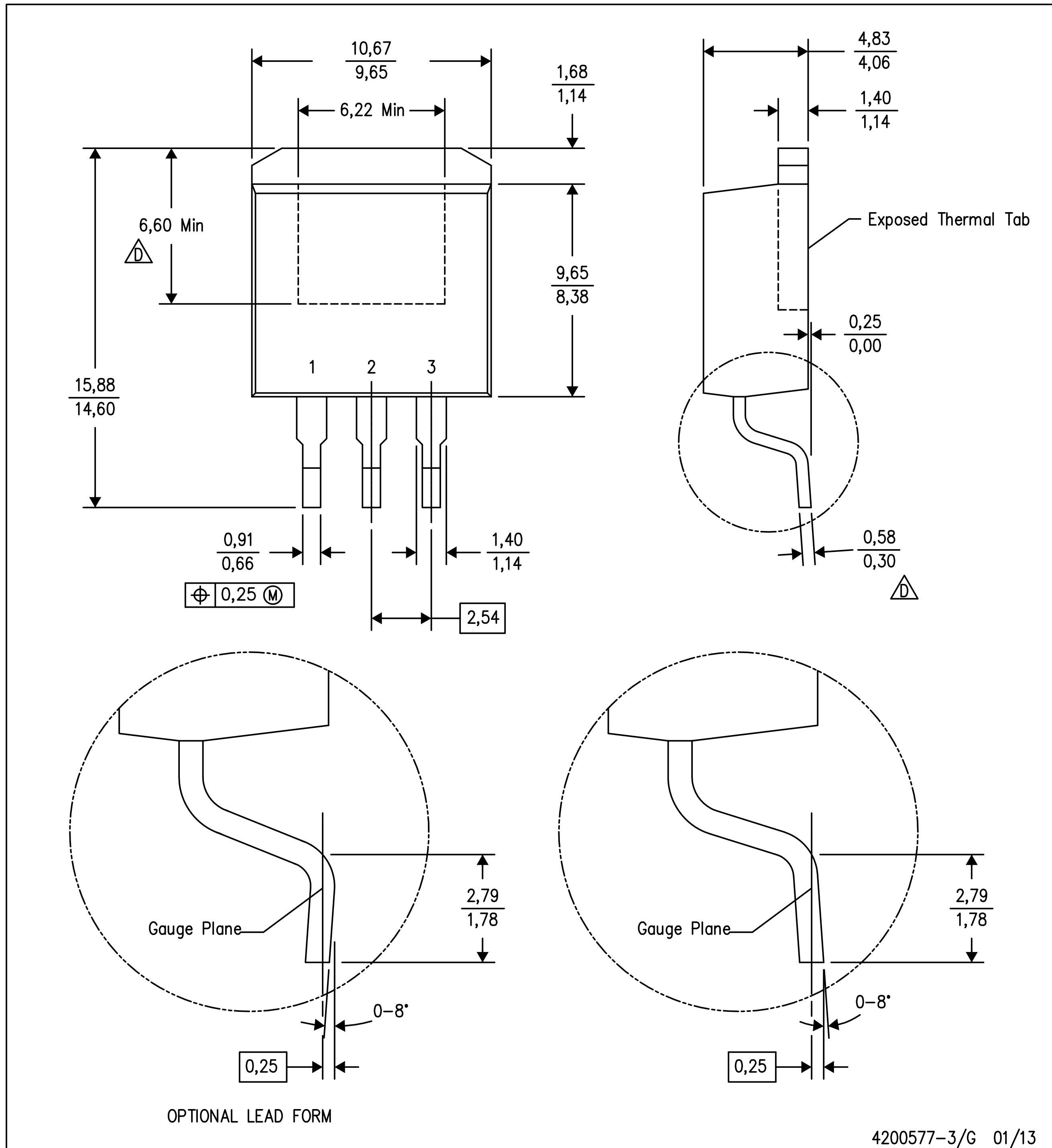
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.