P-Channel NexFET™ Power MOSFET

Check for Samples: CSD25301W1015

FEATURES

- **Ultra Low Qg and Qgd**
- **Small Footprint**
- **Low Profile 0.62mm Height**
- **Pb Free**
- **RoHS Compliant**
- **Halogen Free**
- **CSP 1 × 1.5 mm Wafer Level Package**

APPLICATIONS

- **Battery Management**
- **Load Switch**
- **Battery Protection**

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	–20		V
Q_g	Gate Charge Total (4.5V)	1.9		nC
Q_{gd}	Gate Charge Gate to Drain	0.4		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.5V	175	mΩ
		V_{GS} = –2.5V	80	mΩ
		V_{GS} = –4.5V	62	mΩ
$V_{GS(th)}$	Voltage Threshold	–0.75		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25301W1015	1 × 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

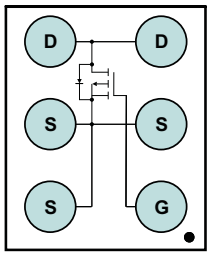
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Continuous Drain Current, T_C = 25°C(1)	–2.2	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	–8.8	A
P_D	Power Dissipation(1)	1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

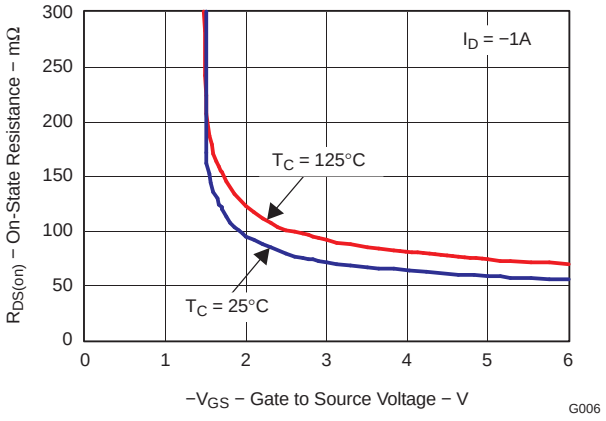
(1) $R_{\theta JA}$ = 85°C/W on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%

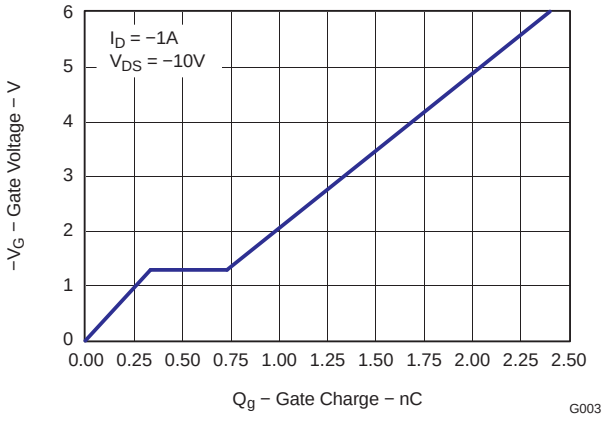
Top View



$R_{DS(ON)}$ vs V_{GS}



Gate Charge



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

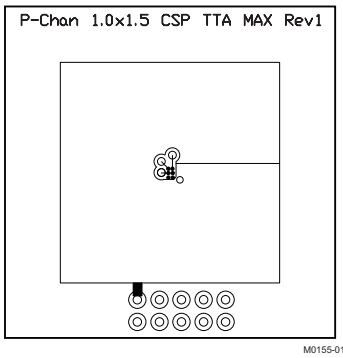
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = –250μA	–20			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = –16V			–1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = ±8V			–100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250μA	–0.4	–0.75	–1	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.5V, I_D = –1A		175	220	mΩ
		V_{GS} = –2.5V, I_D = –1A		80	100	mΩ
		V_{GS} = –4.5V, I_D = –1A		62	75	mΩ
g_{fs}	Transconductance	V_{DS} = –10V, I_D = –1A		5.8		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = –10V, f = 1MHz		210	270	pF
C_{OSS}	Output Capacitance			90	120	pF
C_{RSS}	Reverse Transfer Capacitance			30	40	pF
Q_g	Gate Charge Total (–4.5V)	V_{DS} = –10V, I_D = –1A		1.9	2.5	nC
Q_{gd}	Gate Charge Gate to Drain			0.4		nC
Q_{gs}	Gate Charge Gate to Source			0.35		nC
Qg(th)	Gate Charge at Vth			0.17		nC
Q_{OSS}	Output Charge	V_{DS} = –9.8V, V_{GS} = 0V		1.7		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10V, V_{GS} = –4.5V, I_D = –1A, R_G = 20Ω		4		ns
t_r	Rise Time			2		ns
$t_{d(off)}$	Turn Off Delay Time			29		ns
t_f	Fall Time			12		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = –1A, V_{GS} = 0V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{dd}= –9.8V, I_F = –1A, di/dt = 200A/μs		0.9		nC
t_{rr}	Reverse Recovery Time	V_{dd}= –9.8V, I_F = –1A, di/dt = 200A/μs		8.2		ns

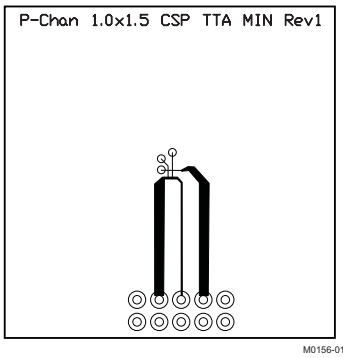
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			270	°C/W
	Thermal Resistance Junction to Ambient (1 in^2 Cu area)			105	°C/W



Max $R_{\theta JA}$ = 105°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 270°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

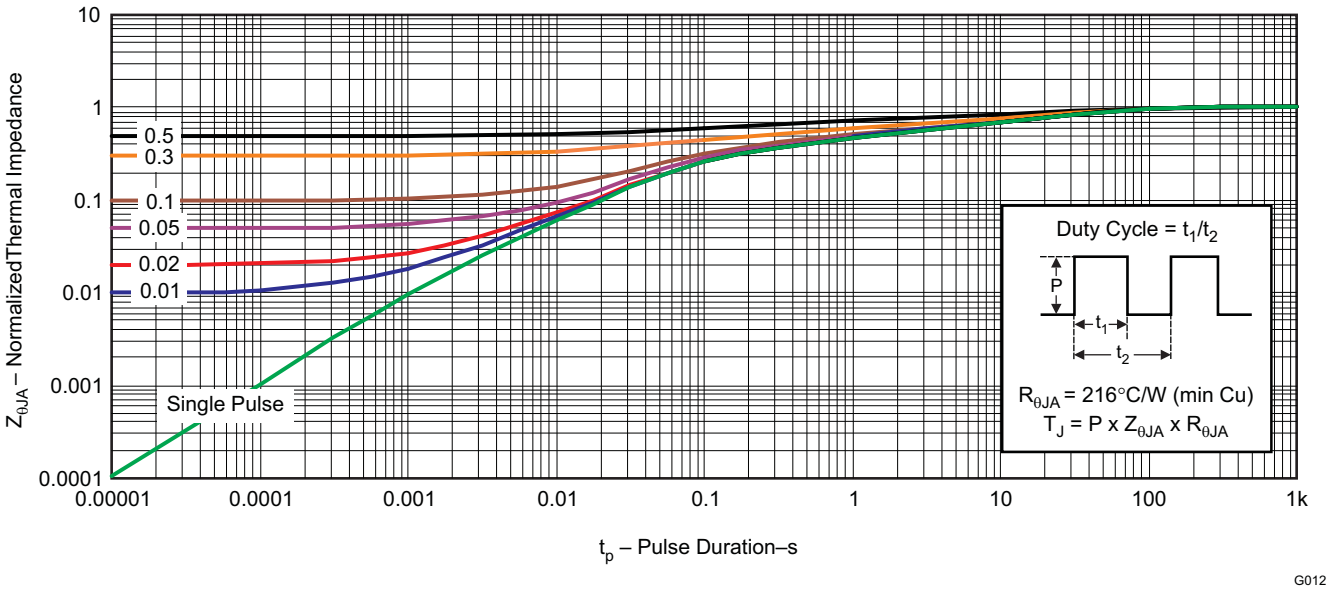


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

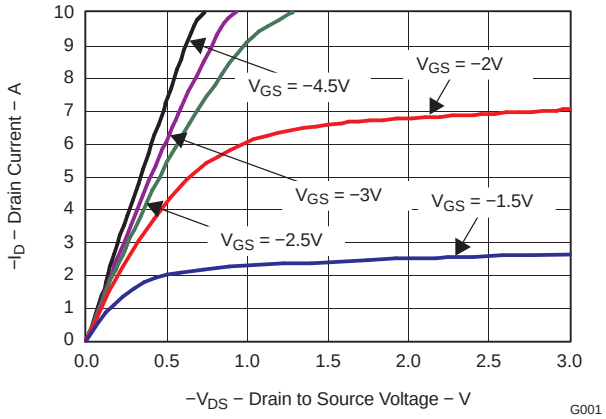


Figure 2. Saturation Characteristics

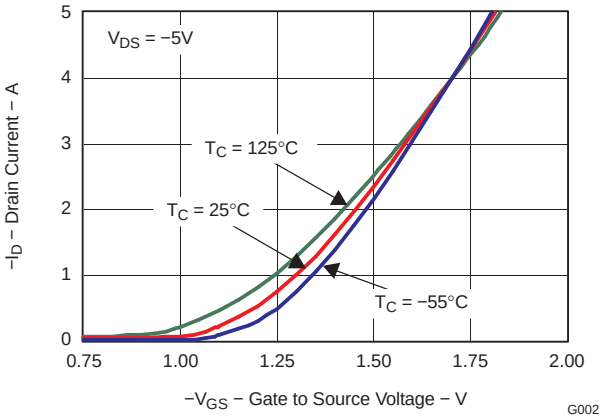


Figure 3. Transfer Characteristics

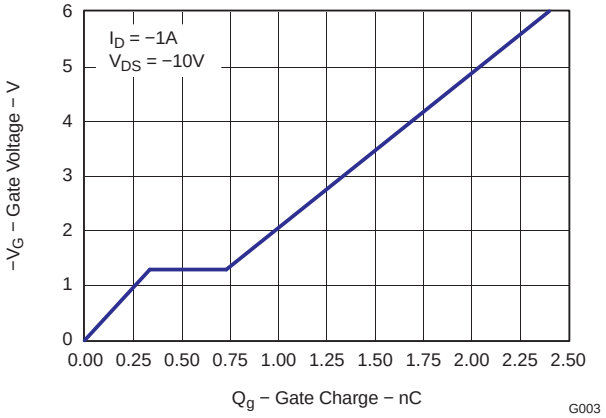


Figure 4. Gate Charge

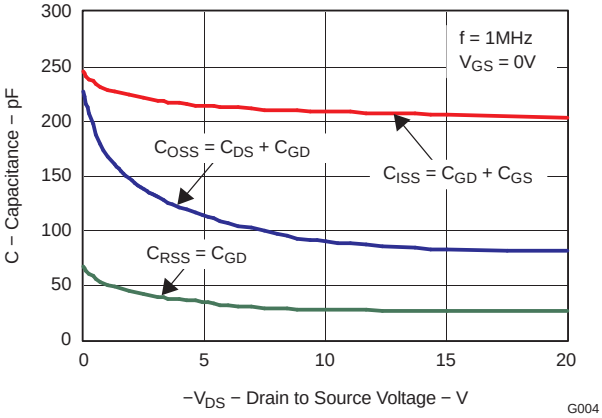


Figure 5. Capacitance

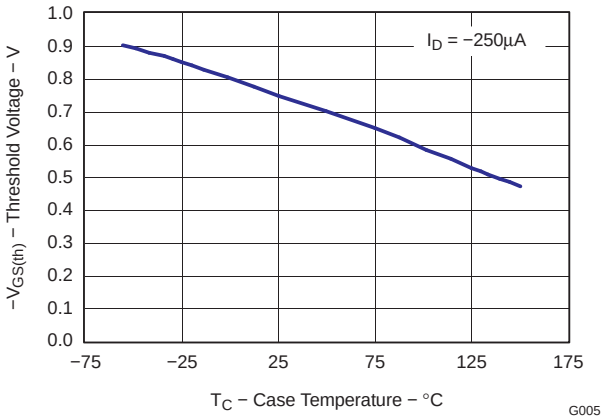


Figure 6. Threshold Voltage vs. Temperature

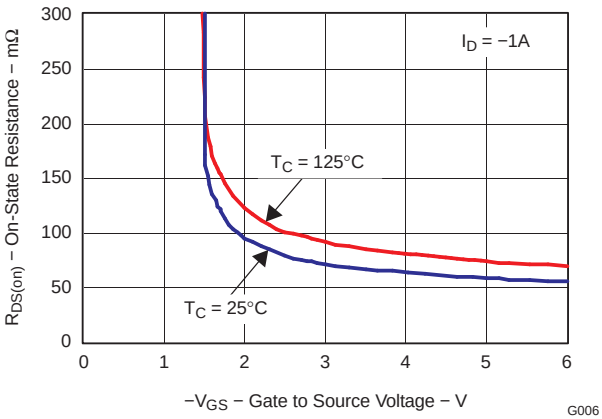


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

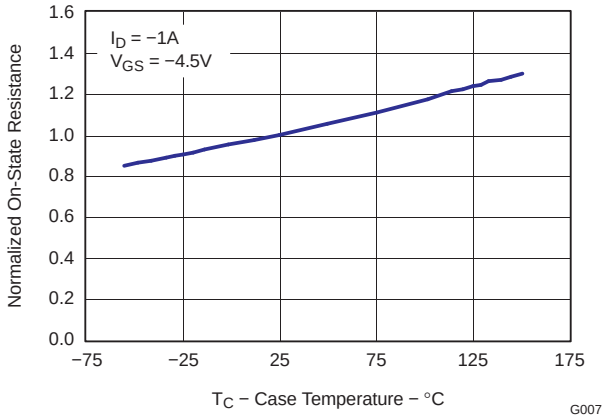


Figure 8. On Resistance vs. Temperature

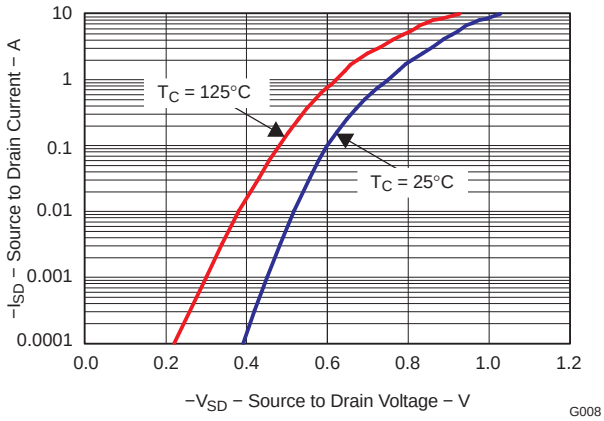


Figure 9. Typical Diode Forward Voltage

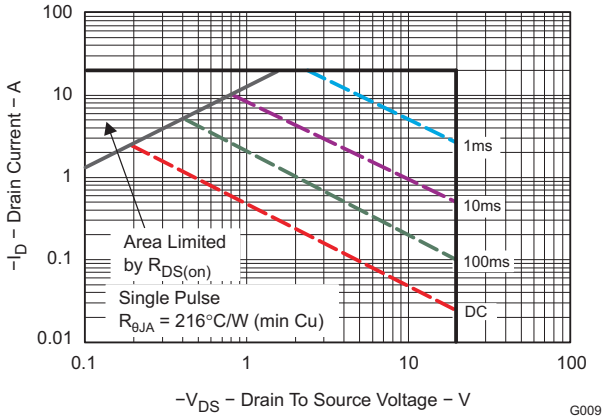


Figure 10. Maximum Safe Operating Area

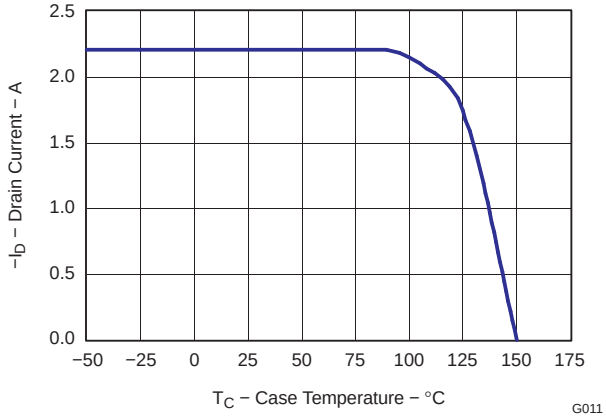
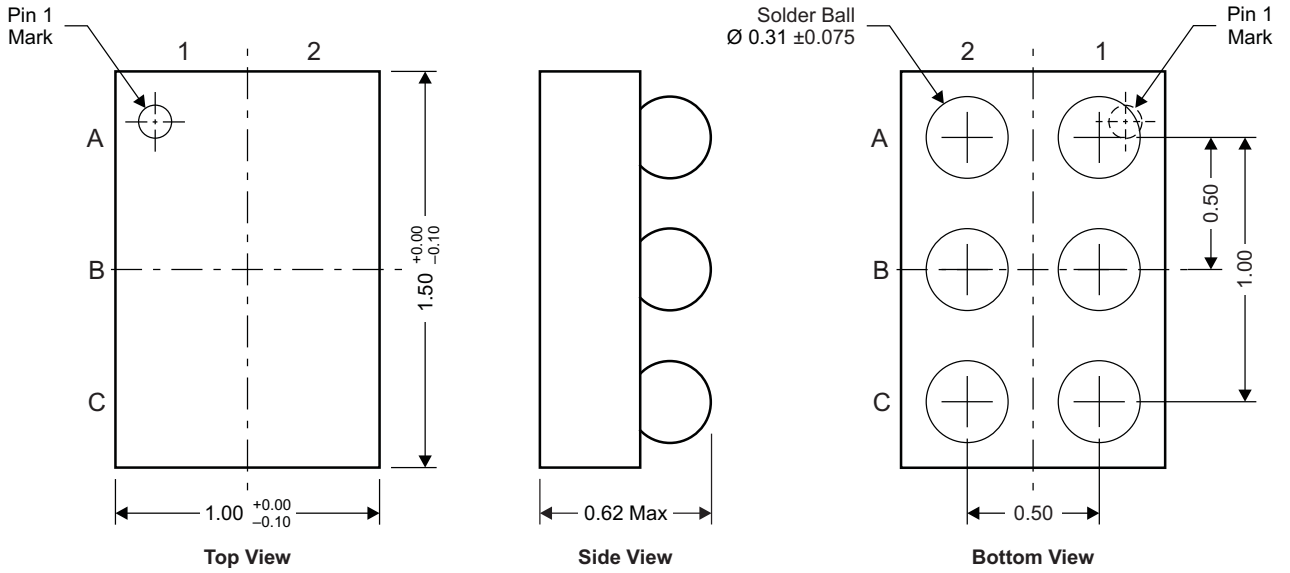
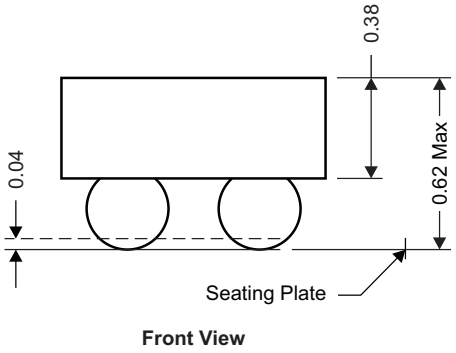


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD25301W1015 Package Dimensions





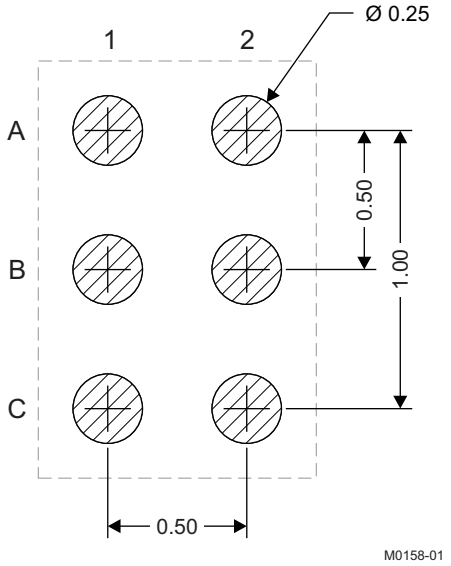
M0157-01

NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

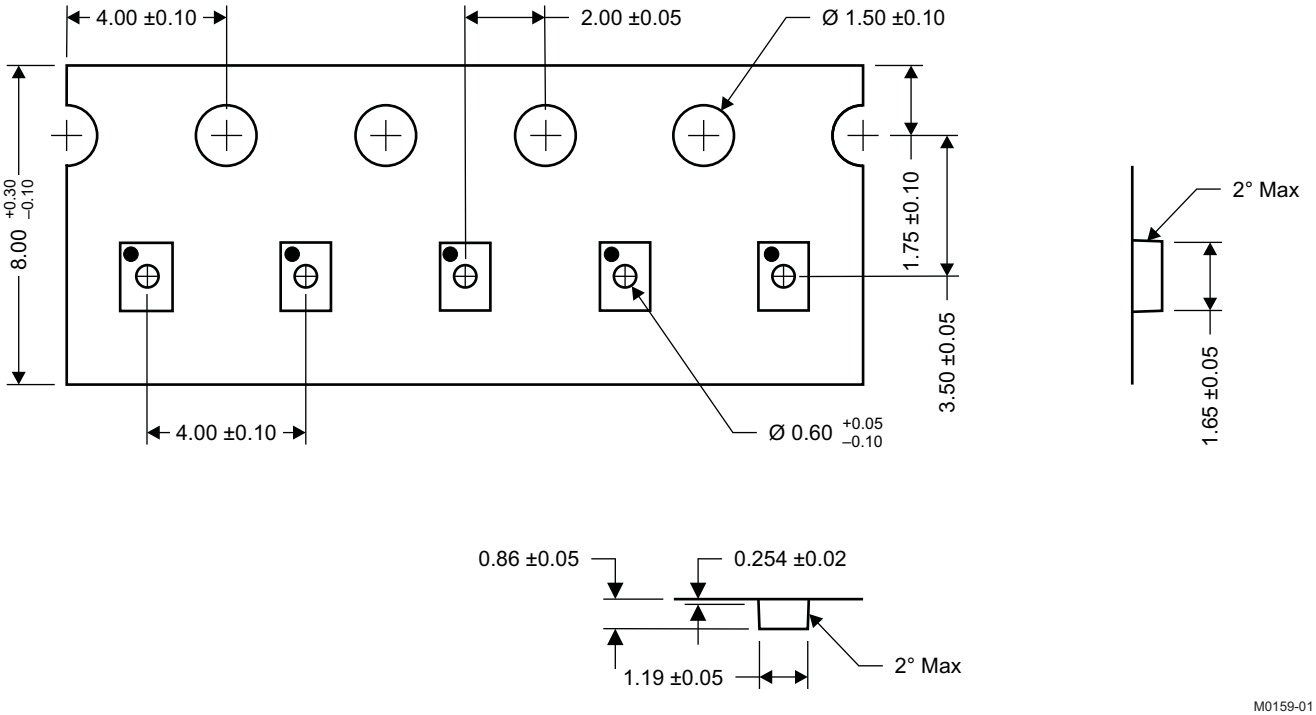
POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• Replaced incorrect label: $R_{\theta JC}$ with $R_{\theta JA}$ in the THERMAL CHARACTERISTICS table.	2

Changes from Revision A (August 2010) to Revision B	Page
• Deleted the Package Marking Information section	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25301W1015	OBSOLETE	DSBGA	YZC	6		Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	25301	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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