TEXAS INSTRUMENTS

LM3671, LM3671-Q1

SNVS294S – NOVEMBER 2004 – REVISED MAY 2016

LM3671/-Q1 2-MHz, 600-mA Step-Down DC-DC Converter

1 Features

- LM3671-Q1 is Qualified for Automotive Applications
- AEC Q100-Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
- 16-µA Typical Quiescent Current
- 600-mA Maximum Load Capability
- 2-MHz PWM Fixed Switching Frequency (Typical)
- Automatic PFM-PWM Mode Switching
- Internal Synchronous Rectification for High Efficiency
- Internal Soft Start
- 0.01-µA Typical Shutdown Current
- Operates from a Single Li-Ion Cell Battery
- Only Three Tiny Surface-Mount External Components Required (One Inductor, Two Ceramic Capacitors)
- Current Overload and Thermal Shutdown Protection
- Available in Fixed Output Voltages and Adjustable Version

2 Applications

- Mobile Phones
- PDAs
- MP3 Players
- W-LAN
- Portable Instruments
- Digital Still Cameras
- Portable Hard Disk Drives
- Automotive
- Portable Medical Equipment
- Handheld Transaction Terminals
- Wireless Home-Automation Equipment

3 Description

The LM3671 step-down DC-DC converter is optimized for powering low voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.7 V to 5.5 V. It provides up to 600-mA load current, over the entire input voltage range. There are several different fixed voltage output options available as well as an adjustable output voltage version range from 1.1 V to 3.3 V.

The device offers superior features and performance for mobile phones and similar portable systems. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During PWM mode, the device operates at a fixed-frequency of 2 MHz (typical). Hysteretic PFM mode extends the battery life by reducing the quiescent current to 16 µA (typical) during light load and standby operation. Internal synchronous rectification provides high efficiency during PWM mode operation. In shutdown mode, the device turns off and reduces battery consumption to 0.01 µA (typical).

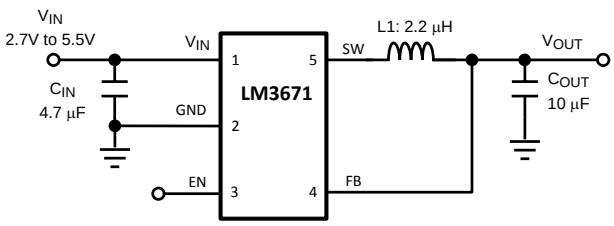
A high-switching frequency of 2 MHz (typical) allows use of tiny surface-mount components. Only three external surface-mount components, an inductor, and two ceramic capacitors, are required.

Device Information(1)

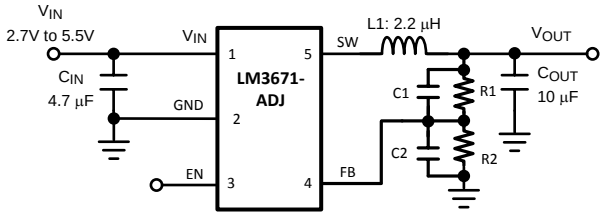
PART NUMBER	PACKAGE	BODY SIZE
LM3671	USON (6)	2.00 mm × 2.00 mm (NOM)
LM3671 LM3671-Q1	SOT-23 (5)	2.90 mm × 1.60 mm (NOM)
	DSBGA (5)	1.413 mm × 1.083 mm (MAX)

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit: Fixed-Voltage



Typical Application Circuit: ADJ



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (November 2014) to Revision S — **Page**

- Added top nav icon for TI Design ... 1
- Added several new "*Applications*" ... 1
- moved storage temperature to *Abs Max* table ... 4
- Changed *Handling Ratings* to *ESD Ratings* ... 4
- Changed $R_{\theta JA}$ for USON from 165°C/W to 174.7°C/W; for SOT-23 from 130°C/W to 165.7°C/W, and for DSBGA from 85°C/W to 181.0°C/W; added additional thermal values ... 5
- Changed $R_{\theta JA}$ values in *Dissipation Ratings* table ... 5

Changes from Revision Q (November 2013) to Revision R — **Page**

- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section ... 1

Changes from Revision O (April 2013) to Revision P — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 22

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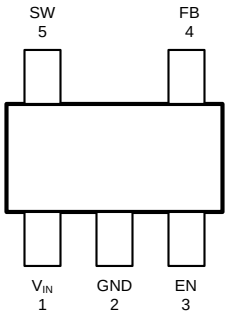
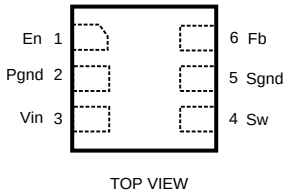
5 Pin Configuration and Functions

DBV Package
5 Pin SOT-23
Top View

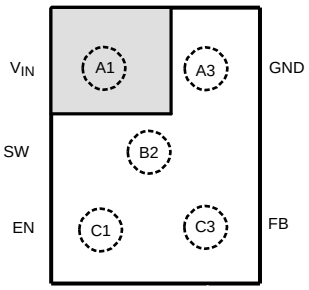


NKH Package
6-Pin USON

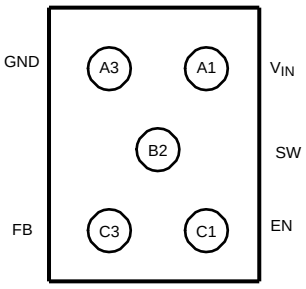


TOP VIEW

YZR Package
5-Pin DSBGA



Top View



Bottom View

Pin Functions

PIN				TYPE	DESCRIPTION
LM3671, LM3671-Q1		LM3671	NAME		
SOT-23	DSBGA	USON			
1	A1	3	V_{IN}	Power	Power supply input. Connect to the input filter capacitor (see *Input Capacitor Selection*).
2	A3	2	GND	Ground	Ground pin.
3	C1	1	EN	Digital	Enable pin. The device is in shutdown mode when voltage to this pin is < 0.4 V and enabled when > 1 V. Do not leave this pin floating.
4	C3	6	FB	Analog	Feedback analog input. Connect directly to the output filter capacitor for fixed voltage versions. For adjustable version external resistor dividers are required (see *Typical Application: ADJ Version*). The internal resistor dividers are disabled for the adjustable version.
5	B2	4	SW	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
—	—	5	S_{GND}	Ground	Signal ground (feedback ground).

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
V_{IN} pin: voltage to GND	−0.2	6	V
FB, SW, EN pins	GND − 0.2	V_{IN} + 0.2	V
Continuous power dissipation(3)	Internally Limited		
Junction temperature, $T_{J\text{-}MAX}$		125	°C
Maximum lead temperature (soldering, 10 sec.)		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150°C (typical) and disengages at T_J= 130°C (typical).

6.2 ESD Ratings: LM3671

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		Machine model	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM3671-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except corner pins	±500	
			Corner pins (1, 3, 4, and 5): SOT-23	±750	
			Corner pins (A1, A3, C1, and C3): DSBGA	±750	
		Machine model		±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage(3)	2.7	5.5	V
Recommended load current	0	600	mA
Junction temperature, T_J	–40	125	°C
Ambient temperature, T_A(4)	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) The input voltage range recommended for ideal applications performance for the specified output voltages are given below: V_{IN} = 2.7 V to 4.5 V for 1.1 V ≤ V_{OUT} < 1.5 V_{IN} = 2.7 V to 5.5 V for 1.5 V ≤ V_{OUT} < 1.8 V_{IN} = (V_{OUT} + $V_{DROPOUT}$) to 5.5 V for 1.8 V ≤ V_{OUT} ≤ 3.3 V where $V_{DROPOUT}$ = I_{LOAD} × ($R_{DSON,\ PFET}$ + $R_{INDUCTOR}$).
(4) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX}$), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$) and the junction to ambient thermal resistance of the package ($R_{\theta JA}$) in the application, as given by the following equation: $T_{A\text{-}MAX}$ = $T_{J\text{-}MAX}$ − ($R_{\theta JA}$ × $P_{D\text{-}MAX}$). Refer to *Dissipation Ratings* for $P_{D\text{-}MAX}$ values at different ambient temperatures.

6.5 Thermal Information

THERMAL METRIC(1)		LM3671	LM3671 and LM3671-Q1		UNIT
		NKH (USON)	DBV (SOT-23)	YZR (DSBGA)	
		6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174.7	165.7	181.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.1	116.6	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	109.0	26.8	110.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	13.3	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	109.0	26.3	110.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Dissipation Ratings

$R_{\theta JA}$	T_A≤ 25°C POWER RATING	T_A= 60°C POWER RATING	T_A= 85°C POWER RATING
165.7°C/W (4 layer board) SOT-23	770 mW	500 mW	310 mW
181°C/W (4 layer board) 5-bump DSBGA	1179 mW	765 mW	470 mW
174.7°C/W (4 layer board) 6-pin USON	606 mW	394 mW	242 mW

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6.7 Electrical Characteristics

Unless otherwise noted, limits apply for for T_J = 25°C, and specifications apply to the LM3671MF/TL/LC with V_{IN} = EN = 3.6 V[1][2][3]

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	−40°C to 125°C, see[4]	2.7		5.5	V
V_{FB}	Feedback voltage (fixed) MF	PWM mode[5], −40°C to 125°C	−4%		4%	
	Feedback voltage (fixed) TL		−2.5%		2.5%	
	Feedback voltage (fixed) LC		−4%		4%	
	Feedback voltage (ADJ) MF[6]	PWM mode[5], −40°C to 125°C	−4%		4%	
	Feedback voltage (ADJ) TL		−2.5		2.5	
	Line regulation	2.7 V ≤ V_{IN} ≤ 5.5 V, I_O = 10 mA		0.031		%/V
	Load regulation	100 mA ≤ I_O ≤ 600 mA, V_{IN} = 3.6 V		0.0013		%/mA
V_{REF}	Internal reference voltage			0.5		V
I_{SHDN}	Shutdown supply current	EN = 0 V		0.01		µA
		EN = 0 V, −40°C to 125°C			1	
I_Q	DC bias current into V_{IN}	No load, device is not switching (FB forced higher than programmed output voltage)		16		µA
		No load, device is not switching (FB forced higher than programmed output voltage), −40°C to 125°C			35	
$R_{DSON\ (P)}$	Pin-pin resistance for PFET	V_{IN} = V_{GS} = 3.6 V		380	500	mΩ
$R_{DSON\ (N)}$	Pin-pin resistance for NFET	V_{IN} = V_{GS}= 3.6 V		250	400	mΩ
I_{LIM}	Switch peak current limit	Open loop[7]		1020		mA
		Open loop[7], −40°C to 125°C	830		1150	
V_{IH}	Logic high input	−40°C to 125°C	1			V
V_{IL}	Logic low input	−40°C to 125°C			0.4	V
I_{EN}	Enable (EN) input current			0.01		µA
		−40°C to 125°C			1	
f_{OSC}	Internal oscillator frequency	PWM Mode[5]		2		MHz
		PWM Mode[5], −40°C to 125°C	1.6		2.6	

(1) Minimum (MIN) and maximum (MAX) limits are specified by design, test or statistical analysis. Typical (TYP) numbers are not specified, but do represent the most likely norm.
(2) The parameters in the electrical characteristic table are tested at V_{IN} = 3.6 V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150°C (typical) and disengages at T_J= 130°C (typical).
(4) The input voltage range recommended for ideal applications performance for the specified output voltages are given below: V_{IN} = 2.7 V to 4.5 V for 1.1 V ≤ V_{OUT} < 1.5 V_{IN} = 2.7 V to 5.5 V for 1.5 V ≤ V_{OUT} < 1.8 V_{IN} = (V_{OUT} + $V_{DROPOUT}$) to 5.5 V for 1.8 V ≤ V_{OUT} ≤ 3.3 V where $V_{DROPOUT}$ = I_{LOAD} × ($R_{DSON,\ PFET}$ + $R_{INDUCTOR}$).
(5) Test condition: for V_{OUT} less than 2.5 V, V_{IN} = 3.6 V; for V_{OUT} greater than or equal to 2.5 V, V_{IN} = V_{OUT} + 1 V.
(6) ADJ version is configured to 1.5 V output. For ADJ output version: V_{IN} = 2.7 V to 4.5 V for 0.9 V ≤ V_{OUT} < 1.1 V_{IN} = 2.7 V to 5.5 V for 1.1 V ≤ V_{OUT} < 3.3 V
(7) Refer to *Typical Characteristics* for closed-loop data and its variation with regards to supply voltage and temperature. *Electrical Characteristics* reflects open-loop data (FB = 0 V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

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6.8 Typical Characteristics

LM3671MF/TL/LC, circuit of *Figure 32*, V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C, unless otherwise noted.

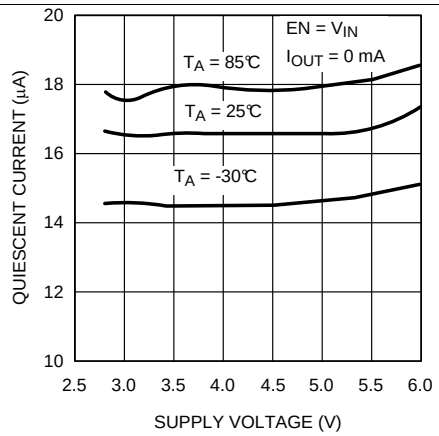

Figure 1. Quiescent Supply Current vs Supply Voltage

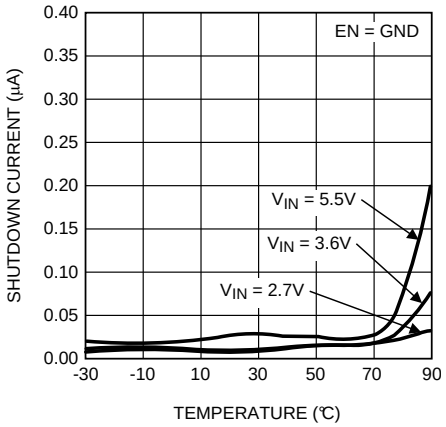

Figure 2. Shutdown Current vs Temp

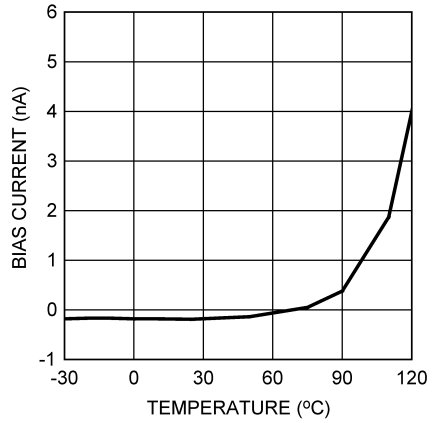

Figure 3. Feedback Bias Current vs Temperature

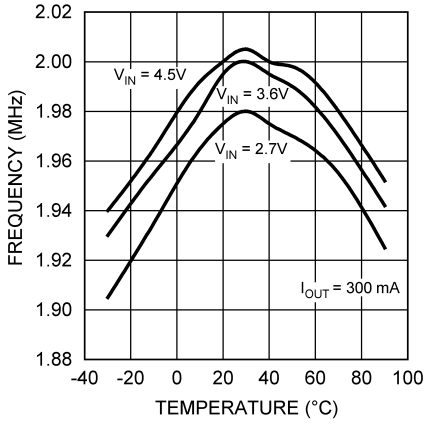

Figure 4. Switching Frequency vs Temperature

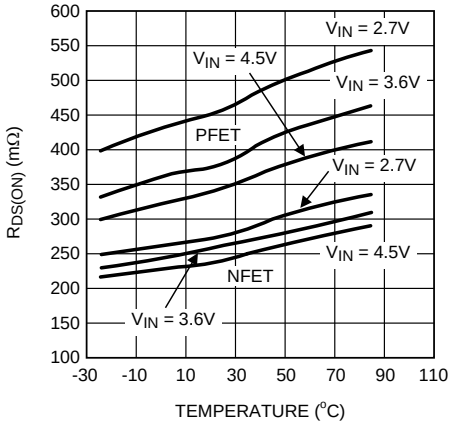

Figure 5. $R_{DS(ON)}$ vs. Temperature

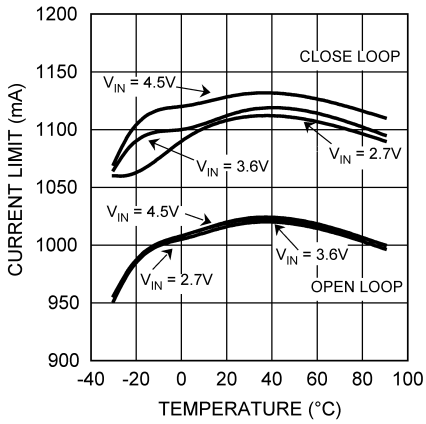

Figure 6. Open/Closed Loop Current Limit vs Temperature

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Typical Characteristics (continued)

LM3671MF/TL/LC, circuit of *Figure 32*, V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C, unless otherwise noted.

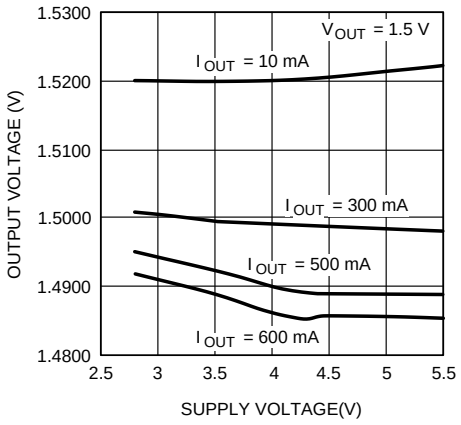

Figure 7. Output Voltage vs. Supply Voltage

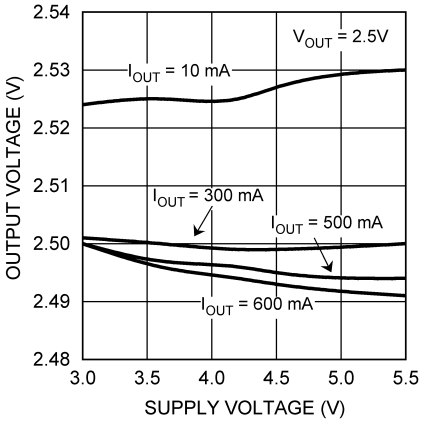

Figure 8. Output Voltage vs Supply Voltage

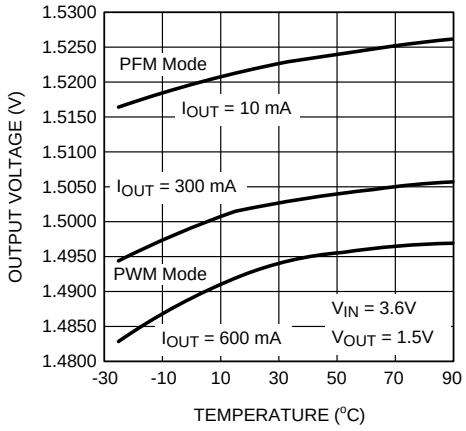

Figure 9. Output Voltage vs Temperature

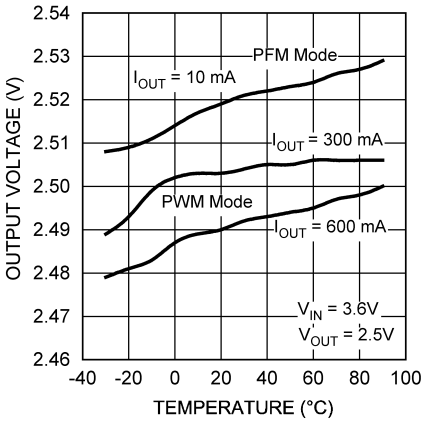

Figure 10. Output Voltage vs Temperature

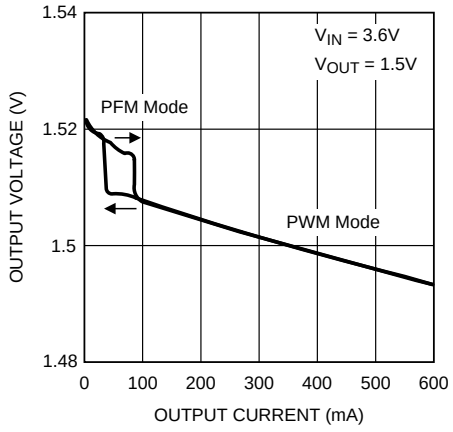

Figure 11. Output Voltage vs Output Current

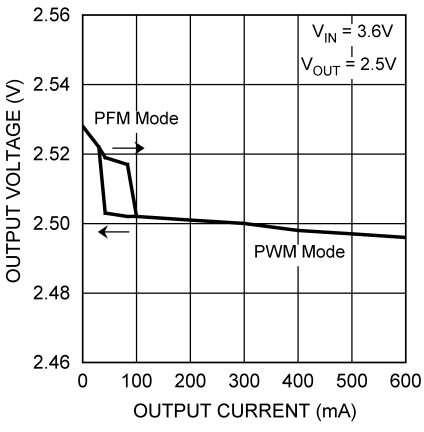

Figure 12. Output Voltage vs Output Current

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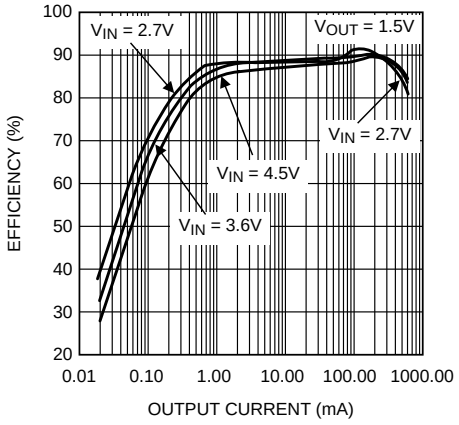
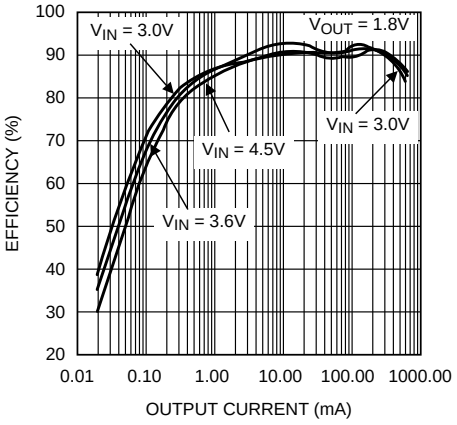
Typical Characteristics (continued)

LM3671MF/TL/LC, circuit of *Figure 32*, V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C, unless otherwise noted.



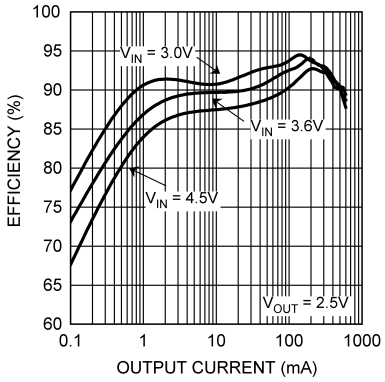
L = 2.2 µH

Figure 13. Efficiency vs Output Current



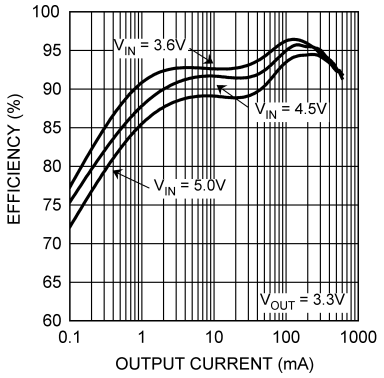
L = 2.2 µH

Figure 14. Efficiency vs Output Current



L = 2.2 µH

Figure 15. Efficiency vs Output Current



L = 2.2 µH

Figure 16. Efficiency vs Output Current

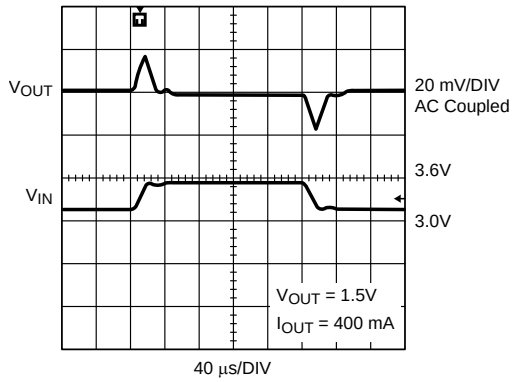


Figure 17. Line Transient Response (PWM Mode)

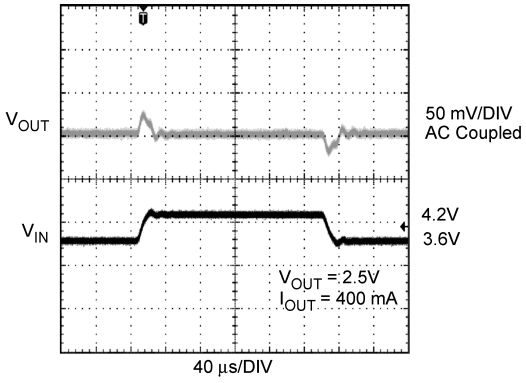


Figure 18. Line Transient Response (PWM Mode)

Typical Characteristics (continued)

LM3671MF/TL/LC, circuit of *Figure 32*, V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C, unless otherwise noted.

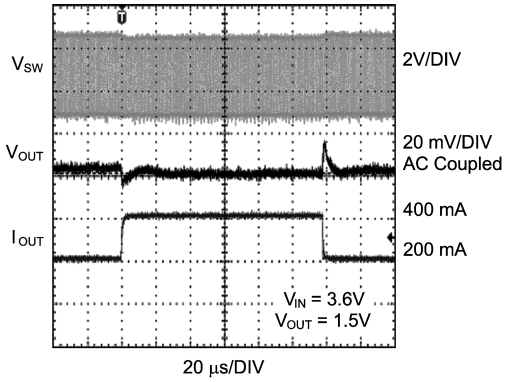


Figure 19. Load Transient Response (PWM Mode)

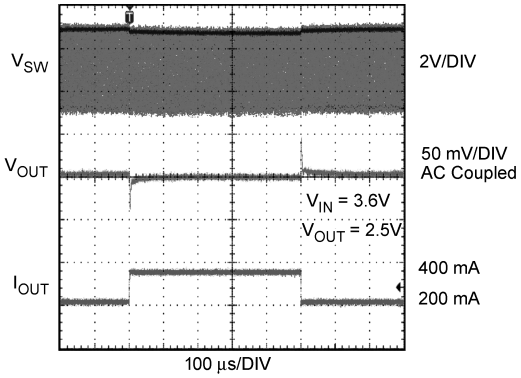
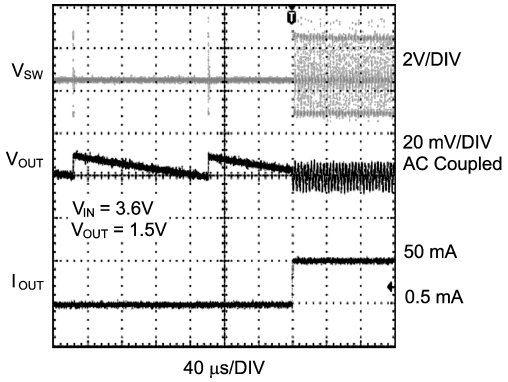
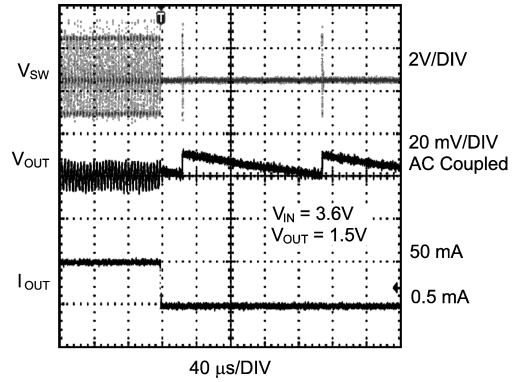


Figure 20. Load Transient Response (PWM Mode)



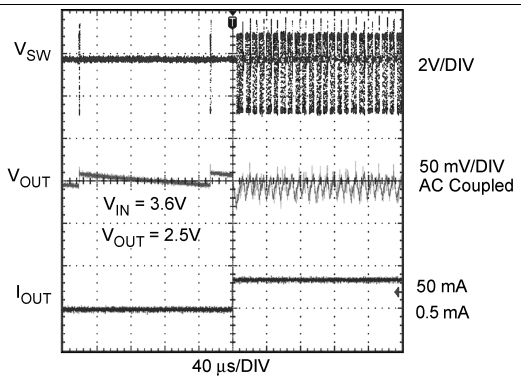
PFM Mode 0.5 mA to 50 mA

Figure 21. Load Transient Response



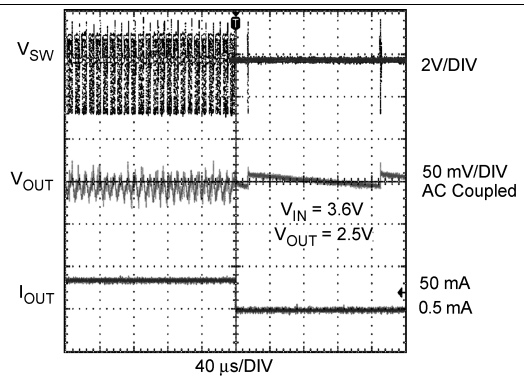
PFM Mode 0.5 mA to 50 mA

Figure 22. Load Transient Response



PFM Mode 0.5 mA to 50 mA

Figure 23. Load Transient Response



PFM Mode 50 mA to 0.5 mA

Figure 24. Load Transient Response

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Typical Characteristics (continued)

LM3671MF/TL/LC, circuit of *Figure 32*, V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C, unless otherwise noted.

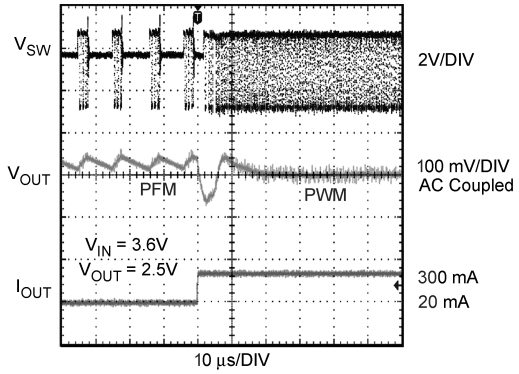


Figure 25. PFM-to-PWM Mode Change by Load Transients

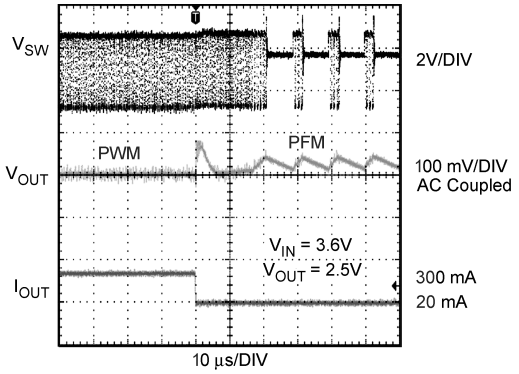


Figure 26. PWM-to-PFM Mode Change by Load Transients

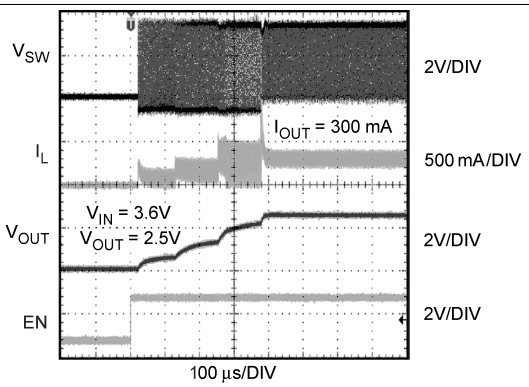


Figure 27. Start-Up into PWM Mode

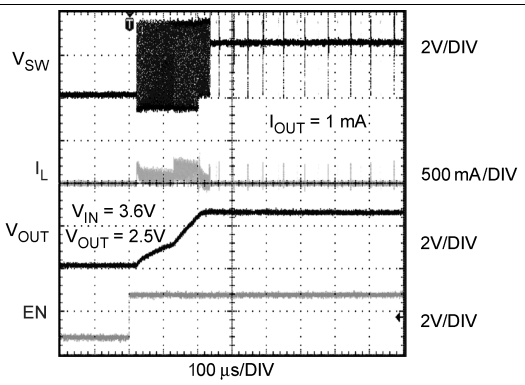


Figure 28. Start-Up into PFM Mode

7 Detailed Description

7.1 Overview

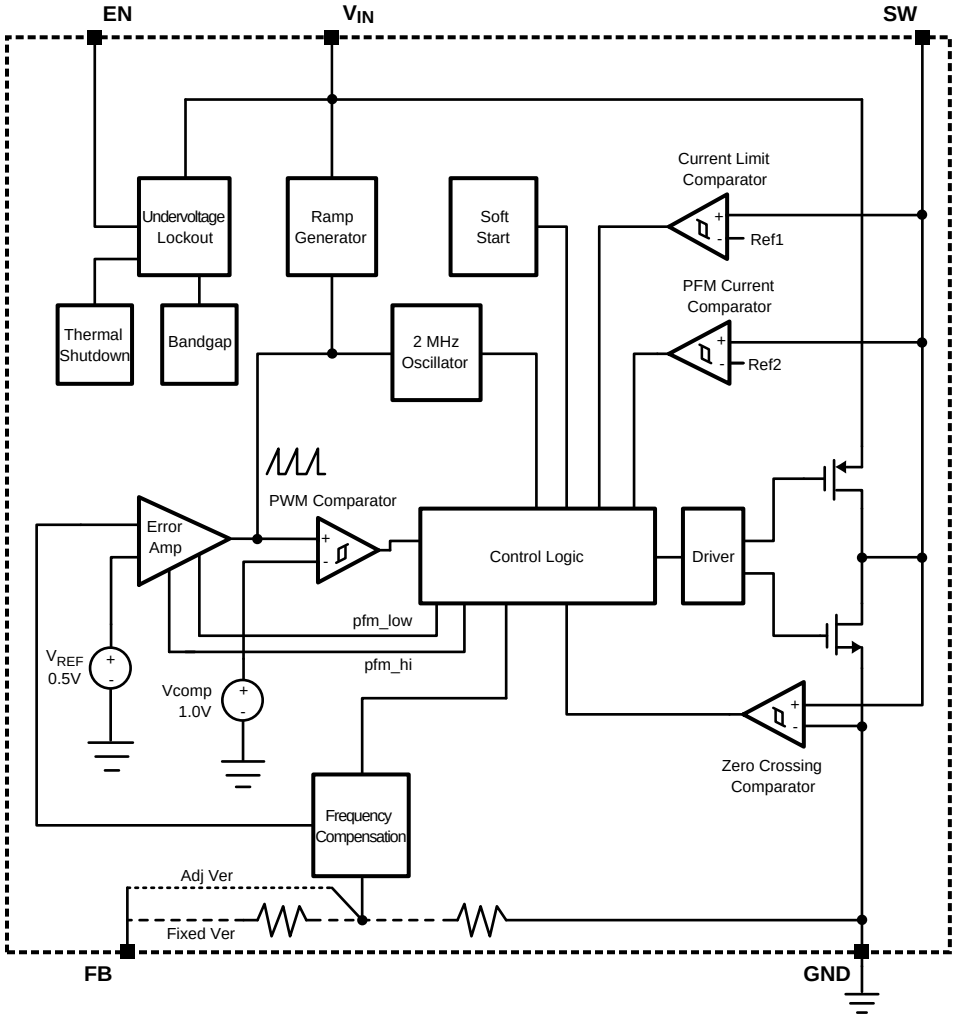
The LM3671, a high-efficiency step-down DC-DC switching buck converter, delivers a constant voltage from a single Li-Ion battery and input voltage rails from 2.7 V to 5.5 V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3671 has the ability to deliver up to 600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required: pulse width modulation (PWM), pulse frequency modulation (PFM), and shutdown. The device operates in PWM mode at load current of approximately 80 mA or higher. Lighter load current cause the device to automatically switch into PFM for reduced current consumption (I_Q = 16 µA typical) and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.01 µA typical).

Additional features include soft-start, undervoltage protection, current overload protection, and thermal shutdown protection. As shown in the *Figure 35*, only three external power components are required for implementation.

The device uses an internal reference voltage of 0.5 V. TI recommends keeping the device in shutdown until the input voltage is 2.7 V or higher.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Circuit Operation

During the first portion of each switching cycle, the control block in the LM3671 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} – V_{OUT})/L$, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $–V_{OUT}/L$.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

7.3.2 Soft Start

The LM3671 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after Vin reaches 2.7 V. Soft start is implemented by increasing switch current limit in steps of 70 mA, 140 mA, 280 mA and 1020 mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at startup. Typical start-up times with a 10-µF output capacitor and 300-mA load is 400 µs and with 1-mA load is 275 µs.

7.4 Device Functional Modes

7.4.1 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

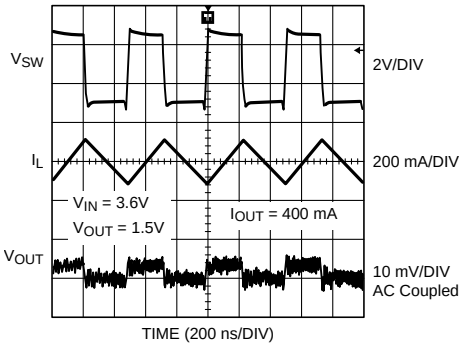

Figure 29. Typical PWM Operation

Device Functional Modes (continued)

7.4.1.1 Internal Synchronous Rectification

While in PWM mode, the LM3671 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

7.4.1.2 Current Limiting

A current limit feature allows the LM3671 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1020 mA (typical). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay, thereby preventing runaway.

7.4.2 PFM Operation

At very light load, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The device automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The NFET current reaches zero.
2. The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 30 mA + V_{IN}/42 Ω).

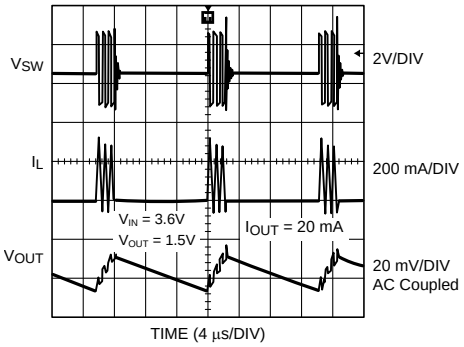

Figure 30. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between approximately 0.6% and 1.7% above the nominal PWM output voltage. If the output voltage is below the high PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the high PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112 mA + V_{IN}/27 Ω.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 31), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off, and the device enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 16 µA (typ.), which allows the device to achieve high efficiency under extremely light load conditions.

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Device Functional Modes (continued)

If the load current should increase during PFM mode (see Figure 31) causing the output voltage to fall below the low2 PFM threshold, the device will automatically transition into fixed-frequency PWM mode. When V_{IN} = 2.7 V the device transitions from PWM to PFM mode at approximately 35 mA output current and from PFM to PWM mode at approximately 85 mA , when V_{IN} = 3.6 V, PWM to PFM transition happens at approximately 50 mA and PFM to PWM transition happens at approximately 100 mA, when V_{IN} = 4.5 V, PWM to PFM transition happens at approximately 65 mA and PFM to PWM transition happens at approximately 115 mA.

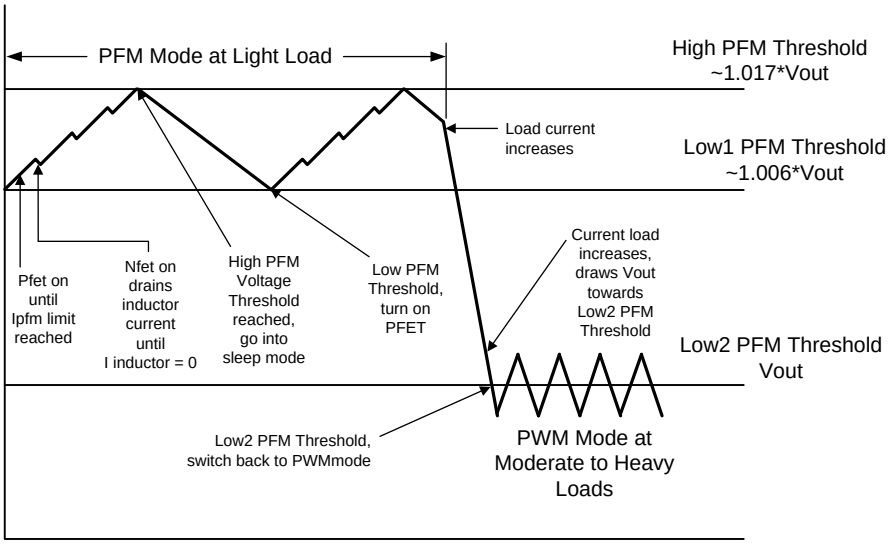

Figure 31. Operation in PFM Mode and Transfer to PWM Mode

7.4.3 Shutdown

Setting the EN input pin low (< 0.4 V) places the LM3671 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3671 are turned off. Setting EN high (> 1 V) enables normal operation. It is recommended to set EN pin low to turn off the LM3671 during system power up and undervoltage conditions when the supply is less than 2.7 V. Do not leave the EN pin floating.

7.4.4 Low Dropout Operation (LDO)

The LM3671-ADJ can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage is

$$V_{IN,\ MIN} = I_{LOAD} \times (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT} \quad (1)$$

where

- I_{LOAD}: Load current
- $R_{DSON,\ PFET}$: Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$: Inductor resistance

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The external control of this device is very easy. First make sure the correct voltage been applied at V_{IN} pin, then simply apply the voltage at EN pin according to the *Electrical Characteristics* to enable or disable the output voltage.

8.2 Typical Application

8.2.1 Typical Application: Fixed-Voltage Version

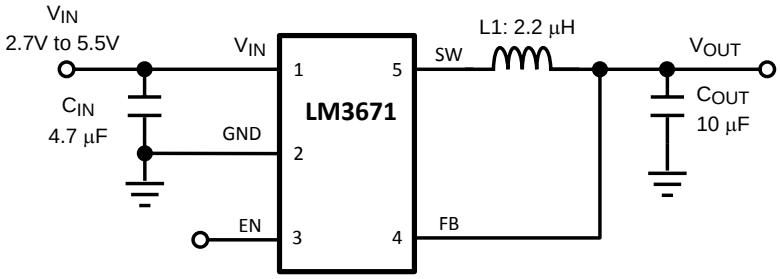

Figure 32. LM3671 Fixed-Voltage Typical Application Circuit

8.2.1.1 Design Requirements

Two ceramic capacitors and one inductor required for this application. These three external components need to be selected very carefully for property operation. Please read *Detailed Design Procedure*.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. *The minimum value of inductance to specify good performance is 1.76 µH at I_{LIM} (typical) DC current over the ambient temperature range.* Shielded inductors radiate less noise and should be preferred.

There are two methods to choose the inductor saturation current rating.

8.2.1.2.1.1 Method 1

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

where

- I_{RIPPLE}: average to peak inductor current

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Typical Application (continued)

- I_{OUTMAX}: maximum load current (600 mA)
- V_{IN}: maximum input voltage in application
- L : min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f : minimum switching frequency (1.6 MHz)
- V_{OUT}: output voltage (2)

8.2.1.2.1.2 Method 2

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 1150 mA.

A 2.2-µH inductor with a saturation current rating of at least 1150 mA is recommended for most applications. Inductor resistance should be less than 0.3 Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

8.2.1.2.2 Input Capacitor Selection

A ceramic input capacitor of 4.7 µF, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. *The minimum input capacitance to specify good performance is 2.2 µF at 3-V DC bias; 1.5 µF at 5-V DC bias including tolerances and over ambient temperature range.* The input filter capacitor supplies current to the PFET switch of the LM3671 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$ (3)

Table 1. Suggested Inductors and Their Suppliers

MODEL	VENDOR	DIMENSIONS L × W × H (mm)	D.C.R (maximum)(mΩ)
DO3314-222MX	Coilcraft	3.3 × 3.3 × 1.4	200
LPO3310-222MX	Coilcraft	3.3 × 3.3 × 1	150
ELL5GM2R2N	Panasonic	5.2 × 5.2 × 1.5	53
CDRH2D14NP-2R2NC	Sumida	3.2 × 3.2 × 1.55	94

8.2.1.2.3 Output Capacitor Selection

A ceramic output capacitor of 10 µF, 6.3 V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to specify good performance is 5.75 µF at 1.8-V DC bias including tolerances and over ambient temperature range. The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

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The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed by Equation 4:

$$V_{PP-C} = \frac{I_{RIPPLE}}{4*f*C} \quad (4)$$

Voltage peak-to-peak ripple due to ESR can be expressed by Equation 5:

$$V_{PP-ESR} = (2 \times I_{RIPPLE}) \times R_{ESR} \quad (5)$$

Because these two components are out of phase the rms (root mean squared) value can be used to get an approximate value of peak-to-peak ripple.

The peak-to-peak ripple voltage, rms value can be expressed by Equation 6:

$$V_{PP-RMS} = \sqrt{V_{PP-C}^{2} + V_{PP-ESR}^{2}} \quad (6)$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 2. Suggested Capacitors and Their Suppliers

MODEL	TYPE	VENDOR	VOLTAGE RATING (V)	CASE SIZE INCH (mm)
4.7 µF for C_{IN}				
C2012X5R0J475K	Ceramic, X5R	TDK	6.3	0805 (2012)
JMK212BJ475K	Ceramic, X5R	Taiyo-Yuden	6.3	0805 (2012)
GRM21BR60J475K	Ceramic, X5R	Murata	6.3	0805 (2012)
C1608X5R0J475K	Ceramic, X5R	TDK	6.3	0603 (1608)
10 µF for C_{OUT}				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3	0805 (2012)
C1608X5R0J106K	Ceramic, X5R	TDK	6.3	0603 (1608)

8.2.1.3 Application Curves

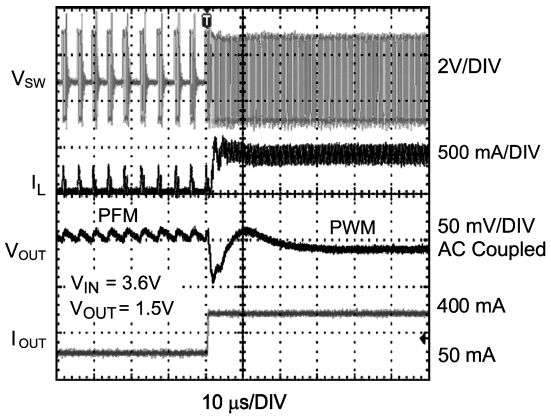

Figure 33. PFM-to-PWM Mode Change by Load Transients

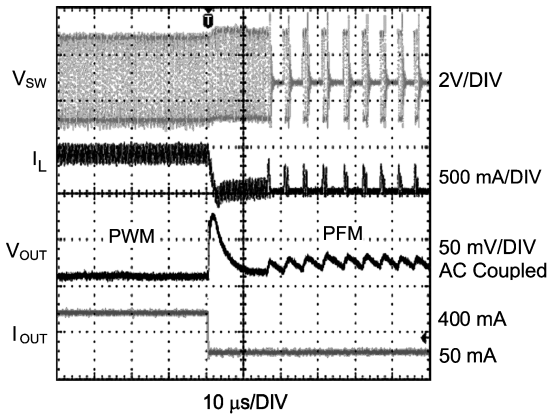

Figure 34. PWM-to-PFM Mode Change by Load Transients

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8.2.2 Typical Application: ADJ Version

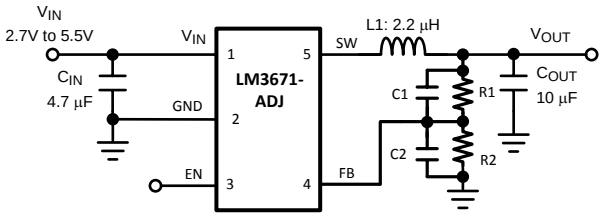

Figure 35. Typical Application Circuit for ADJ Version

8.2.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.5 V
Input capacitor	4.7 µF
Output capacitor	10 µF
Inductor	2.2 µH
ADJ programmable output voltage	1.1 V to 3.3 V

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Voltage Selection for LM3671-ADJ

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to FB, then to GND. V_{OUT} is adjusted to make the voltage at FB equal to 0.5 V. The resistor from FB to GND (R2) should be 200 kΩ to keep the current drawn through this network well below the 16-µA quiescent current level (PFM mode) but large enough that it is not susceptible to noise. If R2 is 200 kΩ, and V_{FB} is 0.5 V, the current through the resistor feedback network will be 2.5 µA. The output voltage of the adjustable parts ranges from 1.1 V to 3.3 V.

The formula for output voltage selection is:

$$V_{OUT} = V_{FB} * \left(1 + \frac{R1}{R2}\right) \quad (7)$$

where

- V_{OUT}: output voltage (volts)
- V_{FB} : feedback voltage = 0.5 V
- R1: feedback resistor from V_{OUT} to FB
- R2: feedback resistor from FB to GND

For any output voltage greater than or equal to 1.1 V, a zero must be added around 45 kHz for stability. The formula for calculation of C1 is:

$$C1 = \frac{1}{(2 * \pi * R1 * 45\ kHz)} \quad (8)$$

For output voltages higher than 2.5 V, a pole must be placed at 45 kHz as well. If the pole and zero are at the same frequency the formula for calculation of C2 is:

$$C2 = \frac{1}{(2 * \pi * R2 * 45\ kHz)} \quad (9)$$

The formula for location of zero and pole frequency created by adding C1 and C2 is given below. By adding C1, a zero as well as a higher frequency pole is introduced.

$$Fz = \frac{1}{(2 * \pi * R1 * C1)} \quad (10)$$

$$Fp = \frac{1}{2 * \pi * (R1 \| R2) * (C1+C2)} \quad (11)$$

See the Table 3 table.

Table 3. LM3671-ADJ Configurations for Various V_{OUT} (Circuit of Figure 35)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)
0.9	160	200	22	none	2.2	4.7	10
1.1	240	200	15	none	2.2	4.7	10
1.2	280	200	12	none	2.2	4.7	10
1.3	320	200	12	none	2.2	4.7	10
1.5	357	178	10	none	2.2	4.7	10
1.6	442	200	8.2	none	2.2	4.7	10
1.7	432	178	8.2	none	2.2	4.7	10
1.8	464	178	8.2	none	2.2	4.7	10
1.875	523	191	6.8	none	2.2	4.7	10
2.5	402	100	8.2	none	2.2	4.7	10
2.8	464	100	8.2	33	2.2	4.7	10
3.3	562	100	6.8	33	2.2	4.7	10

8.2.2.3 Application Curves

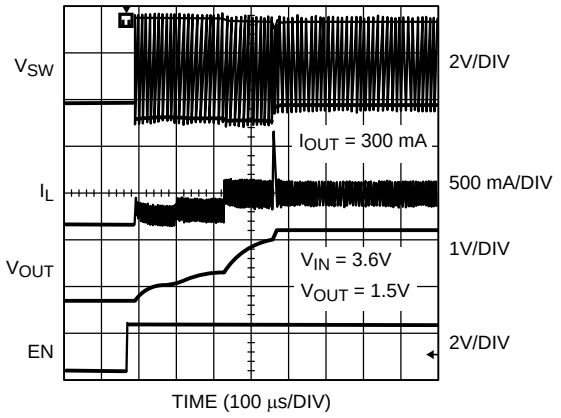

Figure 36. Start-Up into PWM Mode

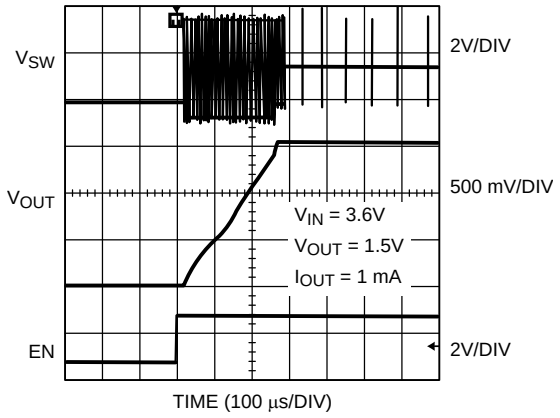

Figure 37. Start-Up into PFM Mode

9 Power Supply Recommendations

The LM3671 is designed to operate from a stable input supply range of 2.7 V to 5.5 V.

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10 Layout

10.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability.

Good layout for the LM3671 can be implemented by following a few simple design rules below. Refer to Figure 38 for top layer board layout.

1. *Place the LM3671, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor through the LM3671 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3671 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LM3671 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3671 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3671 circuit and should be direct but must be routed opposite to noisy components. This reduces EMI-radiated onto the voltage feedback trace of the DC-DC converter. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner, for the adjustable part, the feedback dividers should be on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (because this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to the circuitry is post-regulated to reduce conducted noise, using LDOs.

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10.2 Layout Example

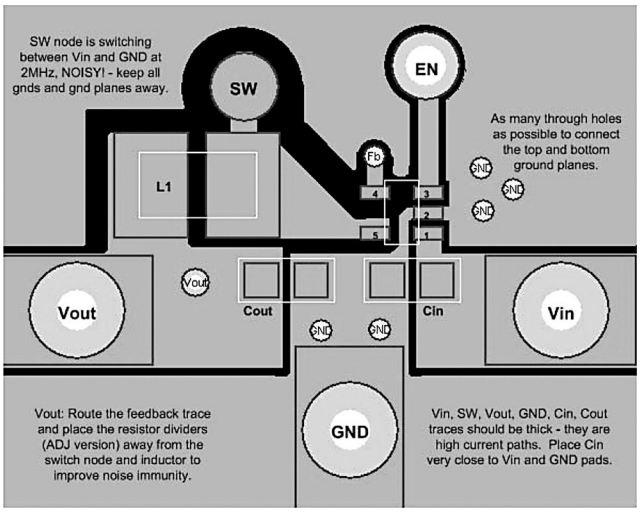

Figure 38. Top Layer Board Layout for SOT-23

10.3 DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009). Refer to the section *Surface Mount Technology (DSBGA) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board must be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009) for specific instructions how to do this. The 5-pin package used for LM3671 has 300-micron solder balls and requires 10.82 mils pads for mounting on the circuit board. The trace to each pad must enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long or longer, as a thermal relief. Then each trace must neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3671 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1 and A3, because V_{IN} and GND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009).

11.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM3671	Click here	Click here	Click here	Click here	Click here
LM3671-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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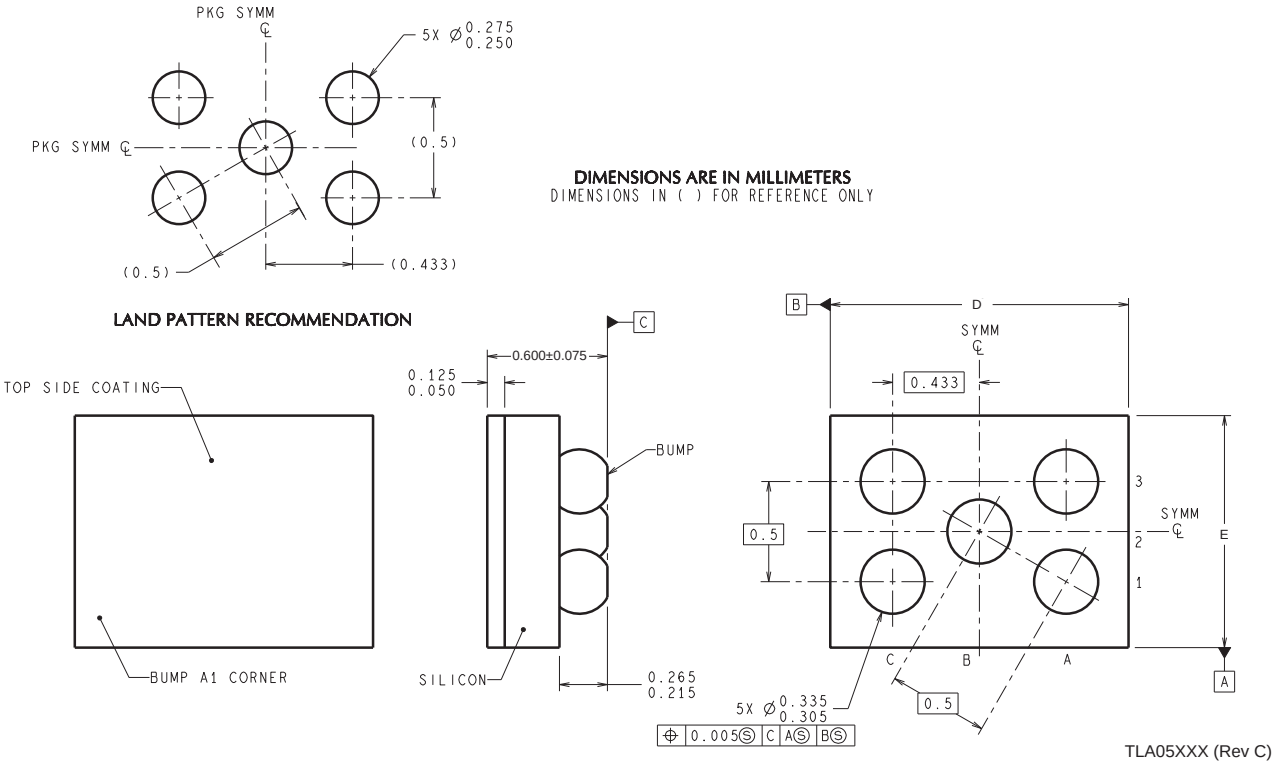
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3671MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671MFX-1.875/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671QMF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671QMFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3671QTL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671QTLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-1.2/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-1.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-2.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-3.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TL-ADJ/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-1.2/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-1.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-2.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-2.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-3.3/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LM3671TLX-ADJ/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3671LC-1.2/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LM3671LC-1.3/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LM3671LC-1.6/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LM3671LC-1.8/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LM3671MF-1.2	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.25/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.375/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-1.875/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MF-ADJ/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671MFX-1.25/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671MFX-1.875/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3671MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671MFX-ADJ/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671QMF-1.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3671QMFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3671QTL-1.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671QTLX-1.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TL-1.2/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TL-1.5/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TL-1.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TL-2.5/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TL-2.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TL-3.3/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TL-ADJ/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LM3671TLX-1.2/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TLX-1.5/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TLX-1.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TLX-2.5/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TLX-2.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TLX-3.3/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LM3671TLX-ADJ/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0

YZR0005



D: Max = 1.413 mm, Min =1.352 mm

E: Max = 1.083 mm, Min =1.022 mm

4215043/A 12/12

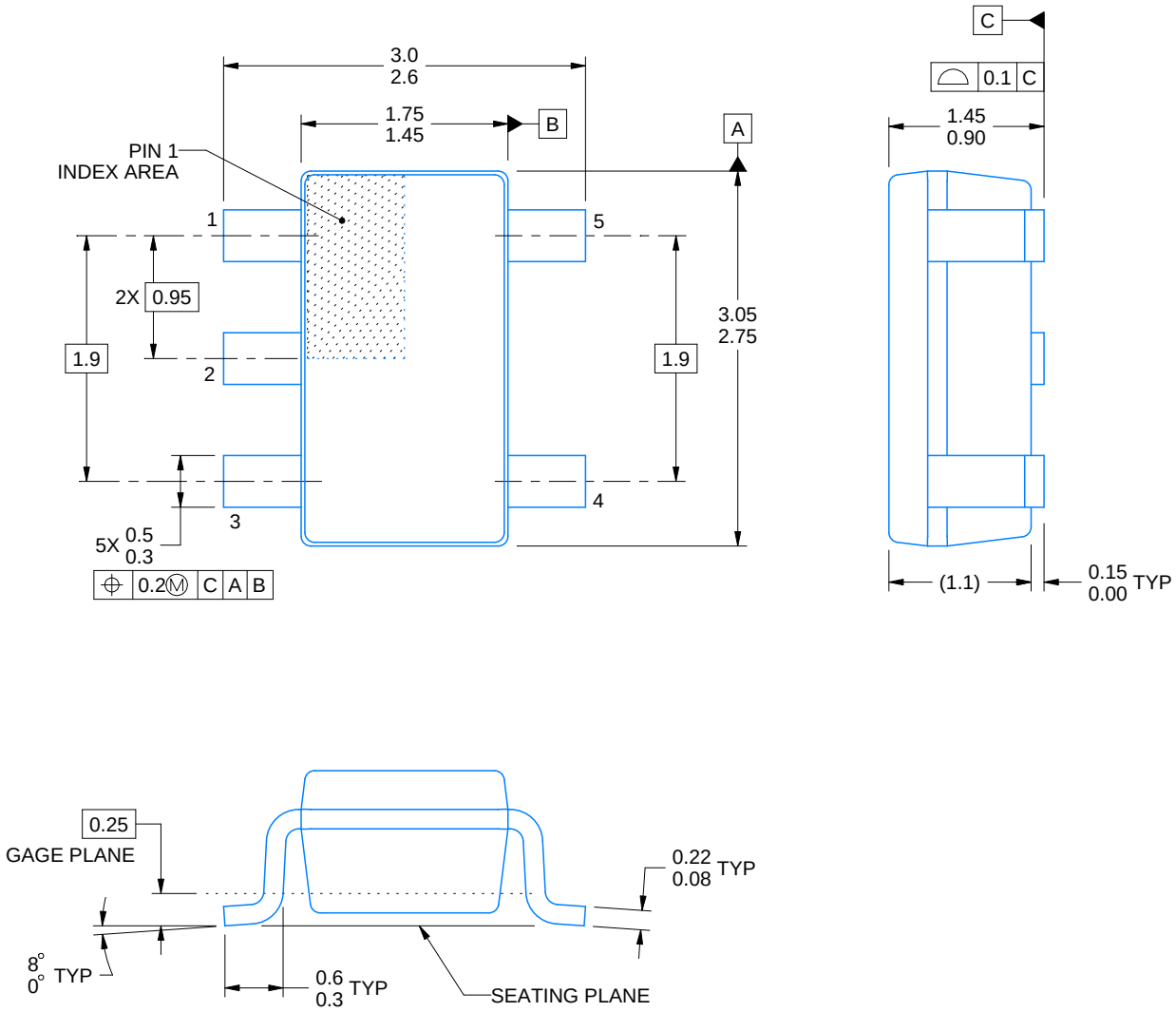
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

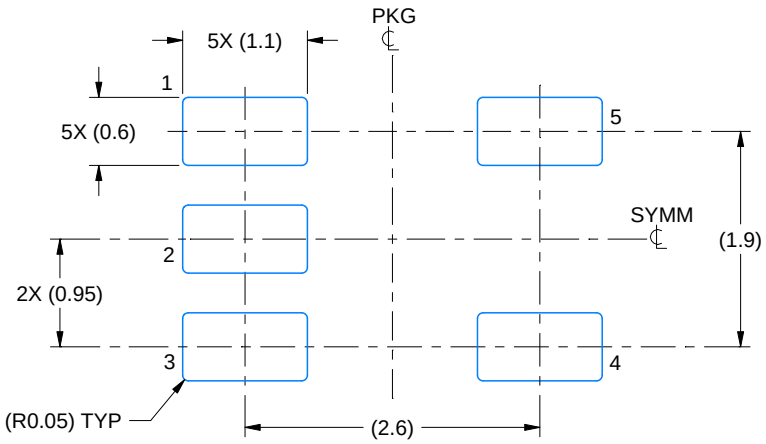
SMALL OUTLINE TRANSISTOR



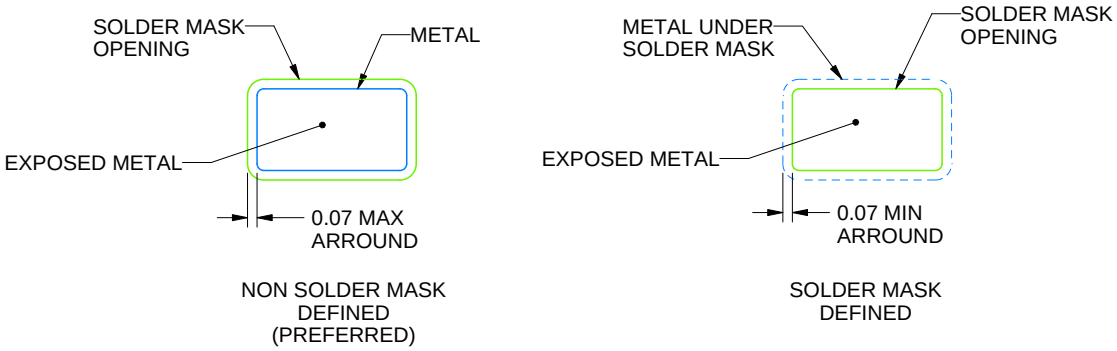
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

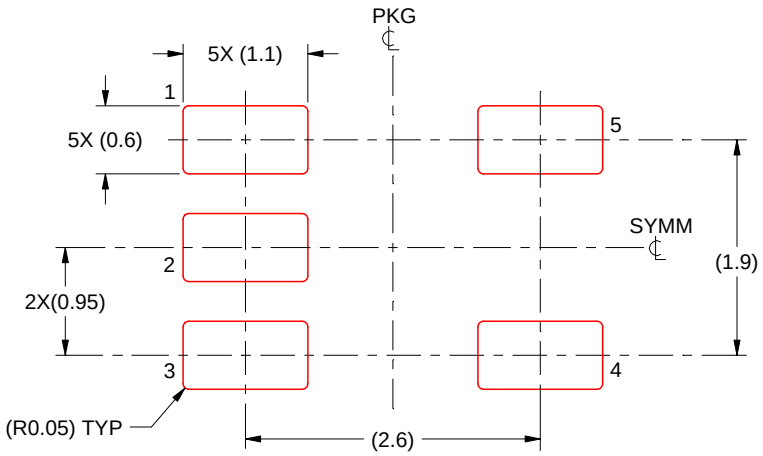


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



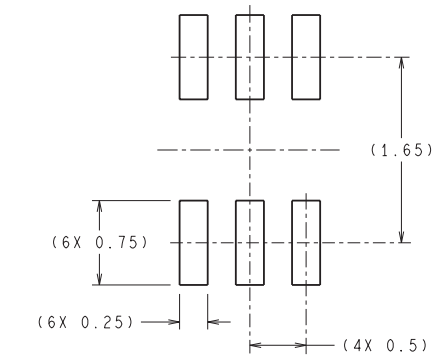
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

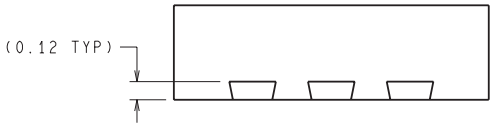
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

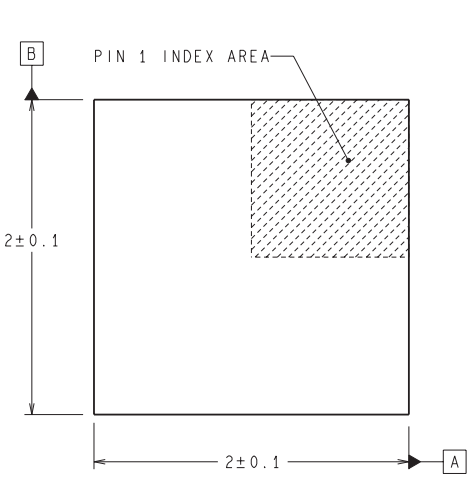
NKH0006B

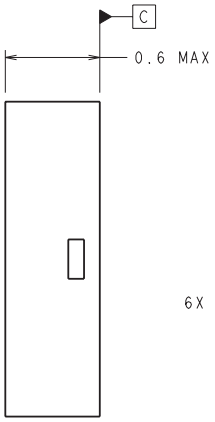


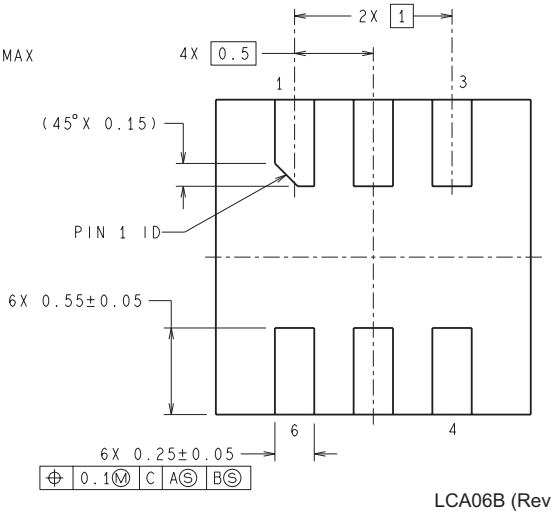
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY









LCA06B (Rev A)

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