TEXAS INSTRUMENTS

OPA211, OPA2211

SBOS377H – OCTOBER 2006 – REVISED NOVEMBER 2015

OPA2x11 1.1-nv/√Hz Noise, Low Power, Precision Operational Amplifier

1 Features

- Low Voltage Noise: 1.1 nV/√Hz at 1 kHz
- Input Voltage Noise: 80 nV_{PP} (0.1 to 10 Hz)
- THD + N: –136 dB (G = 1, f = 1 kHz)
- Offset Voltage: 125 µV (Maximum)
- Offset Voltage Drift: 0.35 µV/°C (Typical)
- Low Supply Current: 3.6 mA/Ch (Typical)
- Unity-Gain Stable
- Gain Bandwidth Product:
  - 80 MHz (G = 100)
  - 45 MHz (G = 1)
- Slew Rate: 27 V/µs
- 16-Bit Settling: 700 ns
- Wide Supply Range: ±2.25 to ±18 V, 4.5 to 36 V
- Rail-to-Rail Output
- Output Current: 30 mA
- SON-8 (3 mm × 3 mm), VSSOP-8, and SOIC-8

2 Applications

- PLL Loop Filters
- Low-Noise, Low-Power Signal Processing
- 16-Bit ADC Drivers
- DAC Output Amplifiers
- Active Filters
- Low-Noise Instrumentation Amps
- Ultrasound Amplifiers
- Professional Audio Preamplifiers
- Low-Noise Frequency Synthesizers
- Infrared Detector Amplifiers
- Hydrophone Amplifiers
- Geophone Amplifiers
- Medical

3 Description

The OPA211 series of precision operational amplifiers achieves very low 1.1-nV/√Hz noise density with a supply current of only 3.6 mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

The extremely low voltage and low current noise, high-speed, and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA211 series of operational amplifiers provides 700-ns settling time to 16-bit accuracy throughout 10-V output swings. This ac performance, combined with only 125 µV of offset and 0.35 µV/°C of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA211 series is specified over a wide dual-power supply range of ±2.25 to ±18 V, or for single-supply operation from 4.5 to 36 V.

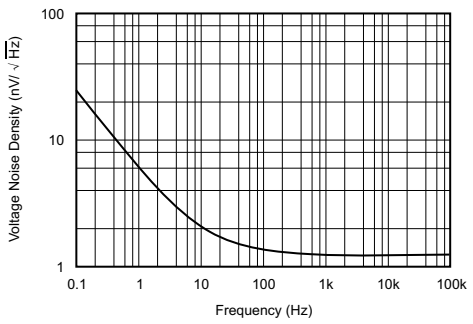
The OPA211 is available in the small SON-8 (3 mm × 3 mm), VSSOP-8, and SOIC-8 packages. A dual version, the OPA2211, is available in the SON-8 (3 mm × 3 mm) or an SO-8 PowerPAD™ package. This series of operational amplifiers is specified from T_A = –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA211	SOIC (8)	4.90 mm × 3.90 mm
	SON (8)	3.00 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2211	SON (8)	3.00 mm × 3.00 mm
	SO PowerPAD (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Input Voltage Noise Density vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2009) to Revision H	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

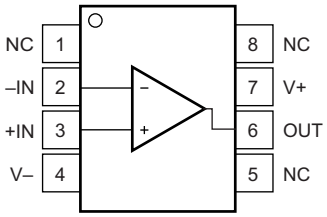
5 Device Comparison Table(1)

PRODUCT	PACKAGE-LEAD	SINGLE	SHUTDOWN	DUAL
STANDARD GRADE				
OPA211AI	SON-8 (3 mm × 3 mm)	✓	✓	
	VSSOP-8	✓	✓	
	SOIC-8	✓		
OPA2211AI	SON-8 (3mm × 3mm)			✓
	SO-PowerPAD-8			✓
HIGH GRADE				
OPA211I	SON-8 (3 mm × 3 mm)	✓	✓	
	VSSOP-8	✓	✓	
	SOIC-8	✓		

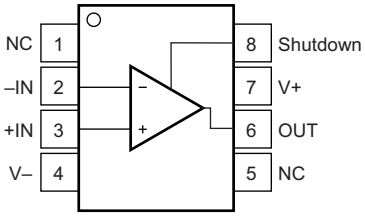
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

6 Pin Configurations

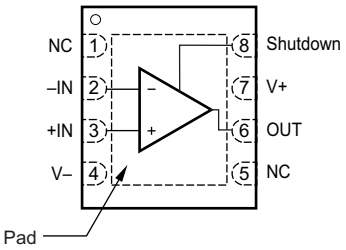
OPA211 D Package
8-Pin SOIC
Top View



OPA211 DGK Package
8-Pin VSSOP
Top View



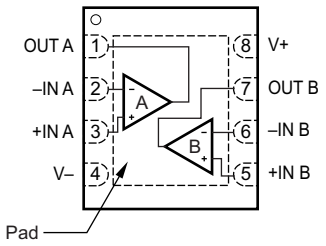
OPA211 DRG Package
8-Pin SON
Top View



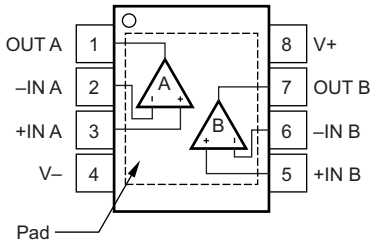
Pin Functions—OPA211

PIN				I/O	DESCRIPTION
NAME	SOIC	VSSOP	SON		
+IN	3	3	3	I	Noninverting input
–IN	2	2	2	I	Inverting input
NC	1, 5, 8	1, 5	1, 5	—	No internal connection. This pin can be left floating or connected to any voltage between (V–) and (V+).
OUT	6	6	6	O	Output
Shutdown	—	8	8	I	Shutdown, Active High The Shutdown function is as follows: Device enabled: (V–) ≤ $V_{SHUTDOWN}$ ≤ (V+) – 3 V Device disabled: $V_{SHUTDOWN}$ ≥ (V+) – 0.35 V
V+	7	7	4	I	Positive power supply
V–	4	4	7	I	Negative power supply
Pad	—	—	9	I	Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad to the printed circuit board is required and improves heat dissipation and provides specified performance.

OPA2211 DRG Package
8-Pin SON With Exposed Thermal Pad
Top View



OPA2211 DDA Package
8-Pin SO PowerPAD With Exposed Thermal Pad
Top View



Pin Functions—OPA2211

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input channel A
–IN A	2	I	Inverting input channel A
+IN B	5	I	Noninverting input channel B
–IN B	6	I	Inverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V+	8	I	Positive power supply
V–	4	I	Negative power supply
Pad	—	—	Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted).(1)

	MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		40	V
Input voltage	(V–) – 0.5	(V+) + 0.5	V
Input current (any pin except power-supply pins)		±10	mA
Output short-circuit(2)	Continuous		
Operating temperature, T_A	–55	150	°C
Junction temperature, T_J		200	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S/2 (ground in symmetrical dual supply setups), one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) - (V-)	4.5 (±2.25)	36 (±18)	36 (±18)	V
Operating temperature, T_A	–55	25	150	°C

7.4 Thermal Information—OPA211

THERMAL METRIC[1]		OPA211			UNIT
		D (SOIC)	DRG (SON)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, high-K board	122.2	125	184.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.5	n/a	71.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	28.8	104.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.2	3	11.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.6	25	103.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	19.1	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information—OPA2211

THERMAL METRIC[1]		OPA2211		UNIT
		DDA (SO-PowerPAD)	DRG (SON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, high-K board	50.4	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.0	28.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	19.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor IC Package Thermal Metrics* application report, SPRA953.

7.6 Electrical Characteristics: V_S = ±2.25 to ±18 V for Standard Grade OPA211AI, OPA2211AI

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = Midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	OPA211AI, V_S = ±15 V		±30	±125	µV
		OPA2211AI, V_S = ±15 V		±50	±150	µV
dV_{OS}/dT	Input offset drift	V_S = ±15 V, T_A = –40°C to +125°C		0.35	1.5	µV/°C
PSRR	Input offset voltage vs power supply	T_A = 25°C		0.1	1	µV/V
		T_A = –40°C to +125°C			3	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±60	±175	nA
		OPA211AI, V_{CM} = 0 V, T_A = –40°C to +125°C			±200	nA
		OPA2211AI, V_{CM} = 0 V, T_A = –40°C to +125°C			±250	nA
I_{OS}	Input offset current	V_{CM} = 0 V		±25	±100	nA
		V_{CM} = 0 V, T_A = –40°C to +125°C			±150	nA
NOISE						
e_n	Input voltage noise	f = 0.1 to 10 Hz		80		nV_{PP}
	Input voltage noise density	f = 10 Hz		2		$nV/\sqrt{Hz}$
		f = 100 Hz		1.4		$nV/\sqrt{Hz}$
		f = 1 kHz		1.1		$nV/\sqrt{Hz}$
I_n	Input current noise density	f = 10 Hz		3.2		$pA/\sqrt{Hz}$
		f = 1 kHz		1.7		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S ≥ ±5 V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5 V	(V–) + 2		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	V_S ≥ ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C	114	120		dB
		V_S < ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C	110	120		dB
INPUT IMPEDANCE						
	Differential			20 || 8		kΩ || pF
	Common-mode			10 || 2		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ, T_A = –40°C to +125°C	114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 600 Ω	110	114		dB
		OPA211, (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, I_O ≤ 15 mA, T_A = –40°C to +125°C	110			dB
		OPA211, (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, 15 mA < I_O ≤ 30 mA, T_A = –40°C to +125°C	103			dB
		OPA2211, (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, I_O ≤ 15 mA, T_A = –40°C to +125°C	100			dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 100		80		MHz
		G = 1		45		MHz
SR	Slew rate			27		V/µs
t_S	Settling time, 0.01%	V_S = ±15 V, G = –1, 10-V Step, C_L = 100 pF		400		ns
	0.0015% (16-bit)	V_S = ±15 V, G = –1, 10-V Step, C_L = 100 pF		700		ns

Electrical Characteristics: V_S = ±2.25 to ±18 V for Standard Grade OPA211AI, OPA2211AI (continued)

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = Midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Overload recovery time	G = –10		500		ns
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3V_{RMS}, R_L = 600 Ω		0.000015 %		
				–136		dB
OUTPUT						
V_{OUT}	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 114 dB, T_A = –40°C to +125°C	(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} ≥ 110 dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 15 mA, A_{OL} ≥ 110 dB, T_A = –40°C to +125°C	(V–) + 0.6		(V+) – 0.6	V
I_{SC}	Short-circuit current			+30/–45		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1 MHz		5		Ω
SHUTDOWN						
$V_{Shutdown}$	Shutdown pin input voltage(1)	Device disabled (shutdown)	(V+) – 0.35			V
		Device enabled			(V+) – 3	V
	Shutdown pin leakage current			1		µA
	Turnon time(2)			2		µs
	Turnoff time(2)			3		µs
	Shutdown current	Shutdown (disabled)		1	20	µA
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		3.6	4.5	mA
		I_{OUT} = 0 A, T_A = –40°C to +125°C			6	mA
TEMPERATURE RANGE						
T_A	Specified range		–40		125	°C
T_A	Operating range		–55		150	°C

(1) When disabled, the output assumes a high-impedance state.
(2) See *Typical Characteristics* curves, Figure 39 through Figure 41.

7.7 Electrical Characteristics: V_S = ±2.25 to ±18 V for High Grade OPA211I

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = Midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±15 V		±20	±50	µV
dV_{OS}/dT	Input offset drift	V_S = ±15 V, T_A = –40°C to +125°C		0.15	0.85	µV/°C
PSRR	Input offset voltage vs power supply	T_A = 25°C		0.1	0.5	µV/V
		T_A = –40°C to +125°C			3	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±50	±125	nA
		V_{CM} = 0 V, T_A = –40°C to +125°C			±200	nA
I_{OS}	Input offset current	V_{CM} = 0 V		±20	±75	nA
		T_A = –40°C to +125°C			±150	nA
NOISE						
e_n	Input voltage noise	f = 0.1 to 10 Hz		80		nV_{PP}
	Input voltage noise density	f = 10 Hz		2		$nV/\sqrt{Hz}$
		f = 100 Hz		1.4		$nV/\sqrt{Hz}$
		f = 1 kHz		1.1		$nV/\sqrt{Hz}$
I_n	Input current noise density	f = 10 Hz		3.2		$pA/\sqrt{Hz}$
		f = 1 kHz		1.7		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S ≥ ±5 V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5 V	(V–) + 2		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	V_S ≥ ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C	114	120		dB
		V_S < ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C	110	120		dB
INPUT IMPEDANCE						
	Differential			20 || 8		kΩ || pF
	Common-mode			10 || 2		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ, T_A = –40°C to +125°C	114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 600 Ω	110	114		dB
		OPA211, (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, I_O ≤ 15 mA, T_A = –40°C to +125°C	110			dB
		OPA211, (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, 15 mA < I_O ≤ 30 mA, T_A = –40°C to +125°C	103			dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 100		80		MHz
		G = 1		45		MHz
SR	Slew rate			27		V/µs
t_S	Settling time, 0.01%	V_S = ±15 V, G = –1, 10-V Step, C_L = 100 pF		400		ns
	0.0015% (16-bit)	V_S = ±15 V, G = –1, 10-V Step, C_L = 100 pF		700		ns
	Overload recovery time	G = –10		500		ns
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = $3V_{RMS}$, R_L = 600 Ω		0.000015 %		
				–136		dB

Electrical Characteristics: V_S = ±2.25 to ±18 V for High Grade OPA211I (continued)

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = Midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 114 dB, T_A = –40°C to +125°C	(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} ≥ 110 dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 15 mA, A_{OL} ≥ 110 dB, T_A = –40°C to +125°C	(V–) + 0.6		(V+) – 0.6	V
I_{SC}	Short-circuit current			+30/–45		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1 MHz		5		Ω
SHUTDOWN						
$V_{Shutdown}$	Shutdown pin input voltage(1)	Device disabled (shutdown)	(V+) – 0.35			V
		Device enabled			(V+) – 3	V
	Shutdown pin leakage current			1		µA
	Turnon time(2)			2		µs
	Turnoff time(2)			3		µs
	Shutdown current	Shutdown (disabled)		1	20	µA
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		3.6	4.5	mA
		I_{OUT} = 0 A, T_A = –40°C to +125°C			6	mA
TEMPERATURE RANGE						
T_A	Specified range		–40		125	°C
T_A	Operating range		–55		150	°C

(1) When disabled, the output assumes a high-impedance state.
(2) See *Typical Characteristics* curves, Figure 39 through Figure 41.

7.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

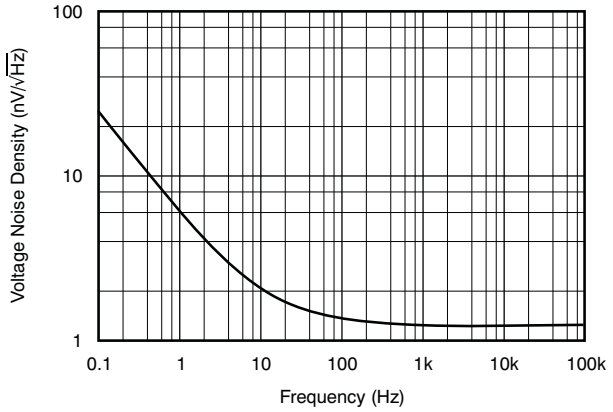


Figure 1. Input Voltage Noise Density vs Frequency

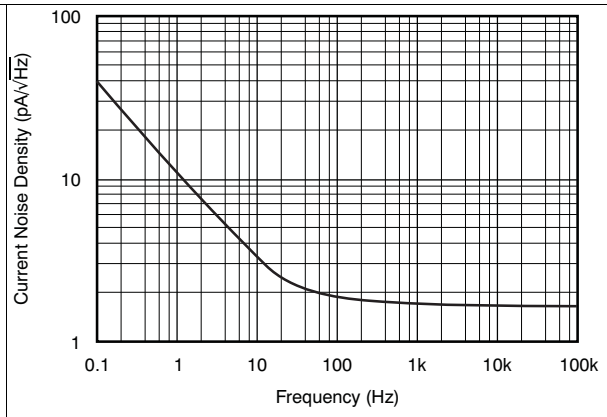


Figure 2. Input Current Noise Density vs Frequency

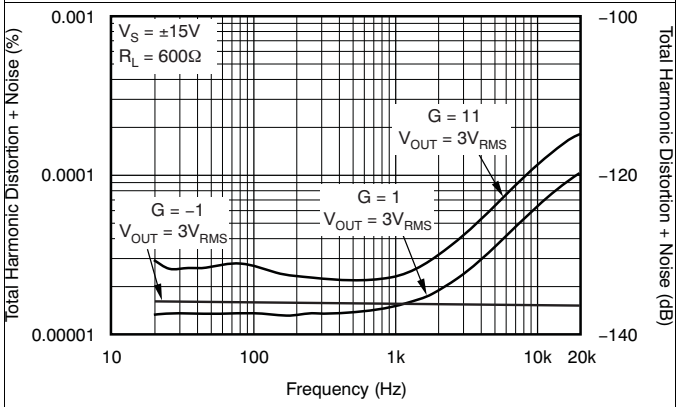


Figure 3. THD + N Ratio vs Frequency

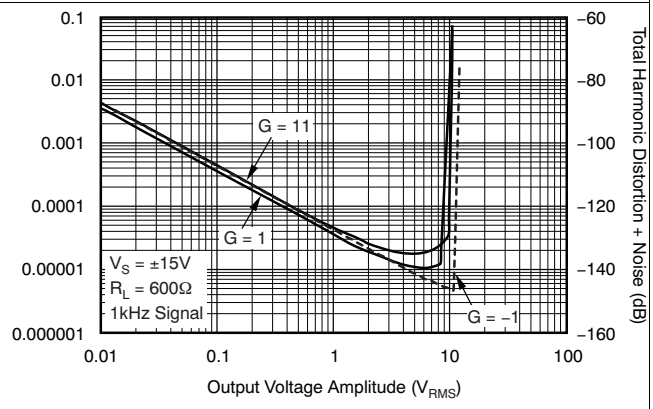


Figure 4. THD + N Ratio vs Output Voltage Amplitude

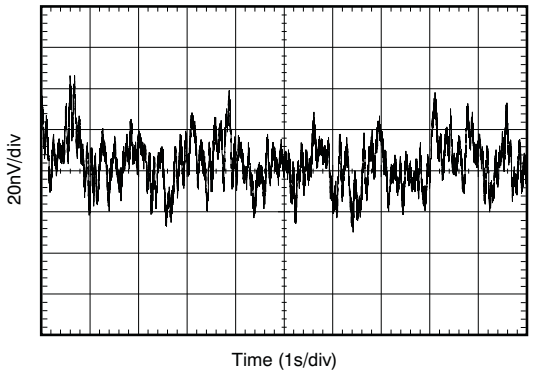


Figure 5. 0.1- to 10-Hz Noise

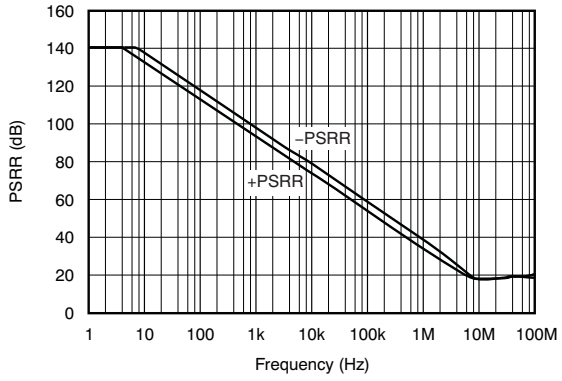


Figure 6. Power-Supply Rejection Ratio vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

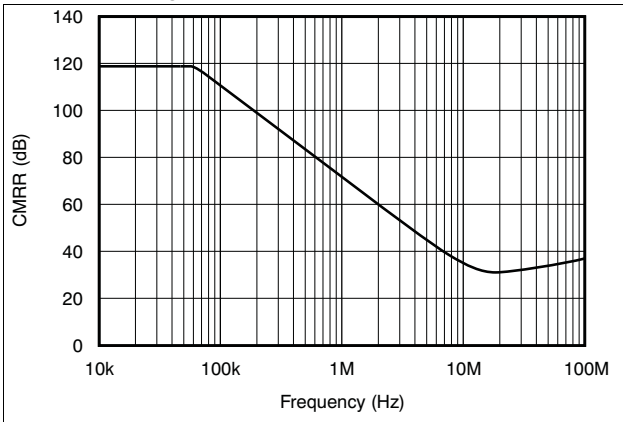


Figure 7. Common-Mode Rejection Ratio vs Frequency

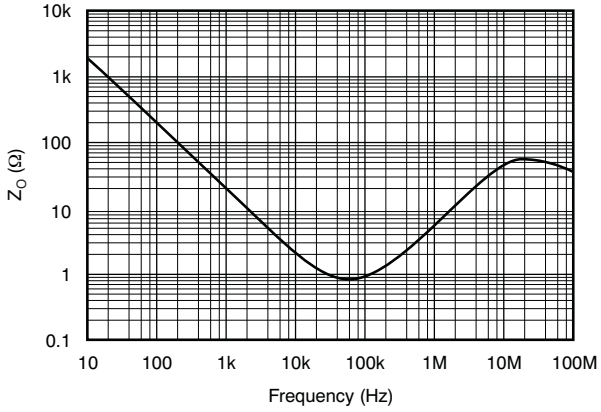


Figure 8. Open-Loop Output Impedance vs Frequency

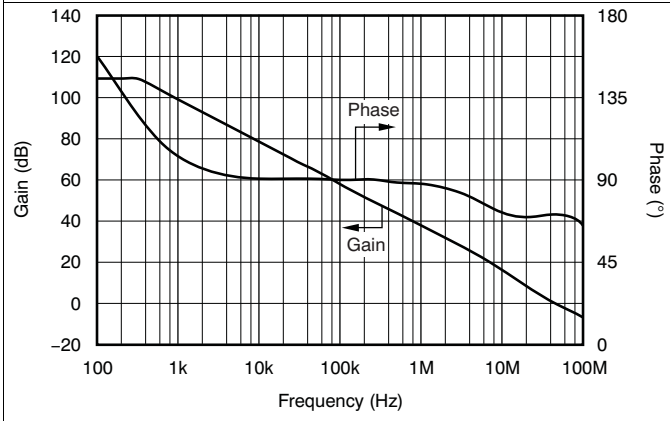


Figure 9. Gain and Phase vs Frequency

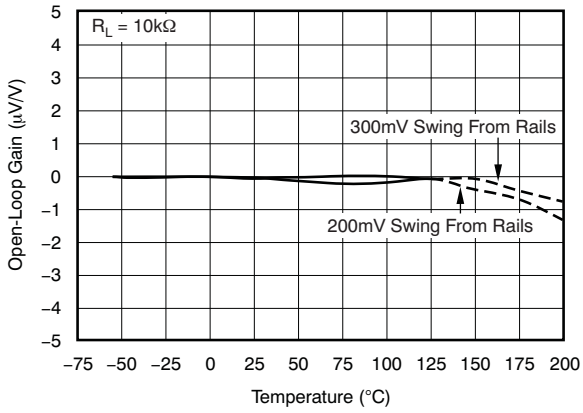


Figure 10. Open-Loop Gain vs Temperature

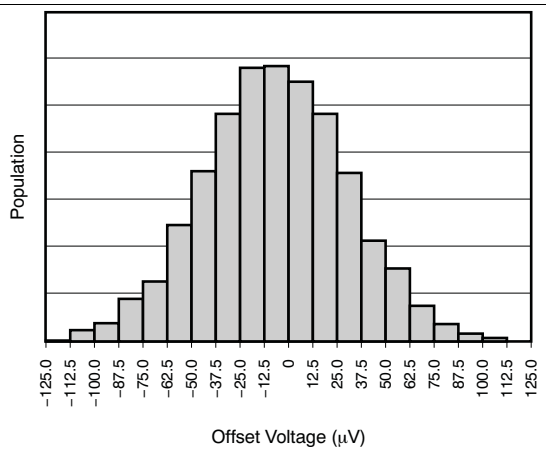


Figure 11. Offset Voltage Production Distribution

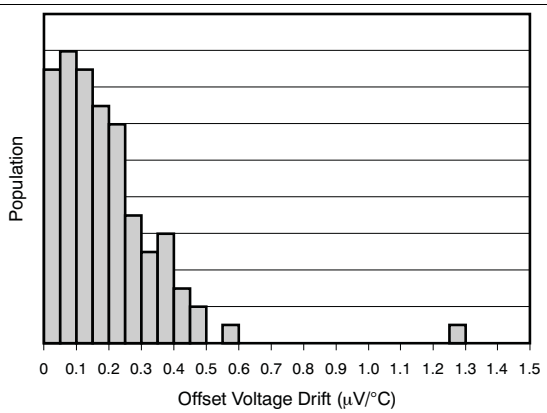


Figure 12. Offset Voltage Drift Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

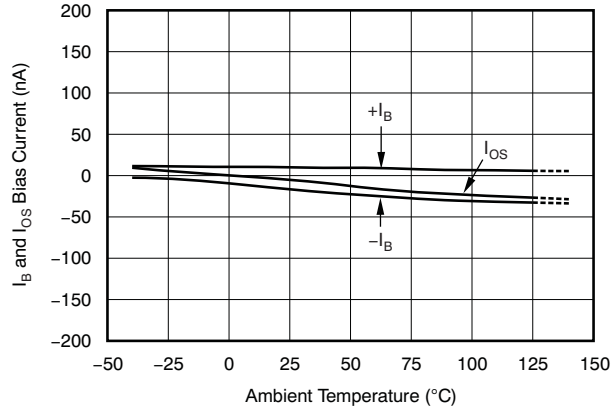


Figure 13. I_B and I_{OS} Current vs Temperature

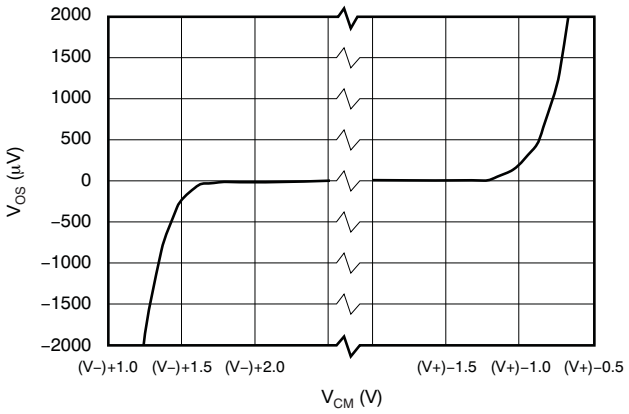


Figure 14. Offset Voltage vs Common-Mode Voltage

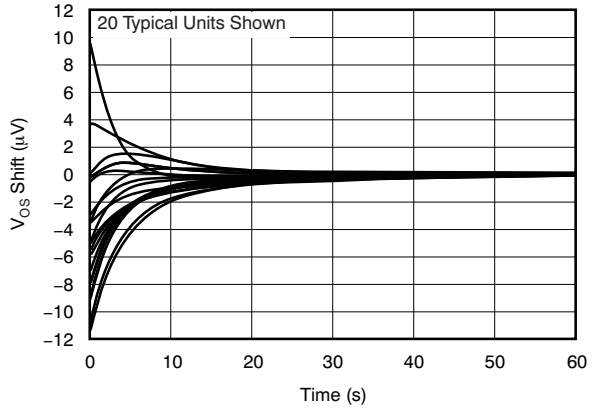


Figure 15. V_{OS} Warm-Up

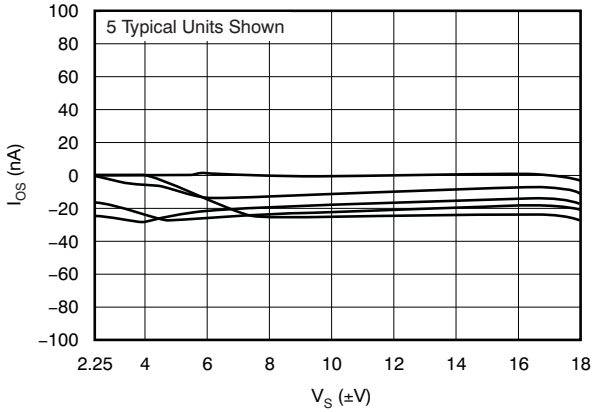


Figure 16. Input Offset Current vs Supply Voltage

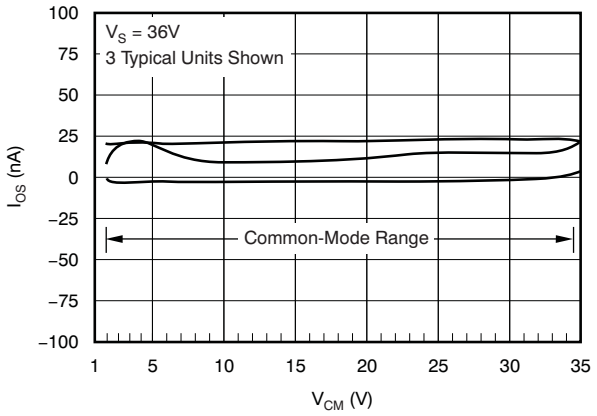


Figure 17. Input Offset Current vs Common-Mode Voltage

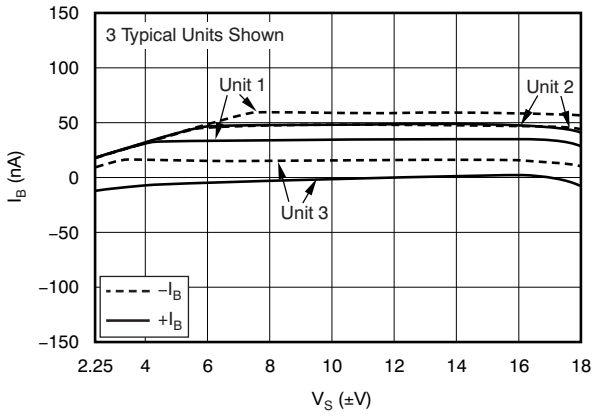


Figure 18. Input Bias Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

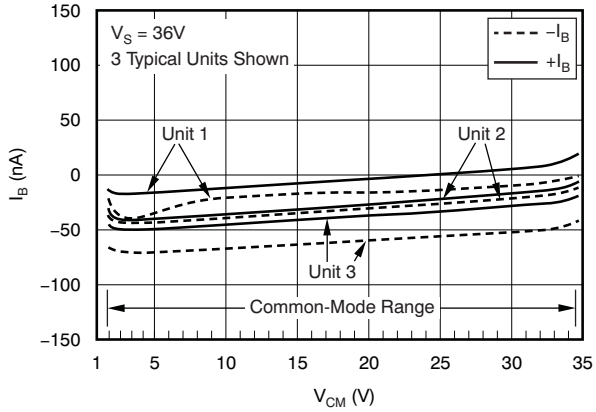


Figure 19. Input Bias Current vs Common-Mode Voltage

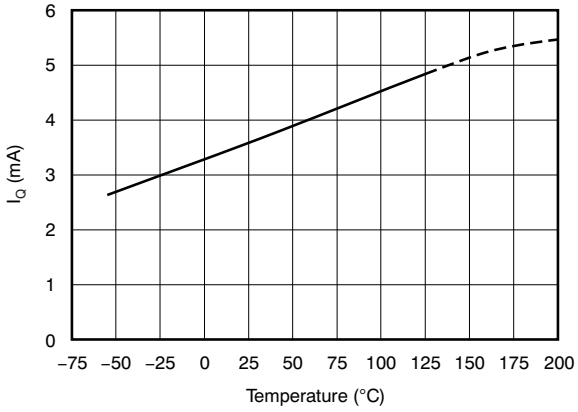


Figure 20. Quiescent Current vs Temperature

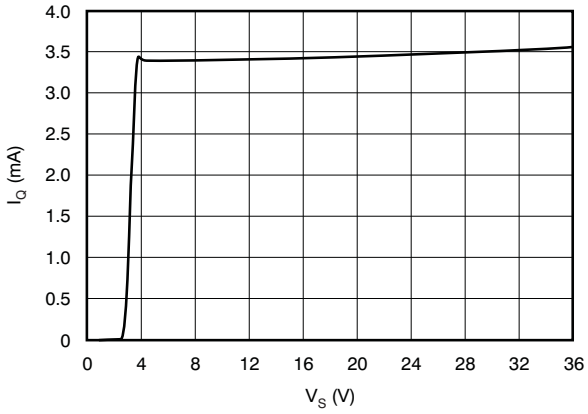


Figure 21. Quiescent Current vs Supply Voltage

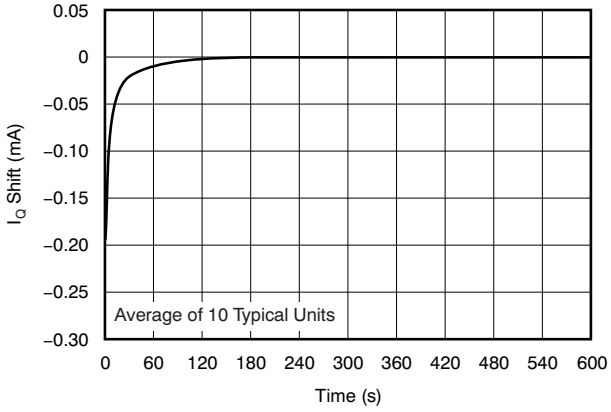


Figure 22. Normalized Quiescent Current vs Time

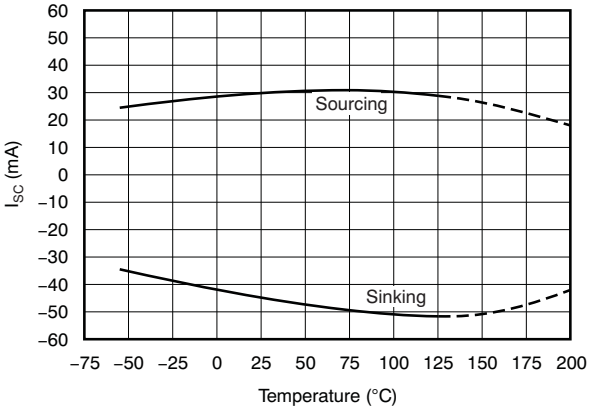


Figure 23. Short-Circuit Current vs Temperature

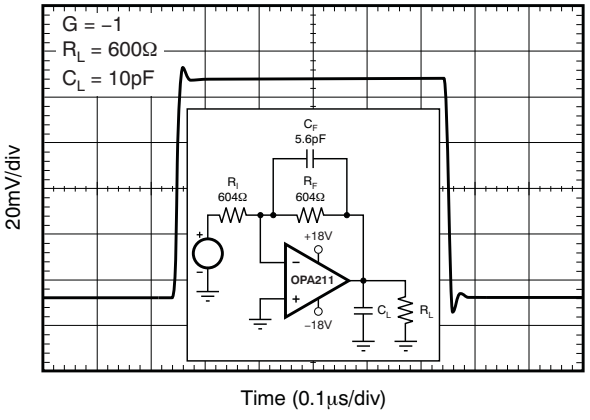


Figure 24. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

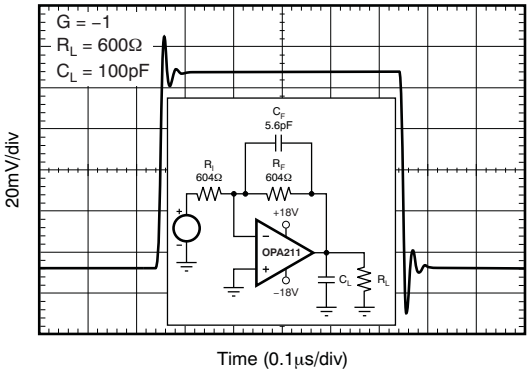


Figure 25. Small-Signal Step Response

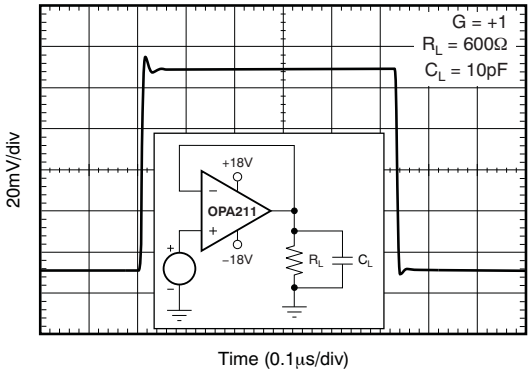


Figure 26. Small-Signal Step Response

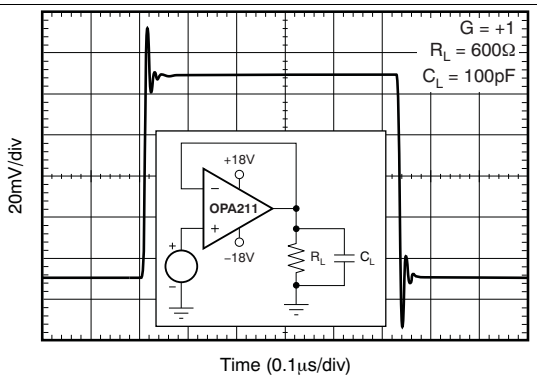


Figure 27. Small-Signal Step Response

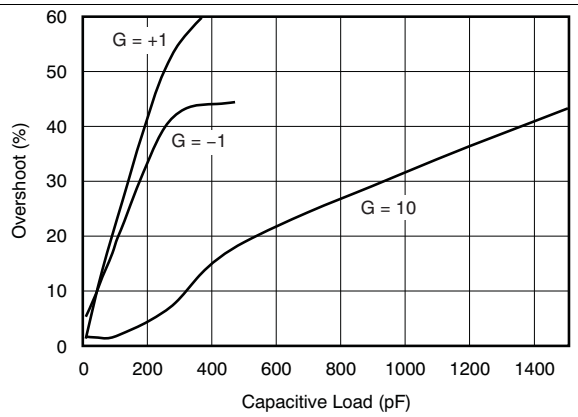


Figure 28. Small-Signal Overshoot vs Capacitive Load

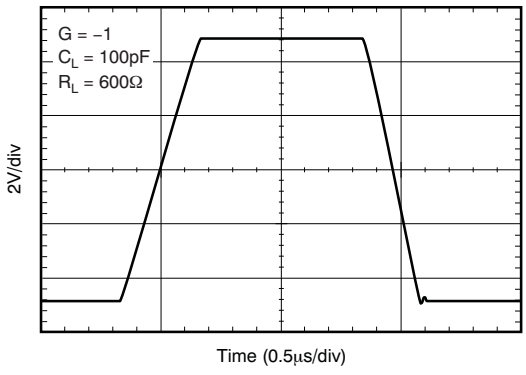


Figure 29. Large-Signal Step Response

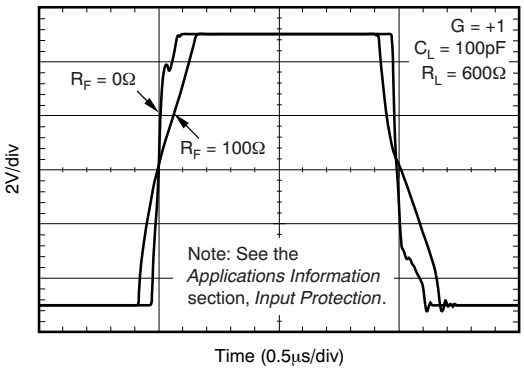
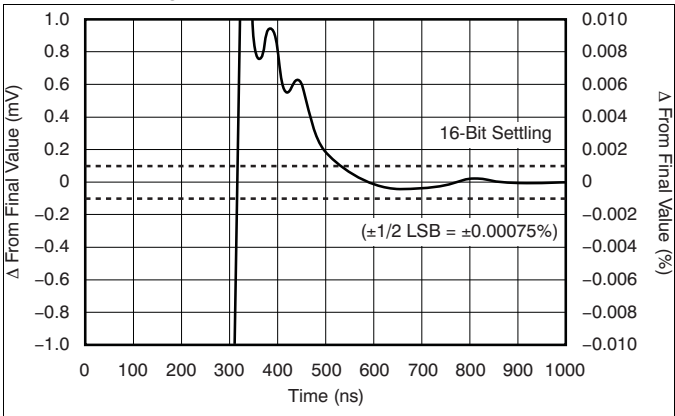


Figure 30. Large-Signal Step Response

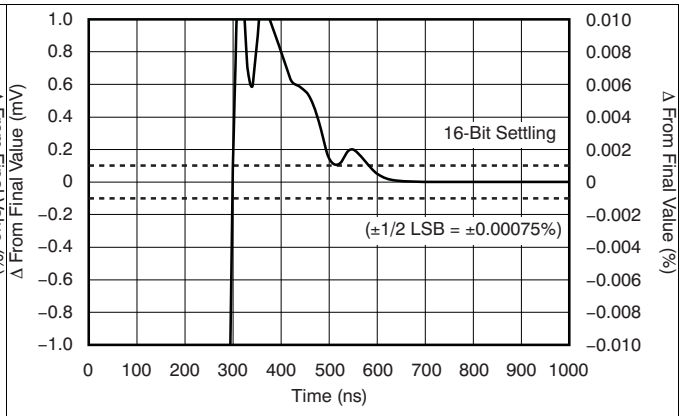
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.



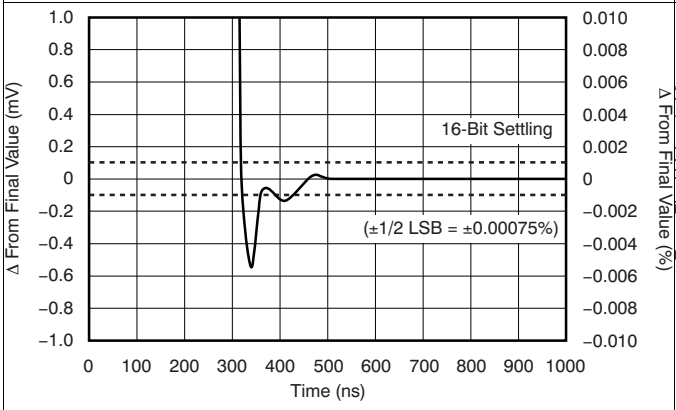
(10 V_{PP}, C_L = 100 pF)

Figure 31. Large-Signal Positive Settling Time



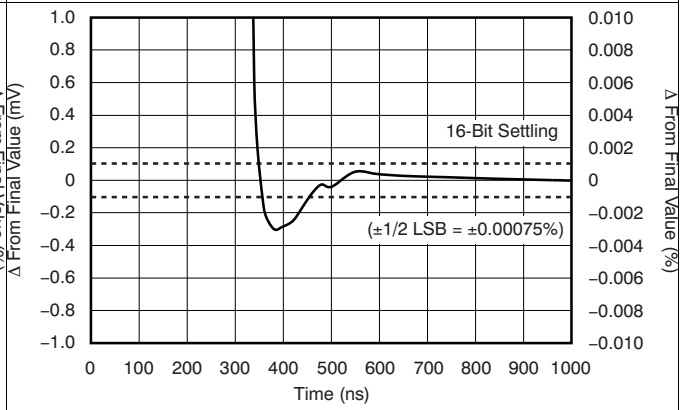
(10 V_{PP}, C_L = 10 pF)

Figure 32. Large-Signal Positive Settling Time



(10 V_{PP}, C_L = 100 pF)

Figure 33. Large-Signal Negative Settling Time



(10 V_{PP}, C_L = 10 pF)

Figure 34. Large-Signal Negative Settling Time

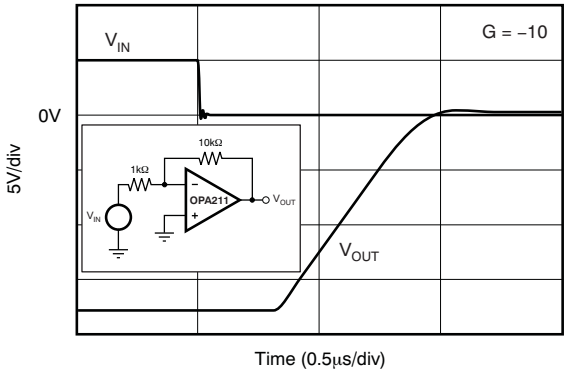


Figure 35. Negative Overload Recovery

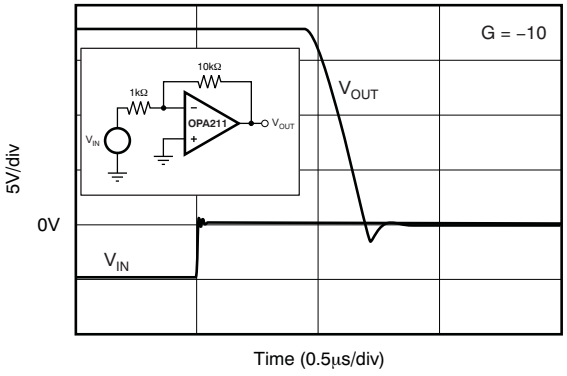


Figure 36. Positive Overload Recovery

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

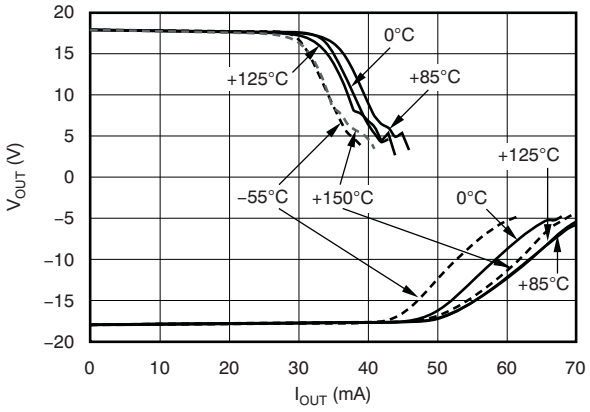


Figure 37. Output Voltage vs Output Current

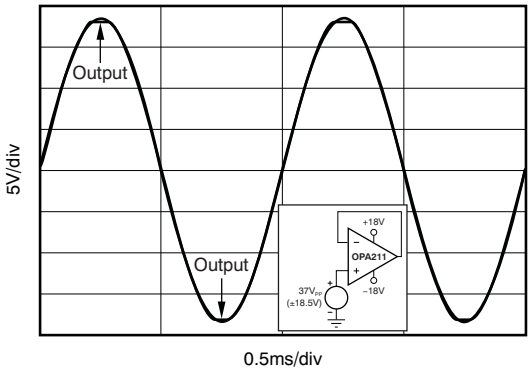


Figure 38. No Phase Reversal

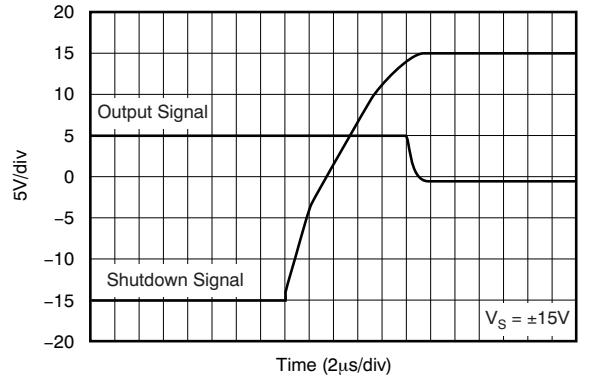


Figure 39. Turnoff Transient

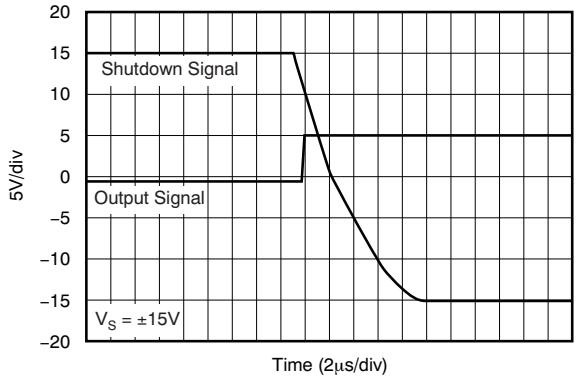


Figure 40. Turnon Transient

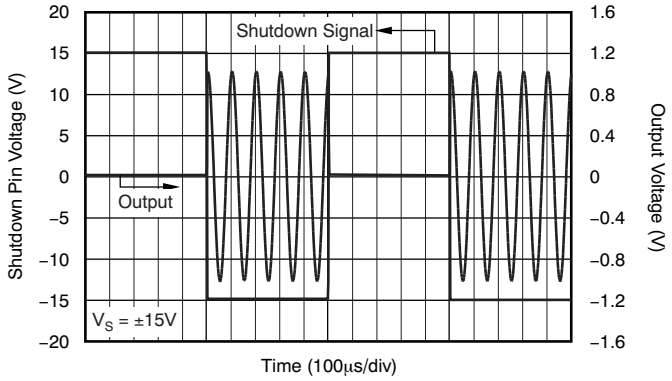


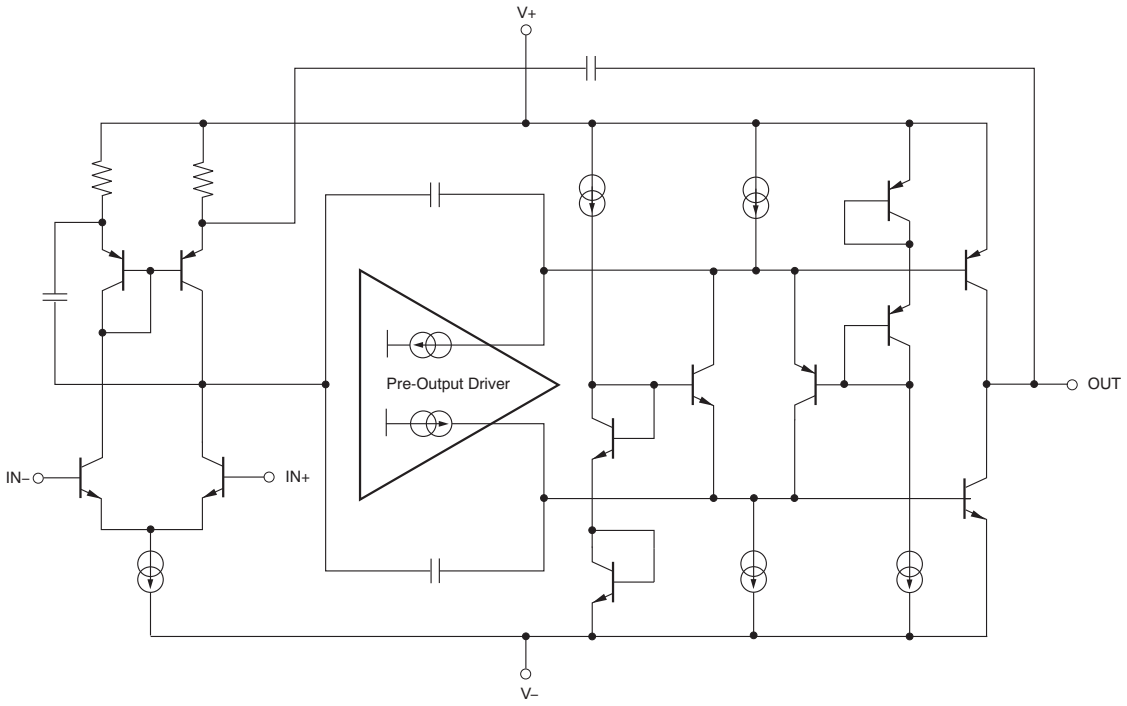
Figure 41. Turnon and Turnoff Transient

8 Detailed Description

8.1 Overview

The OPAx211 family of operational amplifiers are available in single-channel versions (OPA211) and dual-channel versions (OPA2211). Single-channel versions are available with and without shutdown. The OPAx211 family of operational amplifiers features ultra-low noise of 1.1-nV/√Hz, low total harmonic distortion + noise of 0.000015% and wide, rail-to-rail output swing. These unique features makes the OPAx211 family suitable for wide dynamic range applications and driving high-speed analog-to-digital converters. The OPAx211 family is protected against excessive differentially applied input voltages and is fully characterized for electromagnetic interference rejection ratio (EMIRR). The OPAx211 operates with as little as 4.5-V (±2.25-V) power supply voltage and with power supply voltages up to 36 V (±18 V). The OPAx211 family is specified to operate from –40°C to +125°C with little change in parametric behavior over the full temperature range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Total Harmonic Distortion Measurements

OPA211 series operational amplifiers have excellent distortion characteristics. THD + Noise is below 0.0001% (G = +1, V_O = 3 V_{RMS}) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-Ω load.

The distortion produced by OPA211 series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit shown in Figure 43 can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 43 shows a circuit that causes the operational amplifier distortion to be 101 times greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101.

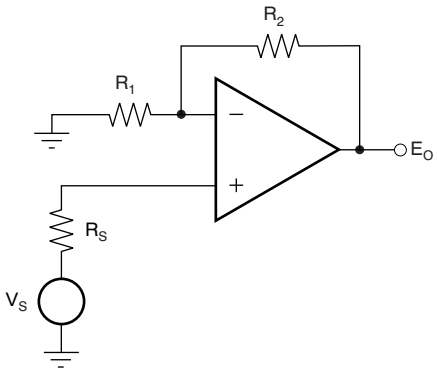
Feature Description (continued)

NOTE

The input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

Noise in Noninverting Gain Configuration



Noise at the output:

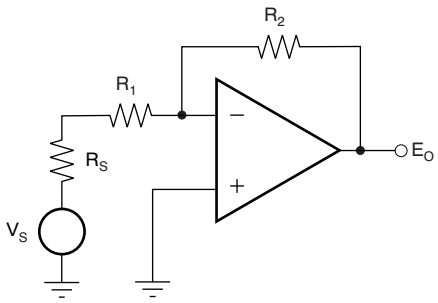
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

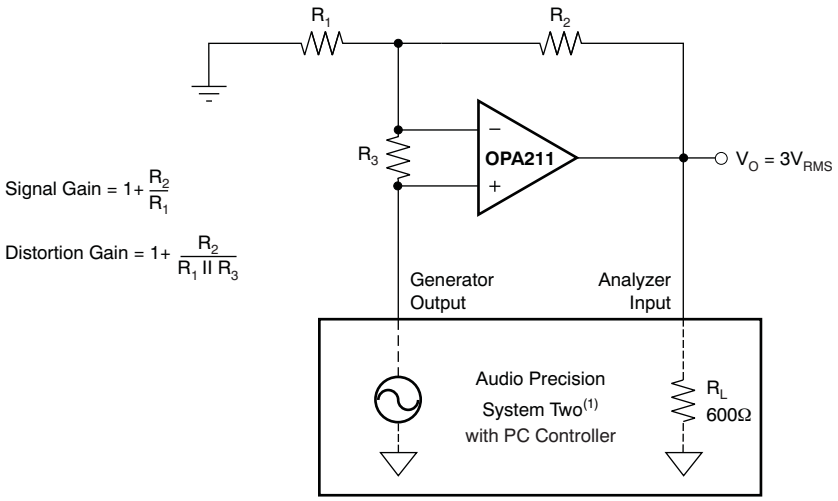
Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA211 series op amps at 1kHz, $e_n = 1.1nV/\sqrt{Hz}$ and $i_n = 1.7pA/\sqrt{Hz}$.

Figure 42. Noise Calculation in Gain Configurations



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

NOTE: (1) Measurement BW = 80kHz.

Figure 43. Distortion Test Circuit

8.4 Device Functional Modes

The OPAx211 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx211 is 36 V (±18 V).

8.4.1 Shutdown

The shutdown (enable) function of the OPA211 is referenced to the positive supply voltage of the operational amplifier. A valid high disables the operational amplifier. A valid high is defined as (V+) – 0.35 V of the positive supply applied to the shutdown pin. A valid low is defined as (V+) – 3 V below the positive supply pin. For example, with V_{CC} at ±15 V, the device is enabled at or below 12 V. The device is disabled at or above 14.65 V. If dual or split power supplies are used, care should be taken to ensure the valid high or valid low input signals are properly referred to the positive supply voltage. This pin must be connected to a valid high or low voltage or driven, and not left open-circuit. The enable and disable times are provided in the *Typical Characteristics* section (see Figure 39 through Figure 41). When disabled, the output assumes a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA211 and OPA2211 are unity-gain stable, precision operational amplifiers with very-low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

9.1.1 Operating Voltage

OPA211 series operational amplifiers operate from ±2.25- to ±18-V supplies while maintaining excellent performance. The OPA211 series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to 25 V with the negative supply at –5 V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

9.1.2 Input Protection

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 44. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is shown in Figure 30 of the *Typical Characteristics*. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA211, and is discussed in the *Noise Performance* section of this data sheet. Figure 44 shows an example implementing a current-limiting feedback resistor.

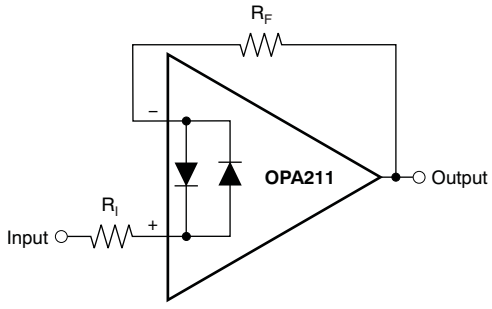


Figure 44. Pulsed Operation

Application Information (continued)

9.1.3 Noise Performance

Figure 45 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA211 has very low voltage noise, making it ideal for low source impedances (less than 2 kΩ). A similar precision operational amplifier, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 to 100 kΩ). Above 100 kΩ, a FET-input operational amplifier such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 45 is shown for the calculation of the total circuit noise.

NOTE

e_n = voltage noise, I_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K.

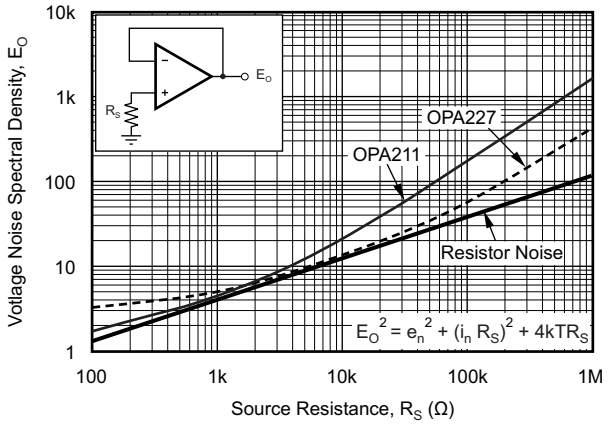


Figure 45. Noise Performance of the OPA211 and OPA227 in Unity-Gain Buffer Configuration

9.1.4 Basic Noise Calculations

Design of low-noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 45. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

Figure 45 depicts total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 42 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Application Information (continued)

9.1.5 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.Figure 46

The EMIRR IN+ of the OPA211 is plotted versus frequency as shown in Figure 46. If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA211 unity-gain bandwidth is 45 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers*, SBOA128, available for download from www.ti.com.

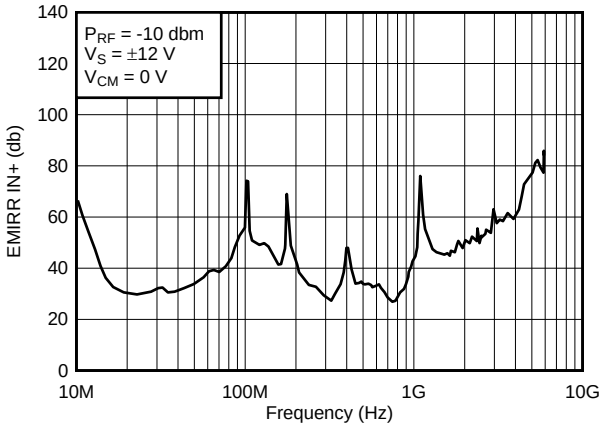


Figure 46. OPA211 EMIRR

Table 1 shows the EMIRR IN+ values for the OPA211 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA211 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48.4 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	34.6 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	46.0 dB

Application Information (continued)

Table 1. OPA211 EMIRR IN+ For Frequencies of Interest (continued)

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	56.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	61.5 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	76.7 dB

9.1.6 EMIRR +IN Test Configuration

Figure 47shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a lowpass filter (LPF) and a digital multimeter (DMM).

NOTE

A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter.

The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

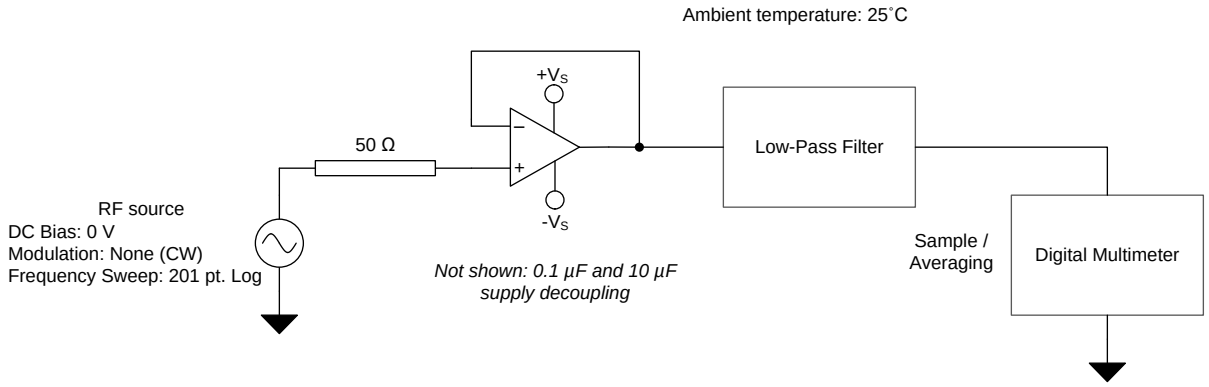


Figure 47. EMIRR +IN Test Configuration

9.1.7 Electrical Overstress

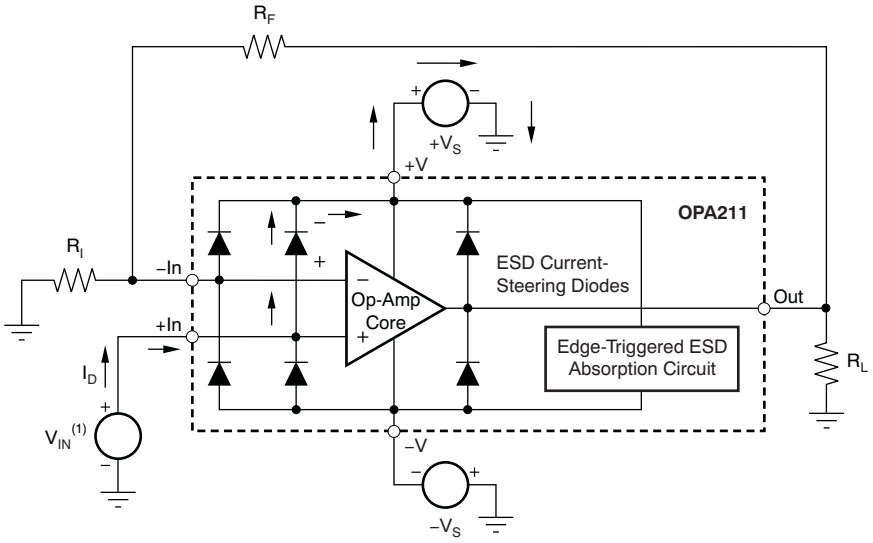
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 48 shows the ESD circuits contained in the OPA211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that shown in Figure 48, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1) $V_{IN} = +V_S + 500$ mV.

Figure 48. Equivalent Internal ESD Circuitry and its Relation to a Typical Circuit Application

Figure 48 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

9.2 Typical Application

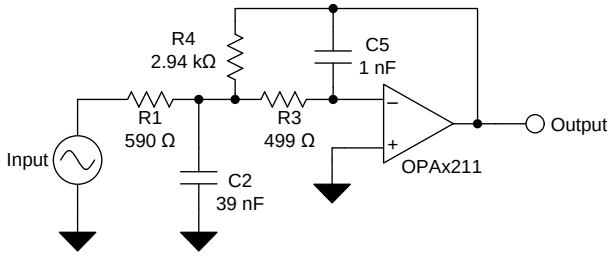


Figure 49. OPA211 Simplified Schematic

9.2.1 Design Requirements

Lowpass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx211 are ideally suited to construct high-speed, high-precision active filters. Figure 49 shows a second order lowpass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Lowpass cutoff frequency = 25 kHz
- Second order Chebyshev filter response with 3-dB gain peaking in the passband

9.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in . Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the lowpass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design.WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

Typical Application (continued)

9.2.3 Application Curve

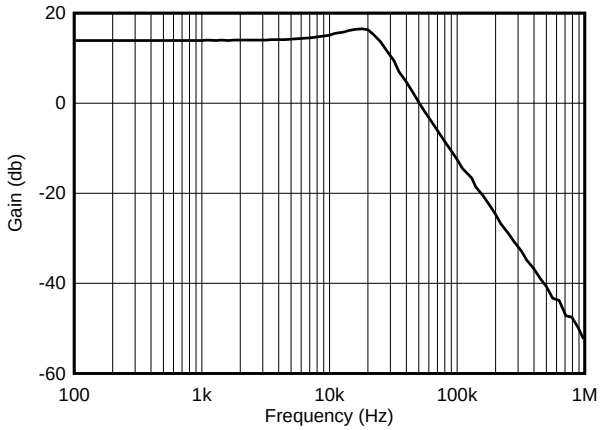


Figure 50. OPAx211 2nd-Order 25-kHz, Chebyshev, Lowpass Filter

10 Power Supply Recommendations

The OPAx211are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pick-up. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 51, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A

Layout Guidelines (continued)

low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.1.1 SON Layout Guidelines

The OPA211 is offered in an SON-8 package (also known as SON). The SON package is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

SON packages are physically small, and have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The SON package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note *QFN/SON PCB Attachment* (SLUA271) and application report *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

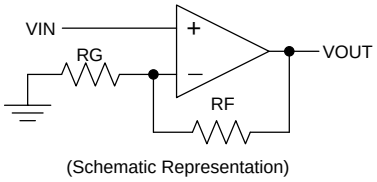
NOTE

The exposed leadframe die pad on the bottom of the package must be connected to V–. Soldering the thermal pad improves heat dissipation and enables specified device performance.

The exposed leadframe die pad on the SON package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

11.2 Layout Example



(Schematic Representation)

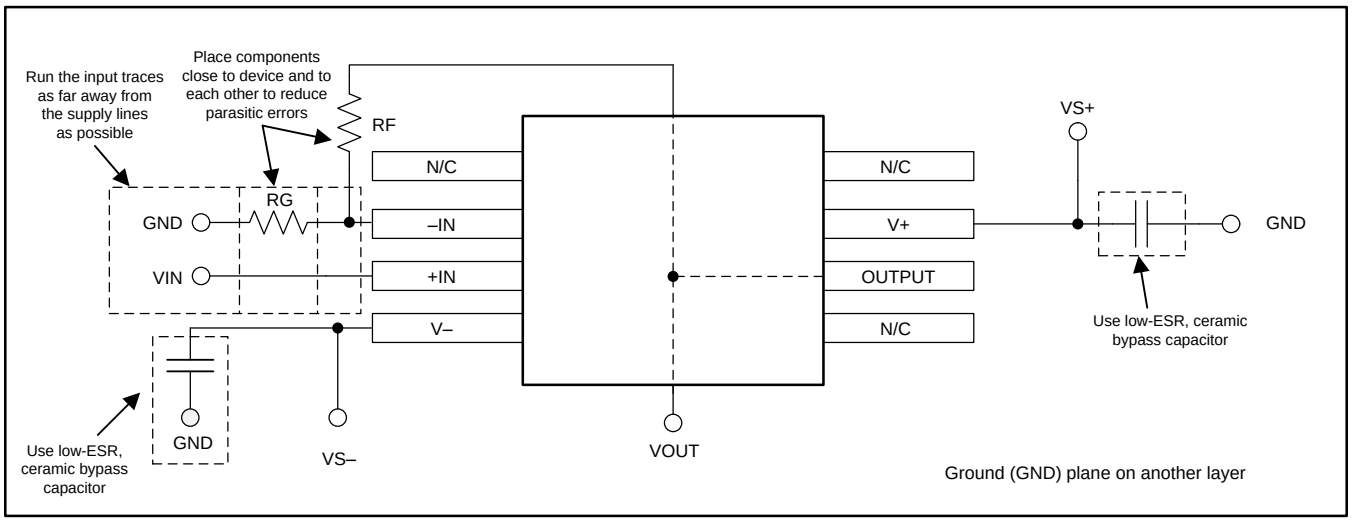


Figure 51. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 TI Precision Designs

The OPAx211 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see:

Circuit Board Layout Techniques, SLOA089.

Op Amps for Everyone, SLOD006.

OPA211, OPA211A, OP2211, OPA2211A EMI Immunity Performance (Rev. A), SBOZ021.

Operational amplifier gain stability, Part 3: AC gain-error analysis, SLYT383.

Operational amplifier gain stability, Part 2: DC gain-error analysis, SLYT374.

Using infinite-gain, MFB filter topology in fully differential active filters, SLYT343.

Op Amp Performance Analysis, SBOS054.

Single-Supply Operation of Operational Amplifiers, SBOA059.

Tuning in Amplifiers, SBOA067.

Shelf-Life Evaluation of Lead-Free Component Finishes, SZZA046.

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA211	Click here	Click here	Click here	Click here	Click here
OPA2211	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, TINA-TI, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA211AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	Samples
OPA211AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	Samples
OPA211AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	Samples
OPA211AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	Samples
OPA211AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBCQ	Samples
OPA211AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	Samples
OPA211AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	Samples
OPA211AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	Samples
OPA211AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	Samples
OPA211AIDRGTG4	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	Samples
OPA211ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211	Samples
OPA211IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	Samples
OPA211IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	Samples
OPA211IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211	Samples
OPA211IDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA211IDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	Samples
OPA2211AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A	Samples
OPA2211AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A	Samples
OPA2211AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ	Samples
OPA2211AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA211 :

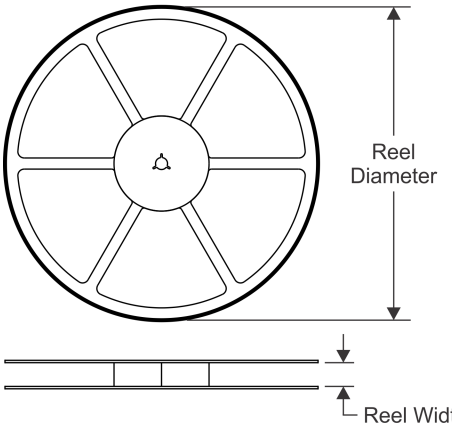
- Enhanced Product: OPA211-EP

NOTE: Qualified Version Definitions:

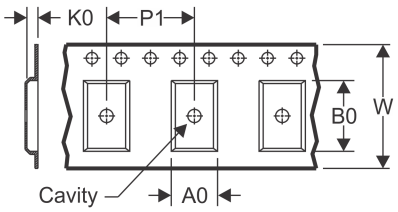
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

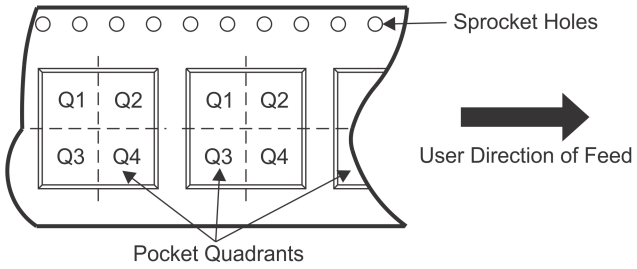


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

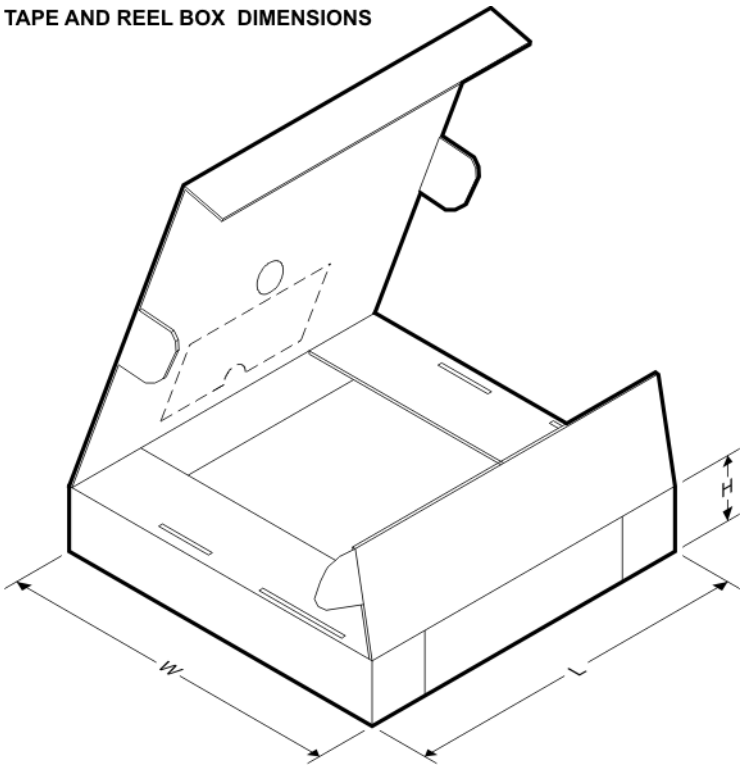
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA211AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA211AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA211IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2211AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2211AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2211AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

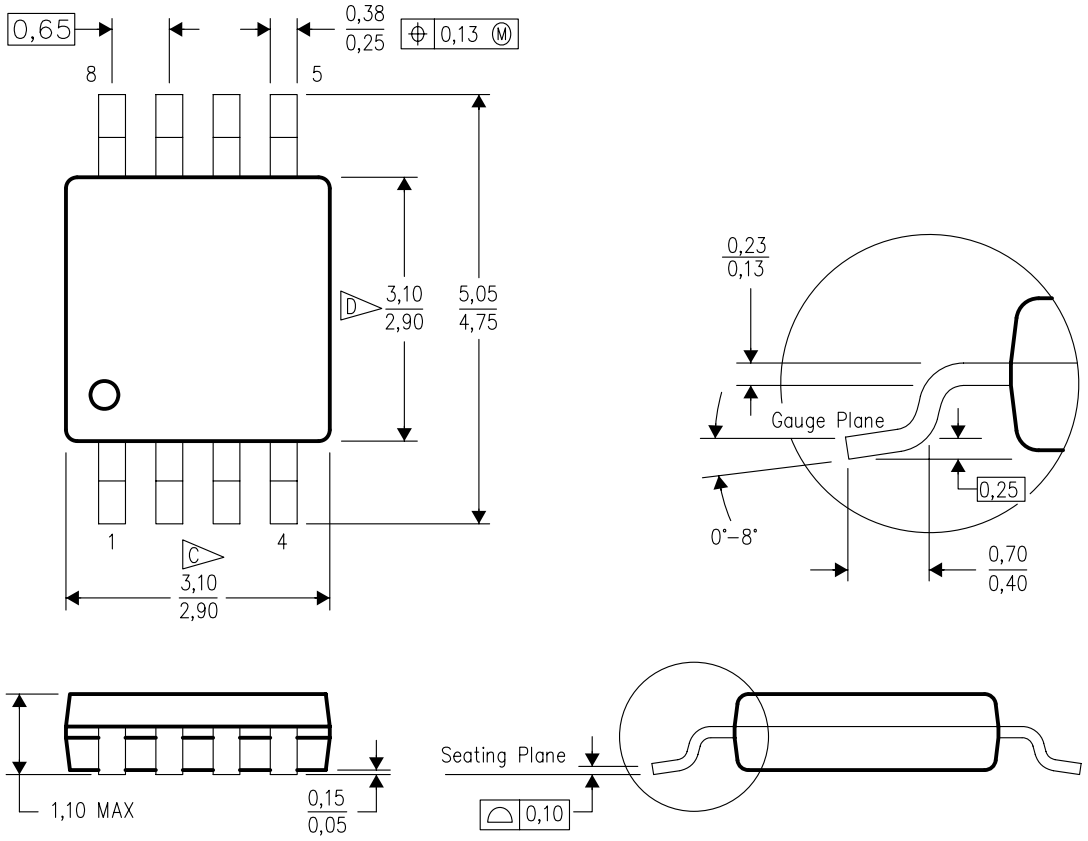
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA211AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA211AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA211AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA211AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA211AIDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA211IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA211IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA211IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA211IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA211IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA2211AIDDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA2211AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2211AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

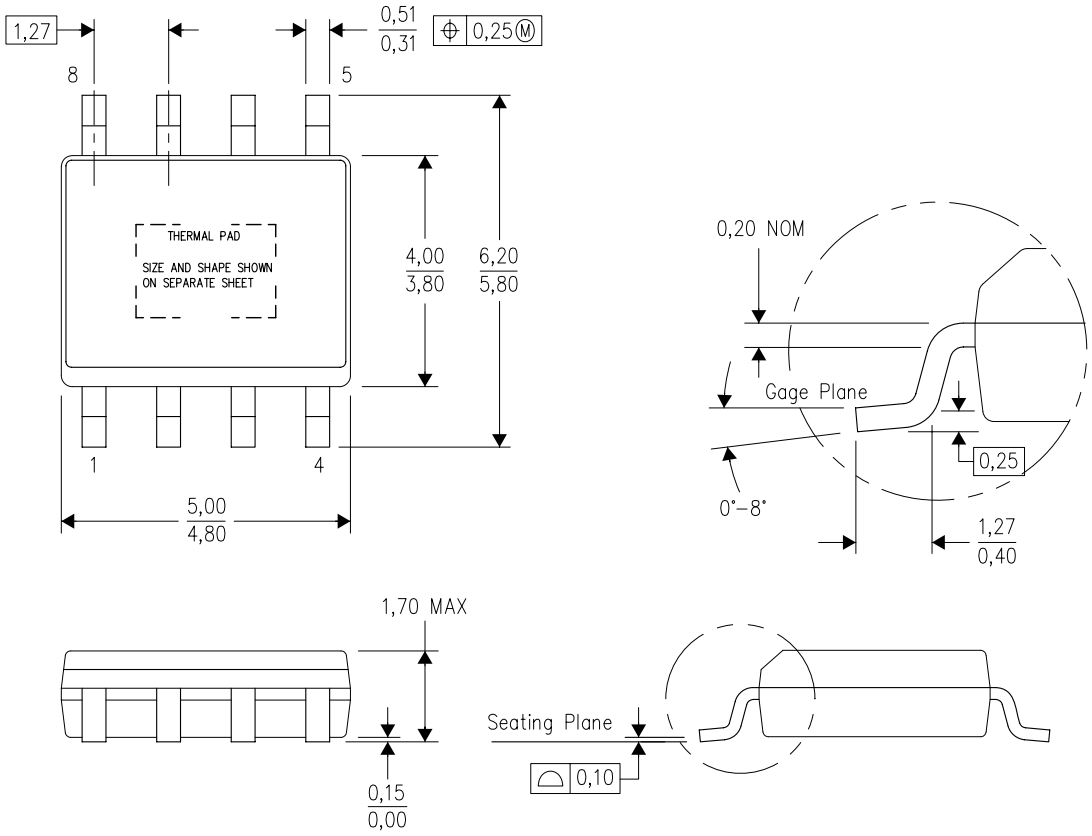
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

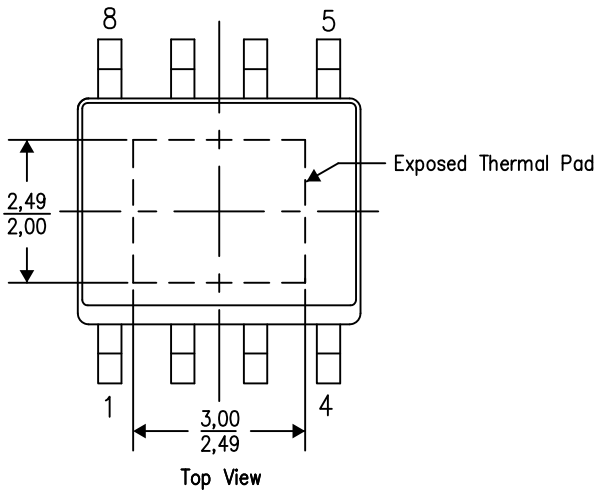
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



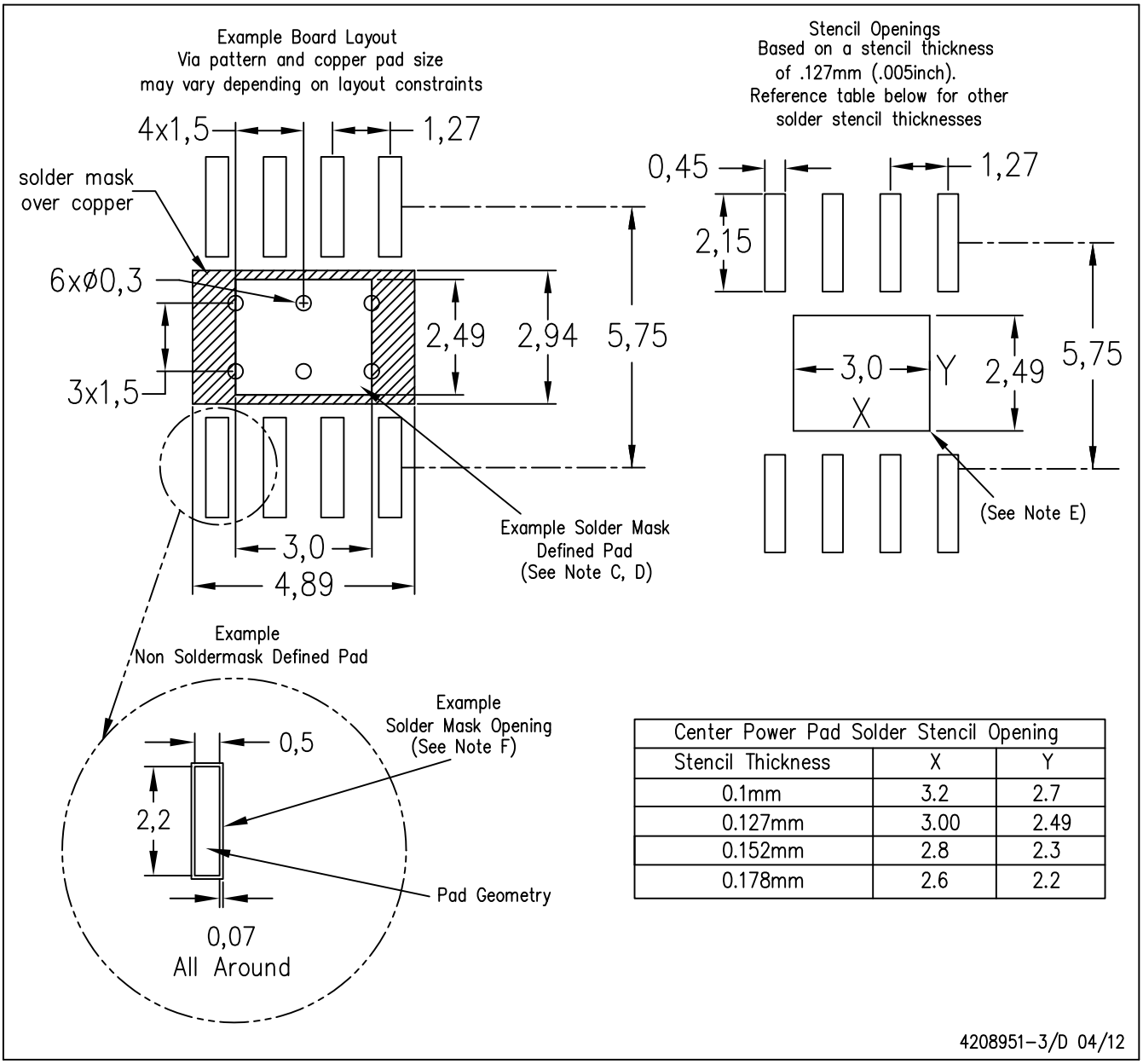
Exposed Thermal Pad Dimensions

4206322–3/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

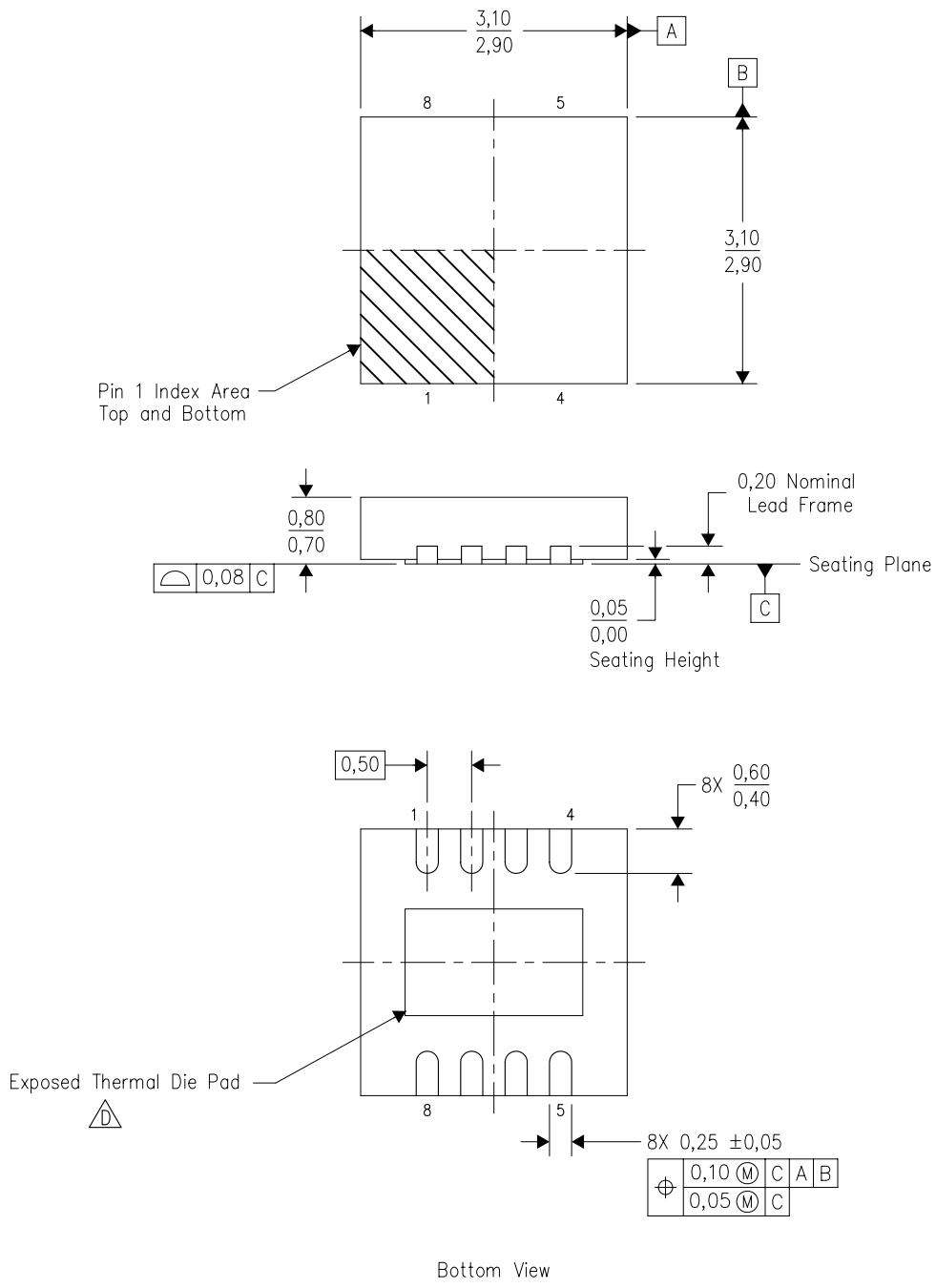
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	2.7
0.127mm	3.00	2.49
0.152mm	2.8	2.3
0.178mm	2.6	2.2

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

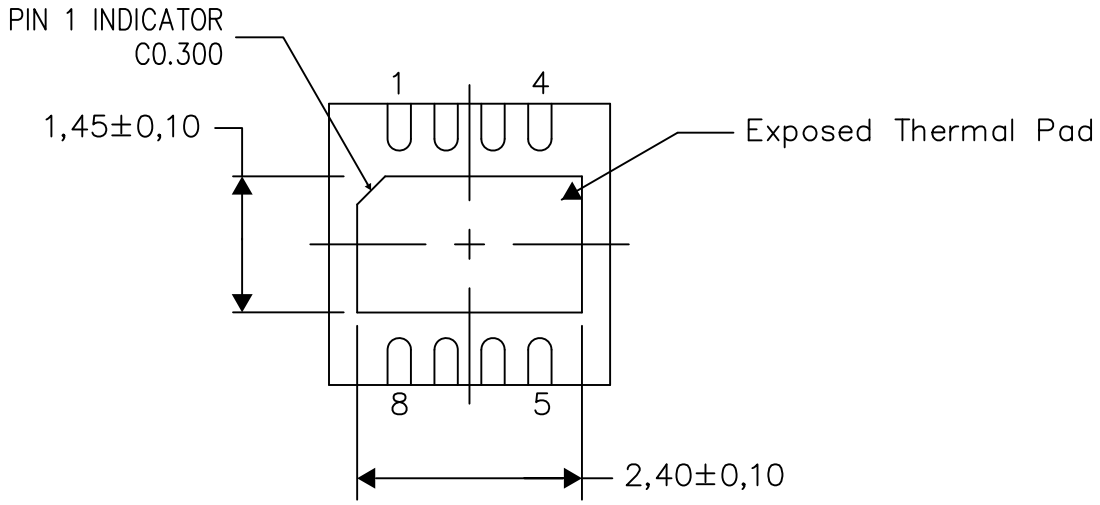
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



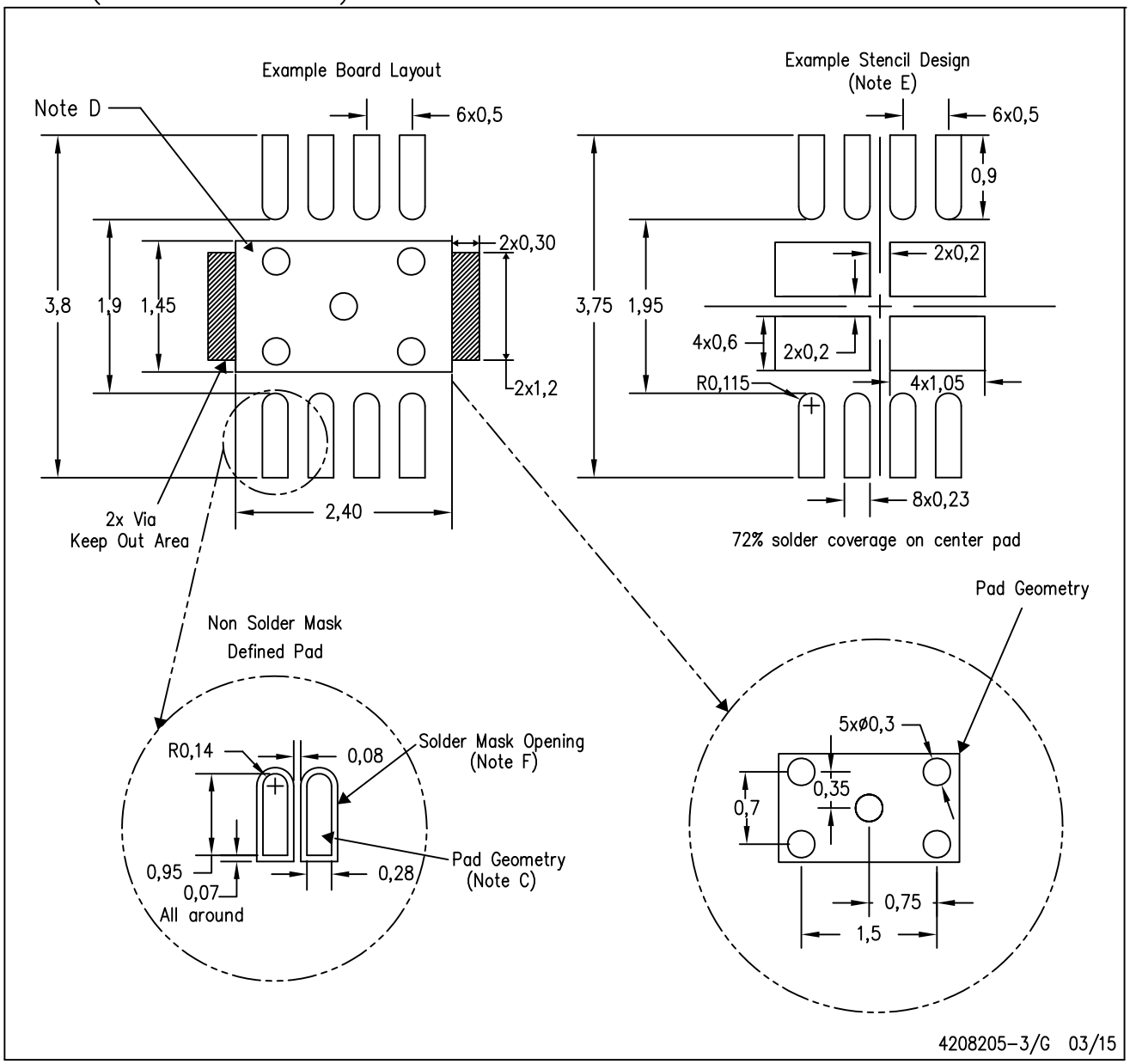
Bottom View

Exposed Thermal Pad Dimensions

4206881–3/I 03/15

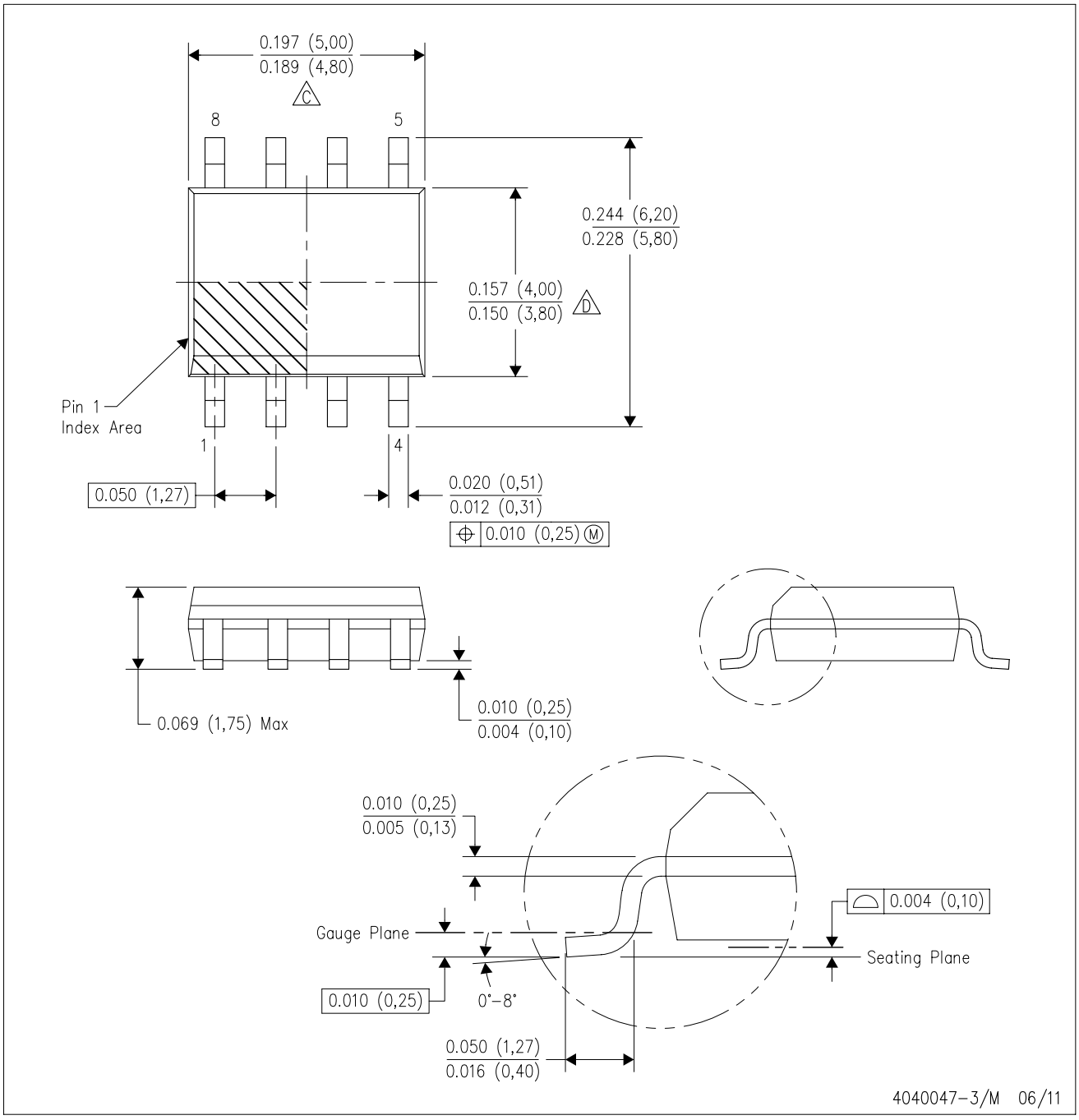
NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



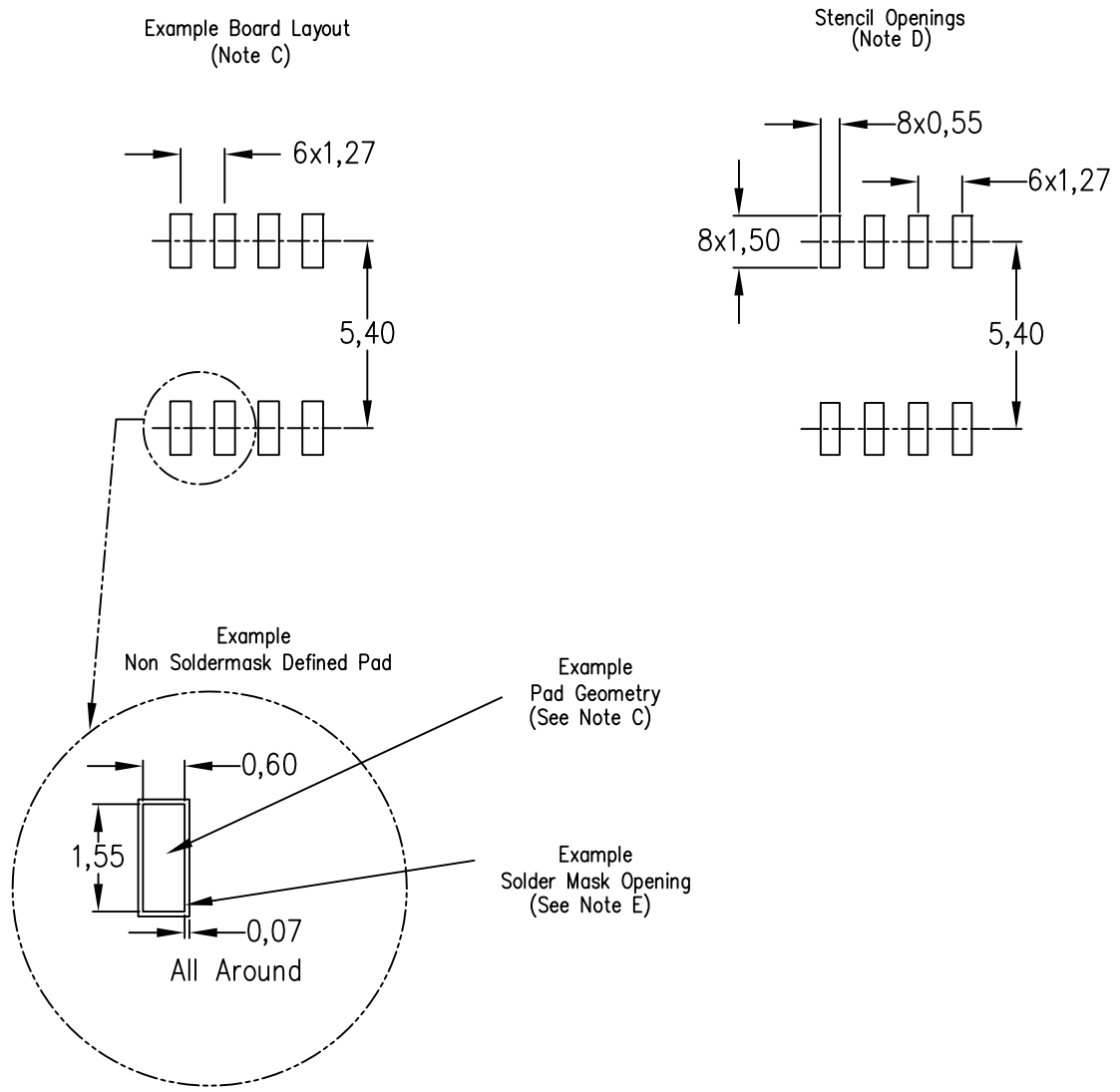
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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