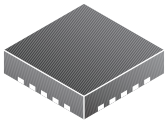


16-Bit, Low-Power Stereo Audio DAC With Analog Mixing, Line and Headphone Outputs

FEATURES

- **Analog Front End:**
  - **Stereo Single-Ended Input**
  - **Microphone Amplifier (12 dB, 20 dB)**
- **Analog Back End:**
  - **Stereo/Mono Line Output With Volume**
  - **Stereo/Mono Headphone Amplifier With Volume**
- **Analog Performance:**
  - **Dynamic Range: 93 dB**
  - **40-mW + 40-mW Headphone Output at R_L = 16 Ω**
- **Power Supply Voltage**
  - **1.71 V to 3.6 V for Digital I/O Section**
  - **1.71 V to 3.6 V for Digital Core Section**
  - **2.4 V to 3.6 V for Analog Section**
  - **2.4 V to 3.6 V for Power Amplifier Section**
- **Low Power Dissipation:**
  - **6.4 mW in Playback, 1.8 V/2.4 V, 44.1 kHz**
  - **3.3 µW in Power Down**
- **Sampling Frequency: 5 kHz to 50 kHz**
- **Operation From a Single Clock Input Without PLL**
- **System Clock:**
  - **Common-Audio Clock (256 f_S/384 f_S), 12/24, 13/26, 13.5/27, 19.2/38.4, 19.68/39.36 MHz**
- **2 (I^2C™) or 3 (SPI) Wire Serial Control**
- **Programmable Function by Register Control:**
- **Digital Attenuation: 0 dB to –62 dB**
- **Digital Gain of DAC: 0, 6, 12, 18 dB**
- **Power Up/Down Control for Each Module**
- **6-dB to –70-dB Gain for Analog Outputs**
- **0/12/20 dB for Microphone Input**
- **0-dB to –21-dB Gain for Analog Mixing**
- **Three-Band Tone Control and 3D Sound**
- **Analog Mixing Control**
- **Pop-Noise Reduction Circuit**
- **Short Protection Circuit**
- **Package: 4-mm × 4-mm QFN Package**
- **Operation Temperature Range: –40°C to 85°C**

APPLICATIONS

- **Portable Audio Player, Cellular Phone**
- **Video Camcorder, Digital Still Camera**
- **PMP/DMB/PND**

DESCRIPTION

The PCM1774 is a low-power stereo DAC designed for portable digital audio applications. The device integrates headphone amplifier, line amplifier, line input, boost amplifier, programmable gain control, analog mixing, and sound effects. It is available in a small-footprint, 4-mm × 4-mm QFN package. The PCM1774 supports right-justified, left-justified, I^2S, and DSP formats, providing easy interfacing to audio DSP and decoder/encoder chips. Sampling rates up to 50 kHz are supported. The user-programmable functions are accessible through a two- or three-wire serial control port.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MAX	UNIT
Supply voltage	V_{DD}, V_{IO}, V_{CC}, V_{PA}	–0.3 to 4	V
Ground voltage differences: DGND, AGND, PGND		±0.1	V
Input voltage		–0.3 to 4	V
Input current (any pin except supplies)		±10	mA
Ambient temperature under bias		–40 to 110	°C
Storage temperature		–55 to 150	°C
Junction temperature		150	°C
Lead temperature (soldering)		260	°C, 5 s
Package temperature (reflow, peak)		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{SS}	Analog supply voltage, V_{CC}, V_{PA}		2.4	3.3	3.6	V
	Digital supply voltage, V_{DD}, V_{IO}		1.71	3.3	3.6	V
	Digital input logic family			CMOS		
	Digital input clock frequency	SCKI system clock	3.072		18.432	MHz
		LRCK sampling clock	8		48	kHz
	Analog output load resistance	LOL and LOR	10			kΩ
		HPOL and HPOR	16			Ω
	Analog output load capacitance				30	pF
	Digital output load capacitance				10	pF
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 16-bit data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Characteristics						
DATA FORMAT						
	Resolution			16		Bits
	Audio data interface format			I^2S, left-, right-justified, DSP		
	Audio data bit length			16		Bits
	Audio data format			MSB first, 2s complement		
	Sampling frequency (f_S)		5		50	kHz
	System clock	V_{DD} < 2 V			27	MHz
		V_{DD} > 2 V			40	
Digital Input/Output						
	Logic family			CMOS compatible		
V_{IH}	Input logic level		0.7 V_{IO}			Vdc
V_{IL}					0.3 V_{IO}	
I_{IH}	Input logic current	V_{IN} = 3.3 V			10	μA
I_{IL}		V_{IN} = 0 V			–10	
V_{OH}	Output logic level	I_{OH} = –2 mA	0.75 V_{IO}			Vdc
V_{OL}		I_{OL} = 2 mA			0.25 V_{IO}	
Digital Input to Line Output Through DAC (LOL and LOR)						
R_L = 10 kΩ, volume = 0 dB, analog mixing = disabled						
DYNAMIC PERFORMANCE						
	Full-scale output voltage	0 dB		2.828		V_{PP}
				1		Vrms
	Dynamic range	EIAJ, A-weighted		93		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	86	93		dB
	Channel separation			91		dB
THD+N	Total harmonic distortion + noise	0 dB		0.008%		
	Load resistance		10			kΩ
Line Input to Line Output Through Mixing Path (LOL and LOR)						
R_L = 10 kΩ, volume = 0 dB, analog mixing = enabled						
DYNAMIC PERFORMANCE						
	Full-scale input and output voltage	0 dB		2.828		V_{PP}
				1		Vrms
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB
Digital Input to Headphone Output Through DAC (HPOL and HPOR)						
R_L = 16 Ω or 32 Ω, ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = disabled, not capless mode						
DYNAMIC PERFORMANCE						
	Full-scale output voltage	0 dB		2.828		V_{PP}
				1		Vrms
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB
THD+N	Total harmonic distortion + noise	30 mW, R_L = 32 Ω, volume = 0 dB		0.1%		
		40 mW, R_L = 16 Ω, volume = –1 dB		0.03%		

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 16-bit data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Load resistance		16			Ω
PSRR	Power-supply rejection ratio	200 Hz, 140 mV_{PP}		–40		dB
		1 kHz, 140 mV_{PP}		–45		
		20 kHz, 140 mV_{PP}		–32		
Line Input to Headphone Output Through Mixing Path (HPOL and HPOR)						
R_L = 16 Ω or 32 Ω, ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = enabled, not capless mode						
DYNAMIC PERFORMANCE						
	Full-scale output voltage	0 dB		2.828		V_{PP}
				1		Vrms
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB
	Load resistance		16			Ω
Filter Characteristics						
INTERPOLATION FILTER FOR DAC						
	Pass band				0.454 f_S	
	Stop band		0.546 f_S			
	Pass-band ripple				±0.04	dB
	Stop-band attenuation		–50			dB
	Group delay			19/f_S		s
	De-emphasis error			±0.1		dB
ANALOG FILTER						
	Frequency response	f = 20 kHz		±0.2		dB
Power Supply and Supply Current						
V_{IO}	Voltage range		1.71	3.3	3.6	Vdc
V_{DD}			1.71	3.3	3.6	
V_{CC}			2.4	3.3	3.6	
V_{PA}			2.4	3.3	3.6	
	Supply current	BPZ input, all active, no load		4.5	10	mA
		All inputs are held static		1	10	μA
	Power dissipation	BPZ input		14.8	33	mW
		All inputs are held static		3.3	33	μW
Temperature Condition						
	Operation temperature		–40		85	°C
$θ_{JA}$	Thermal resistance			40		°C/W

PIN ASSIGNMENTS

PCM1774RGP
(TOP VIEW)

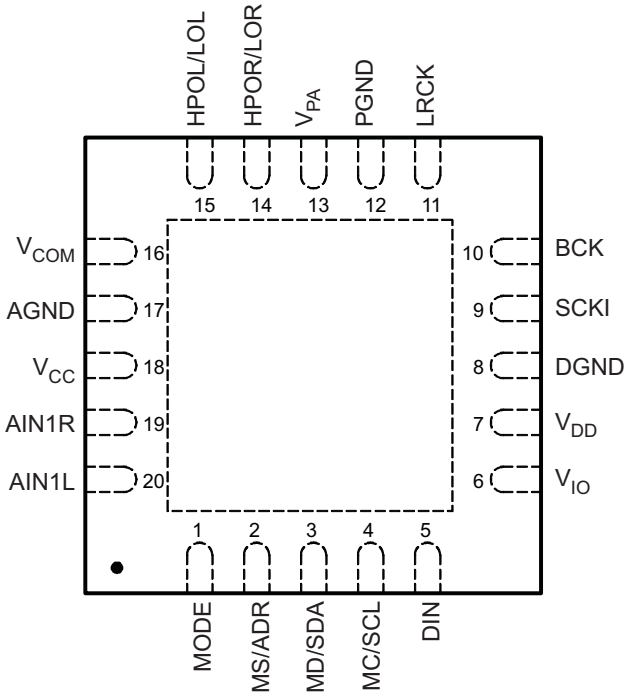
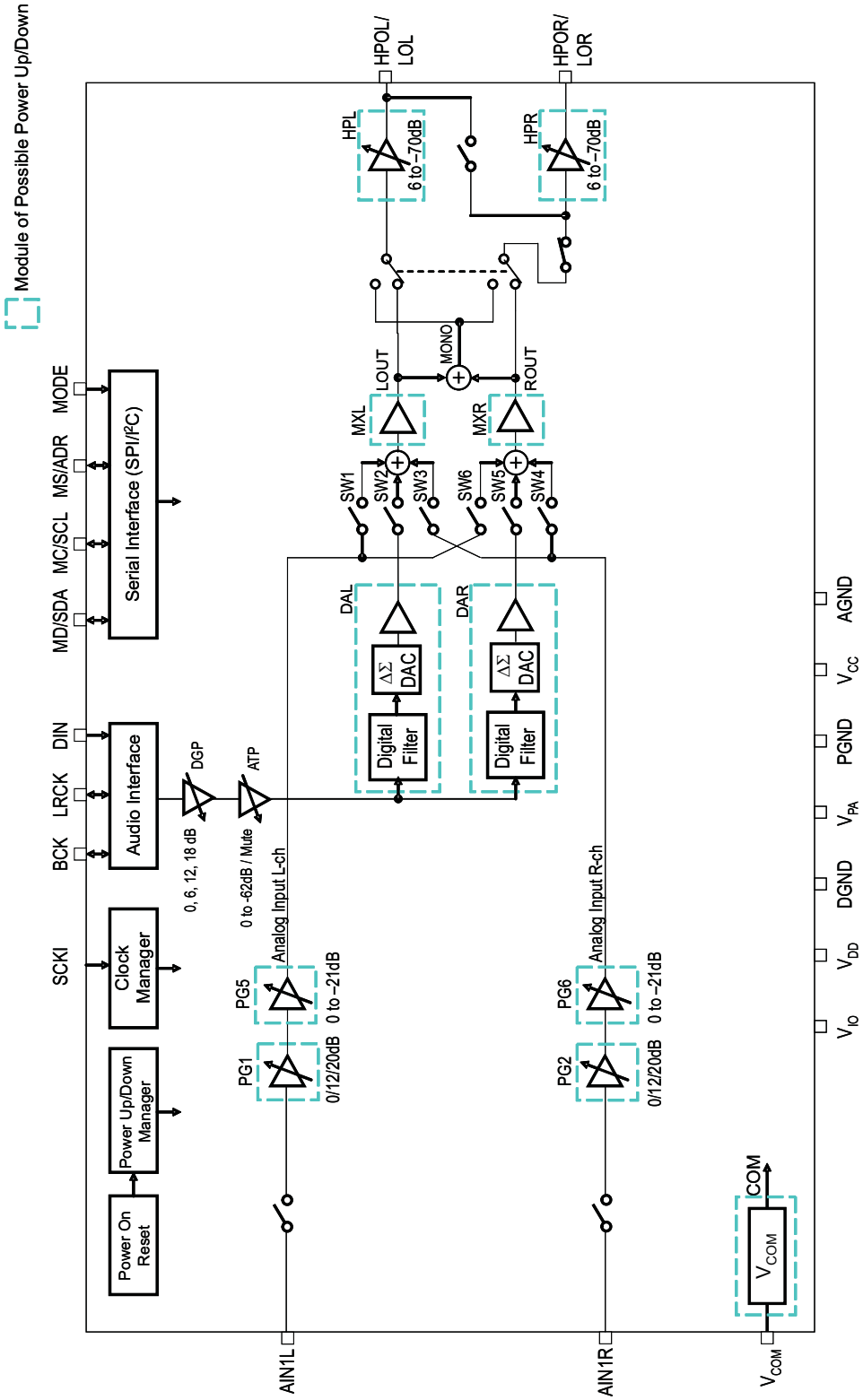


Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	17	–	Ground for analog
AIN1L	20	I	Analog input 1 for L-channel
AIN1R	19	I	Analog input 1 for R-channel
BCK	10	I/O	Serial bit clock
DGND	8	–	Digital ground
DIN	5	I	Serial audio data input
HPOL/LOL	15	O	Headphone/lineout for R-channel
HPOR/LOR	14	O	Headphone/lineout for L-channel
LRCK	11	I/O	Left and right channel clock
MC/SCL	4	I	Mode control clock for three-wire/two-wire interface
MD/SDA	3	I/O	Mode control data for three-wire/two-wire interface
MODE	1	I	Two- or three-wire interface selection (LOW: SPI, HIGH: I^2C)
MS/ADR	2	I	Mode control select for three-wire/two-wire interface
PGND	12	–	Ground for speaker power amplifier
SCKI	9	I	System clock
V_{CC}	18	–	Analog power supply
V_{COM}	16	–	Analog common voltage
V_{DD}	7	–	Power supply for digital core
V_{IO}	6	–	Power supply for digital I/O
V_{PA}	13	–	Power supply for power amplifier

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 16-bit data, unless otherwise noted.

INTERPOLATION FILTER, STOP BAND

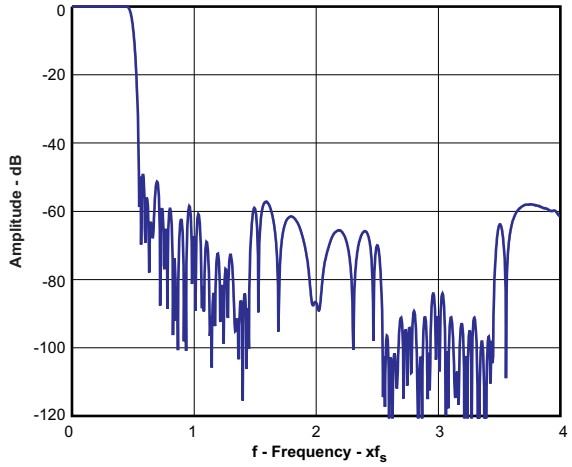


Figure 1.

INTERPOLATION FILTER, PASS BAND

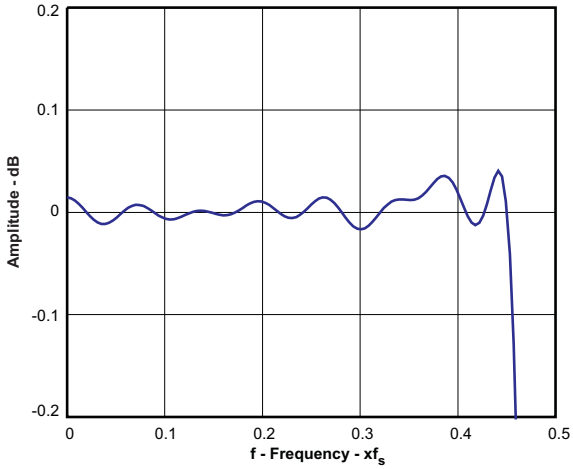


Figure 2.

THREE-BAND TONE CONTROL (BASS, MIDRANGE, TREBLE)

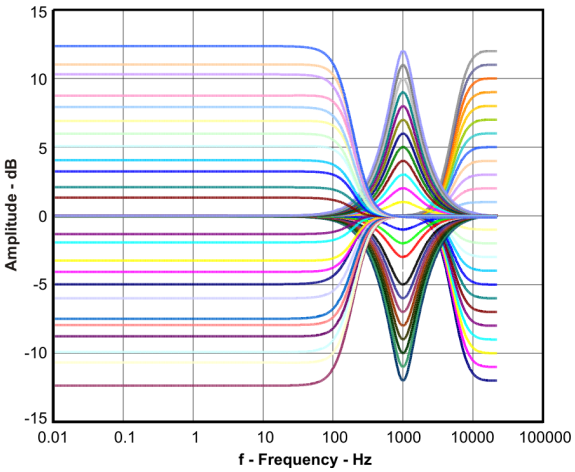


Figure 3.

THREE-BAND TONE CONTROL (BASS)

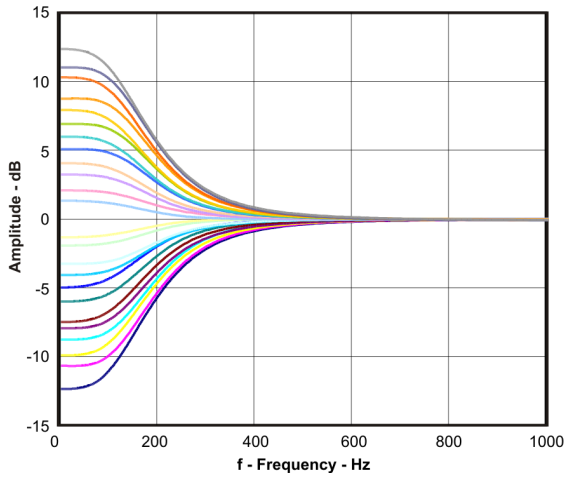


Figure 4.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 16-bit data, unless otherwise noted.

THREE-BAND TONE CONTROL (MIDRANGE)

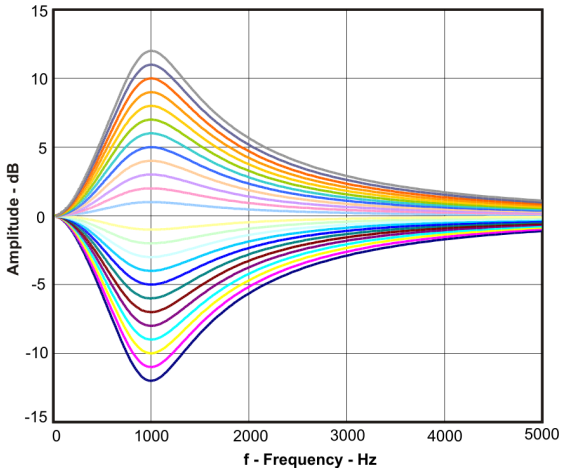


Figure 5.

THREE-BAND TONE CONTROL (TREBLE)

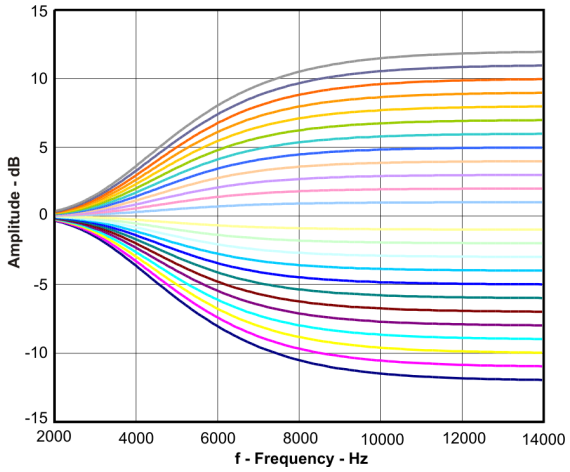


Figure 6.

THD+N/SNR vs POWER SUPPLY
DAC TO HEADPHONE OUTPUT, 16-Ω

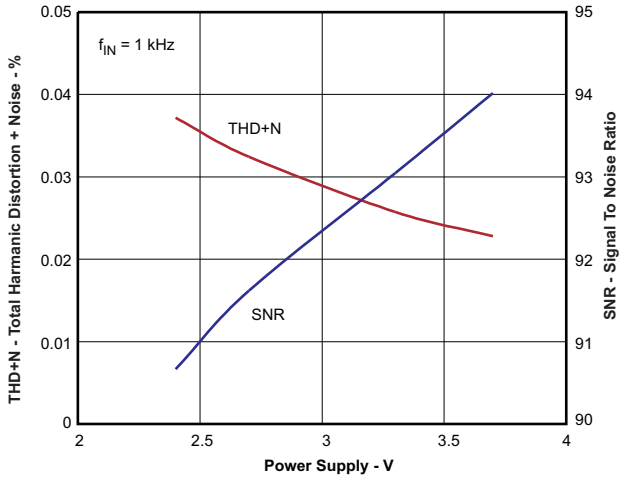


Figure 7.

THD+N/SNR vs POWER SUPPLY
DAC TO LINE OUTPUT, 10-kΩ

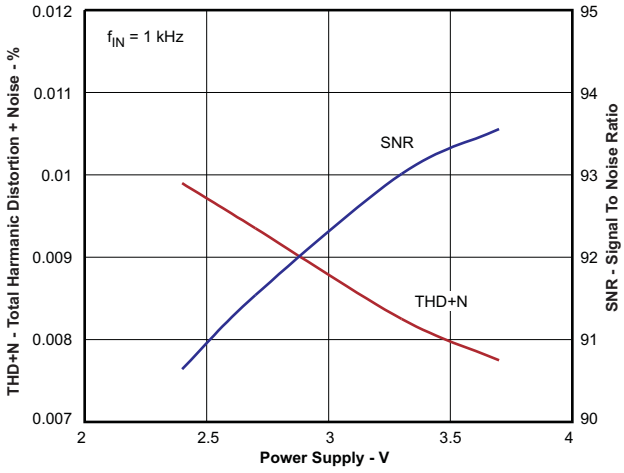


Figure 8.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 16-bit data, unless otherwise noted.

OUTPUT POWER vs POWER SUPPLY (HEADPHONE, 16-Ω)

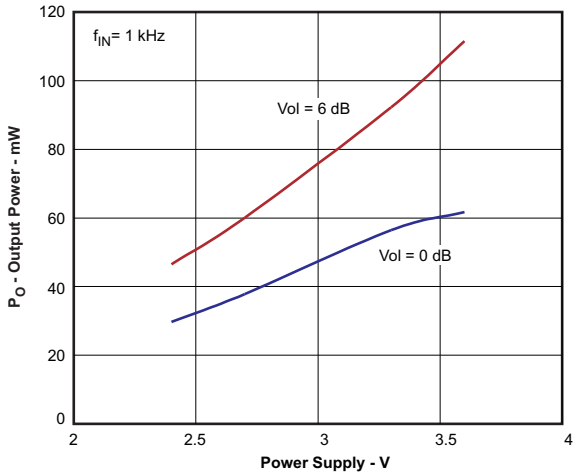


Figure 9.

THD+N vs OUTPUT POWER (HEADPHONE, 16-Ω, VOLUME = 6 dB)

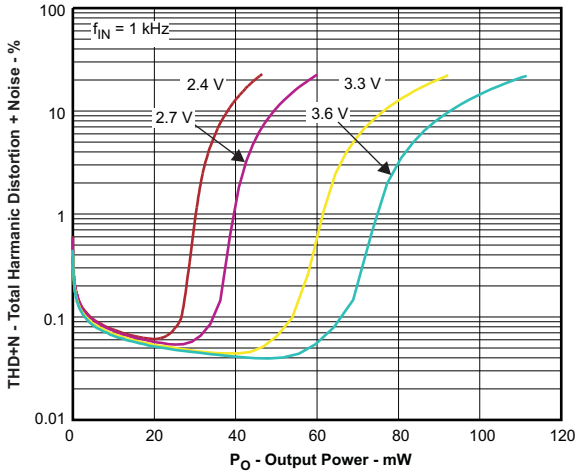


Figure 10.

THD+N vs OUTPUT POWER (HEADPHONE, 16-Ω, VOLUME = 0 dB)

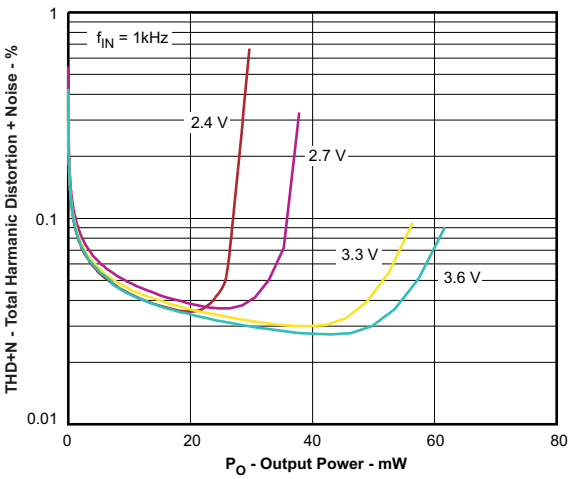


Figure 11.

OUTPUT SPECTRUM (DAC TO HEADPHONE OUTPUT, 16-Ω)

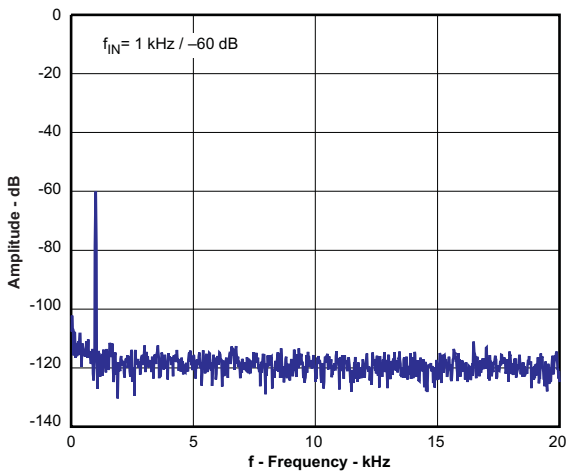


Figure 12.

DETAILED DESCRIPTION

Analog Input

The AIN1L and AIN1R pins can be used as microphone or line inputs with selectable 0-, 12-, or 20-dB boost and 1-Vrms input. All of these analog inputs have high input impedance (20 kΩ), which is not changed by gain settings. One pair of inputs is selected by register 87 (AIL0 and AIR0).

Gain Settings for Analog Input

The gain of the analog signals can be adjusted from 0 dB to –21 dB in 1-dB steps following the 0-, 12-, or 20-dB boost amplifier. The gain level can be set for each channel by registers 89 (GMR[2:0], GML [2:0].

D/A Converter

The DAC includes a multilevel delta-sigma modulator and an interpolation filter. These can be used to obtain high PSRR, low jitter sensitivity, and low out-of-band noise quickly and easily. The interpolation filter includes digital attenuator, digital soft mute, three-band tone control (bass, midrange and treble), and 3-D sound controlled by registers 92 to 95. The de-emphasis filter (32, 44.1 and 48 kHz) is controlled by registers 68 to 70 (ATL[5:0], ATR[5:0], PMUL, PMUR, DEM[1:0]). Oversampling rate control can reduce out-of-band noise when operating at low sampling rates by using register 70 (OVER).

Common Voltage

The V_{COM} pin is normally biased to 0.5 V_{CC}, and it provides the common voltage to internal circuitry. It is recommended that a 4.7-µF capacitor be connected between this pin and AGND to provide clean voltage and avoid pop noise. The PCM1774 may have a little pop noise on each analog output if a capacitor smaller than 4.7 µF is used.

Line Output

The HPOL/LOL and HPOR/LOR pins can drive a 10-kΩ load and be configured by register 74 (HPS[1:0]) as a monaural single-ended, monaural differential, or stereo single-line output with 1-Vrms output. These outputs include an analog volume amplifier that can be set from 6 dB to –70 dB and mute in steps of 0.5-, 1-, 2- or 4-dB. Each output is controlled by registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). No dc blocking capacitor is required when connecting an external speaker amplifier with monaural differential input. The center voltage is 0.5 V_{CC} with zero data input.

Headphone Output

The HPOL/LOL and HPOR/LOR pins can be configured as a stereo, monaural, or monaural differential headphone output by register 74 (HPS[1:0]). These pins have more than 30 or 40 mWrms output power into a 32- or 16-Ω load, either through a dc blocking capacitor or without a capacitor. These outputs include an analog volume amplifier that can be set from 6 dB to –70 dB in steps of 0.5, 1, 2, or 4 dB. Each is controlled by registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). The center voltage is 0.5 V_{CC} with zero data input.

Analog Mixing and Bypass

Mixing amplifiers (MXL, MXR) mix inputs from the AIN pins. The analog inputs are selected by register 87 (AIR0, AIL0) and can bypass the DAC and connect the mixed signal to the headphone or speaker outputs by register 88 (MXR[2:0], MXL[2:0]). The gain of the analog inputs is controlled by register 89 (GMR[2:0], GML[2:0]). These functions are suitable for FM radio, headset, and other analog sources without an ADC.

Digital Gain Control

A portable application with small speakers may be require a high sound level when playing back audio data recorded at low level. Digital gain control (DGC) can be used to amplify the digital input data by 0, 6, 12 or 18 dB by setting register 70 (SPX[1:0]).

3-D Sound

A 3-D sound effect is provided by mixing L-channel and R-channel data with a band-pass filter with two parameters, mixing ratio and band pass filter characteristic, that can be controlled by register 95 (3DP[3:0], 3FLO).

Three-Band Tone Control

Tone control has bass, midrange, and treble controls that can be adjusted from 12 dB to –12 dB in 1-dB steps by registers 92 to 94 (LGA[4:0], MGA[4:0] and HGA[4:0]). Register 92 (LPAE) attenuates the digital input signal automatically to prevent clipping of the output signal at settings above 0 dB for bass control. LPAE has no effect on midrange and treble controls.

Digital Monaural Mixing

The audio data can be converted from stereo digital data to mixed monaural digital data. The conversion occurs in the internal audio interface section and is controlled by register 96 (MXEN).

Zero-Cross Detection

Zero-cross detection minimizes audible zipper noise while changing analog volume and digital attenuation. This function applies to the digital input or digital output as defined by register 86 (ZCRS).

Short Protection

The short-circuit protection on each headphone output prevents damage to the device while an output is shorted to V_{PA}, an output is shorted to PGND, or any two outputs are shorted together. When the short circuit is detected on the outputs, the PCM1774 powers down the shorted amplifier immediately. The short-protection status can be monitored by reading register 77 (STHC, STHL, SCHR) through the I^2C interface. Short-circuit protection operates in any enabled headphone amplifier.

Pop-Noise Reduction Circuit

The pop-noise reduction circuit prevents audible noise when turning the power supply on/off and powering the device up/down in portable applications. It is recommended to establish the register settings in the sequence that is shown in Table 3 and Table 4. No particular external parts are required.

Power Up/Down for Each Module

Using register 72 (PMXL, PMXR), register 73 (PBIS, PDAR, PDAL, PHPR, PHPL) and register 90 (PCOM), unused modules can be powered down to minimize power consumption (7 mW during playback only).

Digital Audio Interface

The PCM1774 can receive I^2S, right-justified, left-justified, and DSP formats in both master and slave modes. These options can be selected in register 70 (PFM[1:0]), register 81 (RFM[1:0]) and register 84 (MSTR).

Digital Interface

All digital I/O pins can interface at various power supply voltages. V_{IO} pin can be connected to a 1.71-V to 3.6-V power supply.

Power Supply

The V_{CC} pin and the V_{PA} pin can be connected to 2.4 V to 3.6 V. The same voltage must be applied to both pins. The V_{DD} pin and the V_{IO} pin can be connected to 1.71 V to 3.6 V. A different voltage can be applied to each of these pins (for example, V_{DD} = 1.8 V, V_{IO} = 3.3 V).

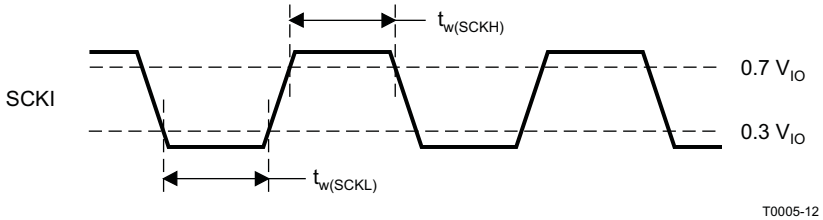
DESCRIPTION OF OPERATION

System Clock Input

The PCM1774 can accept clocks of various frequencies without a PLL. They are used for clocking the digital filters and automatic level control and delta-sigma modulators and are classified as common-audio and application-specific clocks. Table 2 shows frequencies of the common-audio clock and application-specific clock. Figure 13 shows the timing requirements for system clock inputs. The sampling rate and frequency of the system clocks are determined by the settings of register 86 (MSR[2:0]) and register 85 (NPR[5:0]). Note that the sampling rate of the application-specific clock has a little sampling error. The details are shown in Table 9.

Table 2. System Clock Frequencies

CLOCK	FREQUENCIES
Common-audio clock	11.2896, 12.288, 16.9344, 18.432 MHz
Application-specific clock	12, 13, 13.5, 24, 26, 27, 19.2, 19.68, 38.4, 39.36 MHz



PARAMETERS	SYMBOL	MIN	UNITS
System-clock pulse duration, high	$t_{w(SCKH)}$	7	ns
System-clock pulse duration, low	$t_{w(SCKL)}$	7	ns

Figure 13. System Clock Timing

Power-On Reset and System Reset

The power-on-reset circuit outputs a reset signal, typically at V_{DD} = 1.2 V, and this circuit does not depend on the voltage of other power supplies (V_{CC}, V_{PA}, and V_{IO}). Internal circuits are cleared to default status, then all analog and digital outputs have no signal. The PCM1774 does not require any power supply sequencing. Set Register data after turning all power supplies on.

System reset is enabled by setting register 85 (SRST = 1). After the reset sequence, the register data is reset to SRST = 0 automatically. All circuits are cleared to their default status at once by the system reset. Note that the PCM1774 has audible pop noise on the analog outputs when enabling SRST.

Power On/Off Sequence

To reduce audible pop noise, a sequence of register settings is required after turning all power supplies on when powering up, or before turning the power supplies off when powering down. If some modules are not required for a particular application or operation, they should be placed in the power-down state after performing the power-on sequence. The recommended power-on and power-off sequences are shown in Table 3 and Table 4, respectively.

Table 3. Recommended Power-On Sequence

STEP	REGISTER SETTINGS	NOTE
1	–	Turn on all power supplies(1)
2	4027h	Headphone amplifier L-ch volume (–6 dB)(2)
3	4127h	Headphone amplifier R-ch volume (–6 dB)(2)
6	4427h	Digital attenuator L-ch (–24 dB)(2)
7	4527h	Digital attenuator R-ch (–24 dB) (2)
8	4620h	DAC audio interface format (left-justified)(3)
12	49E0h	DAC (DAL, DAR) and analog bias power up
13	5601h	Zero-cross detection enable
14	4803h	Analog mixer (MXL, MXR) power up
15	5811h	Analog mixer input (SW2, SW5) select
16	49ECh	Headphone amplifier (HPL, HPR, HPC) power up
18	4A01h	V_{COM} power up
19	5230h	Analog front end (D2S, MCB, PG1, 2, 5, 6) power up
20	5711h	Analog input (MUX3, MUX4) select. Analog input (MUX1, MUX2) select

(1) V_{DD} should be turned on prior to or simultaneously with, the other power supplies. It is recommended to set register data with the system clock input after turning all power supplies on.
(2) Any level is acceptable for volume or attenuation. Level should be resumed by register data recorded when system powers off.
(3) Audio interface format should be set to match the DSP or decoder being used.

Table 4. Recommended Power-Off Sequence

STEP	REGISTER SETTINGS	NOTE
1	447Fh	DAC L-ch digital soft-mute enable(1)
2	457Fh	DAC R-ch digital soft-mute enable(1)
4	5811h	Analog mixer input (SW2, SW5) select
5	49ECh	Headphone amplifier (HPL, HPR, HPC) power up(2)
6	5200h	Analog front end (D2S, MCB, PG1, 2, 5, 6) power down
7	5A00h	PG1, PG2 gain control (0 dB)
8	4A00h	V_{COM} power down
9	–	Wait time (750 ms) (3)
10	49E0h	Headphone amplifier (HPL, HPR, HPC) power down, speaker amplifier (SPL, SPR) power down
11	4800h	Analog mixer (MXL, MXR) power down
12	4900h	DAC (DAL, DAR) and analog bias power down
13	–	Turn off all power supplies.(4)

(1) Any level is acceptable for volume or attenuation.
(2) The headphone amplifier must be operating during the power-off sequence.
(3) PCM1774 requires time for V_{COM} to reach the ground level from the common level. The wait time allowed depends on the settings of register 125 PTM[1:0], RES[4:0]. The default setting is 750 ms for V_{COM} = 4.7 µF.
(4) Power supply sequencing is not required. It is recommended to turn off all power supplies after setting the registers with the system clock input.

Power-Supply Current

The current consumption of the PCM1774 depends on power up/down status of each circuit module. In order to reduce the power consumption, disabling each module is recommended when it is not used in an application or operation. Table 5 shows the current consumption in some states.

Table 5. Power Consumption Table

OPERATION MODE	CONDITION	V_{OL} [V]	POWER SUPPLY CURRENT [mA]				PD [mW]
			V_{IO}	V_{DD}	V_{CC}	V_{PA}	TOTAL
All Power Down	Zero Data f_S = 44.1 kHz R_L = 0 Ω	1.8	0.000	0.000	–	–	0.000
		2.8	0.000	0.000	–	–	0.000
		3.3	0.000	0.000	–	–	0.000
		2.4	–	–	0.001	0.000	0.002
		2.8	–	–	0.001	0.000	0.003
		3.3	–	–	0.001	0.000	0.003
All Active	Zero Data f_S = 44.1 kHz R_L = 0 Ω	1.8	0	0.84	–	–	1.5
		2.8	0.03	1.47	–	–	4.2
		3.3	0.04	1.84	–	–	6.2
		2.4	–	–	1.68	0.38	4.9
		2.8	–	–	1.81	0.41	6.2
		3.3	–	–	1.96	0.46	8.0
Line Output	Zero Data f_S = 44.1 kHz R_L = 10 Ω	1.8	0	0.84	–	–	1.5
		2.8	0.03	1.47	–	–	4.2
		3.3	0.04	1.84	–	–	6.2
		2.4	–	–	1.38	0.38	4.2
		2.8	–	–	1.50	0.41	5.3
		3.3	–	–	1.64	0.46	6.9
Headphone Output	Zero Data f_S = 44.1 kHz R_L = 16 Ω	1.8	0	0.84	–	–	1.5
		2.8	0.03	1.47	–	–	4.2
		3.3	0.04	1.84	–	–	6.2
		2.4	–	–	1.38	0.38	4.2
		2.8	–	–	1.50	0.41	5.3
		3.3	–	–	1.65	0.46	7.0
Headphone Output with Sound Effect	Zero Data f_S = 44.1 kHz R_L = 16 Ω	1.8	0	1.29	–	–	2.3
		2.8	0.03	2.26	–	–	6.4
		3.3	0.04	2.82	–	–	9.4
		2.4	–	–	1.38	0.38	4.2
		2.8	–	–	1.50	0.42	5.4
		3.3	–	–	1.64	0.46	6.9
Headphone Output with Stereo Analog Mixing	Zero Data f_S = 44.1 kHz R_L = 16 Ω	1.8	0	0.84	–	–	1.5
		2.8	0.03	1.47	–	–	4.2
		3.3	0.04	1.84	–	–	6.2
		2.4	–	–	1.68	0.38	4.9
		2.8	–	–	1.81	0.41	6.2
		3.3	–	–	1.96	0.46	8.0
Headphone Output with Mono Analog Mixing	Zero Data f_S = 44.1 kHz R_L = 16 Ω	1.8	0	0.84	–	–	1.5
		2.8	0.03	1.47	–	–	4.2
		3.3	0.04	1.84	–	–	6.2
		2.4	–	–	1.53	0.38	4.6
		2.8	–	–	1.66	0.41	5.8
		3.3	–	–	1.81	0.46	7.5

Table 5. Power Consumption Table (continued)

OPERATION MODE	CONDITION	V_{OL} [V]	POWER SUPPLY CURRENT [mA]				PD [mW]
			V_{IO}	V_{DD}	V_{CC}	V_{PA}	TOTAL
Headphone Output with Stereo Analog Mixing	Zero Data f_S = 44.1 kHz R_L = 16 Ω No Digital Input(1)	1.8	0	0	–	–	0.0
		2.8	0	0	–	–	0.0
		3.3	0	0	–	–	0.0
		2.4	–	–	0.68	0.38	2.5
		2.8	–	–	0.69	0.41	3.1
		3.3	–	–	0.71	0.46	3.9
Headphone Output with Mono Analog Mixing	Zero Data f_S = 44.1 kHz R_L = 16 Ω No Digital Input(1)	1.8	0	0	–	–	0.0
		2.8	0	0	–	–	0.0
		3.3	0	0	–	–	0.0
		2.4	–	–	0.52	0.38	2.2
		2.8	–	–	0.54	0.42	2.7
		3.3	–	–	0.55	0.46	3.3

(1) All digital inputs are held static.

Audio Serial Interface

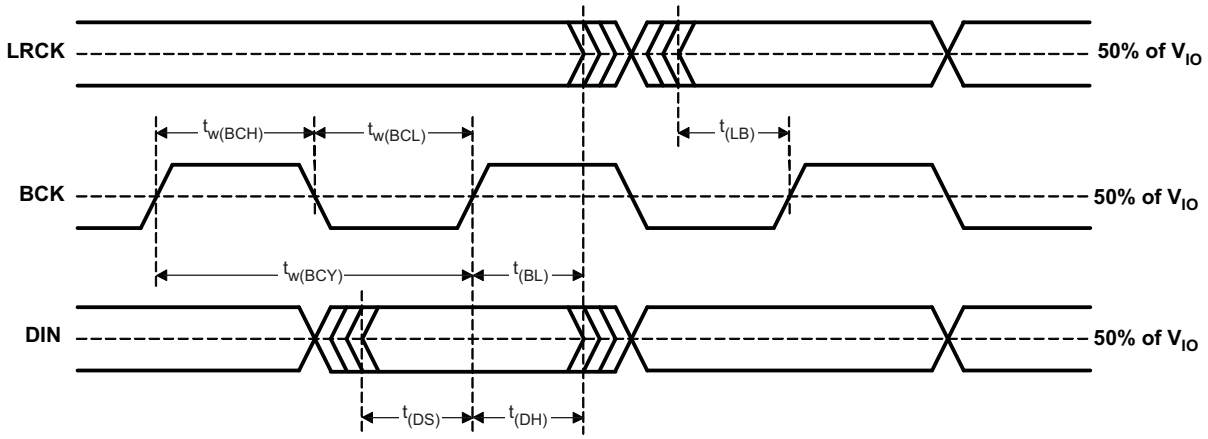
The audio serial interface for the PCM1774 comprises LRCK, BCK, DIN, and DOUT. Sampling rate (f_S), left and right channel are present on LRCK. DIN receives the serial data for the DAC interpolation filter, and DOUT transmits the serial data from the ADC decimation filter. BCK clocks the transfer of serial audio data on DIN and DOUT in its high-to-low transition. BCK and LRCK should be synchronized with audio system clock. Ideally, it is recommended that they be derived from it.

The PCM1774 requires LRCK to be synchronized with the system clock. The PCM1774 does not require a specific phase relationship between LRCK and the system clock.

The PCM1774 has both master mode and slave mode interface formats, which can be selected by register 84 (MSTR). In master mode, the PCM1774 generates LRCK and BCK from the system clock.

Audio Data Formats and Timing

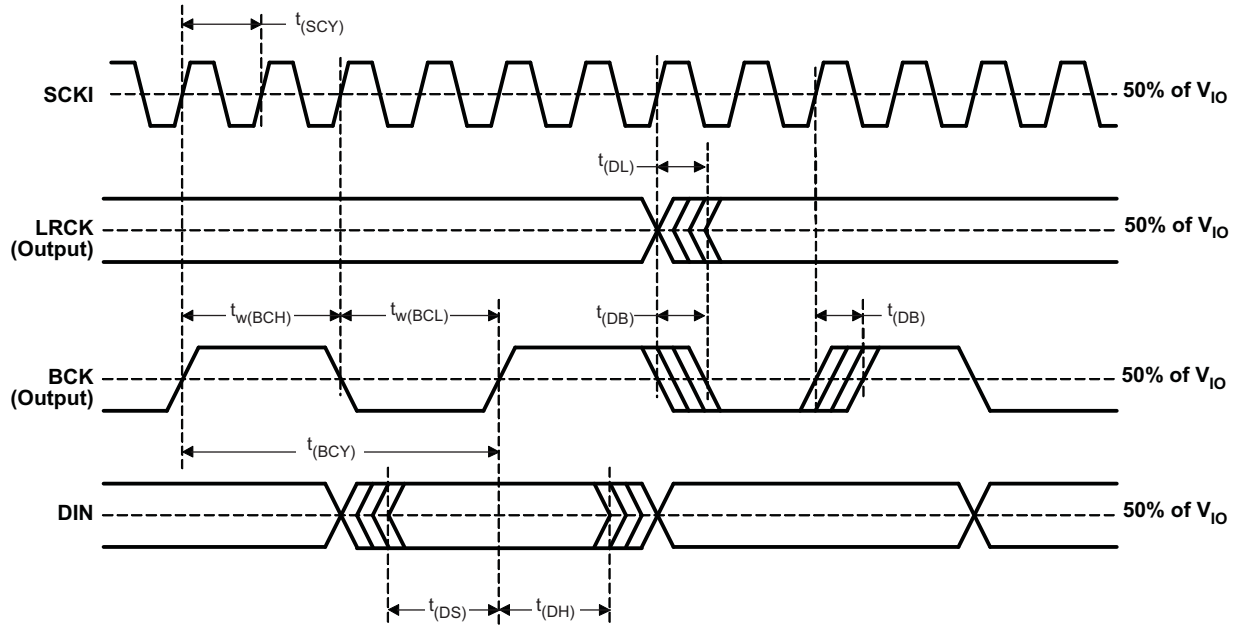
The PCM1774 supports I²S, right-justified, left-justified, and DSP formats. The data formats are shown in Figure 16 and are selected using registers 70 and 81 (RFM[1:0], PFM[1:0]). All formats require binary 2s-complement, MSB-first audio data. The default format is I²S. Figure 14 shows a detailed timing diagram.



PARAMETERS		MIN	MAX	UNITS
$t_{(BCY)}$	BCK pulse cycle time (I²S, left- and right-justified formats)	1/(64 f_S)(1)		
	BCK pulse cycle time (DSP format)	1/(256 f_S)(1)		
$t_{w(BCH)}$	BCK high-level time	35		ns
$t_{w(BCL)}$	BCK low-level time	35		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK edge to BCK rising edge	10		ns
$t_{(DS)}$	DIN set up time	10		ns
$t_{(DH)}$	DIN hold time	10		ns
t_r	Rising time of all signals		10	ns
t_f	Falling time of all signals		10	ns

(1) f_S is the sampling frequency.

Figure 14. Audio Interface Timing (Slave Mode)

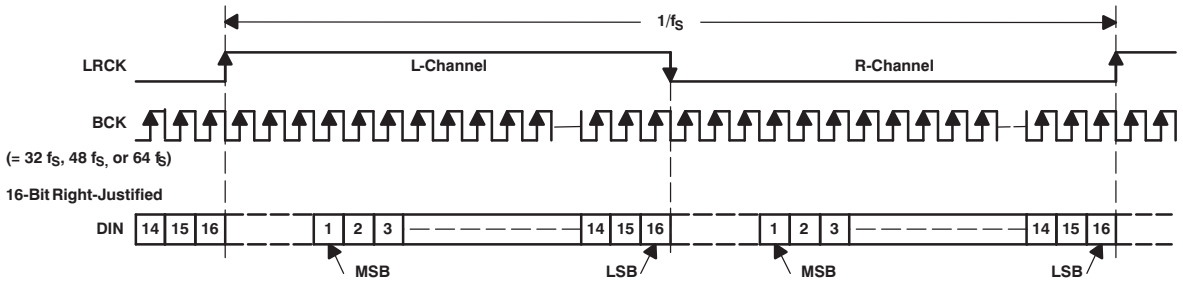


PARAMETERS		MIN	MAX	UNIT
$t_{(SCY)}$	SCKI pulse cycle time	$1/(256\ f_S)$ (1)		
$t_{(DL)}$	LRCK edge from SCKI rising edge	0	40	ns
$t_{(DB)}$	BCK edge from SCKI rising edge	0	40	ns
$t_{(BCY)}$	BCK pulse cycle time	$1/(64\ f_S)$ (1)		
$t_{w(BCH)}$	BCK high level time	146		ns
$t_{w(BCL)}$	BCK low level time	146		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns

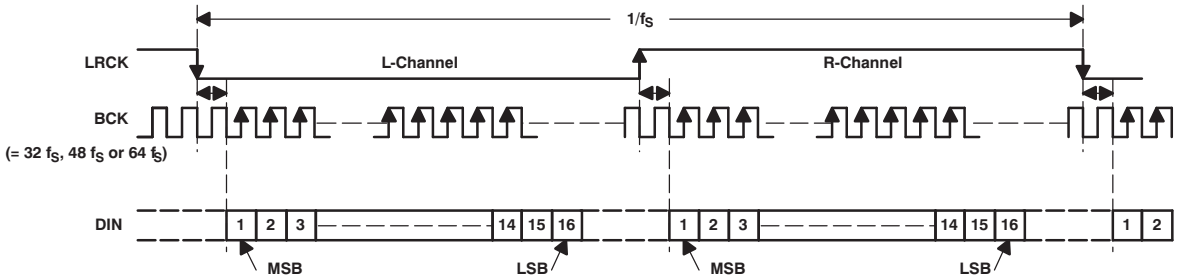
(1) f_S is up to 48 kHz. f_S is the sampling frequency.

Figure 15. Audio Interface Timing (Master Mode)

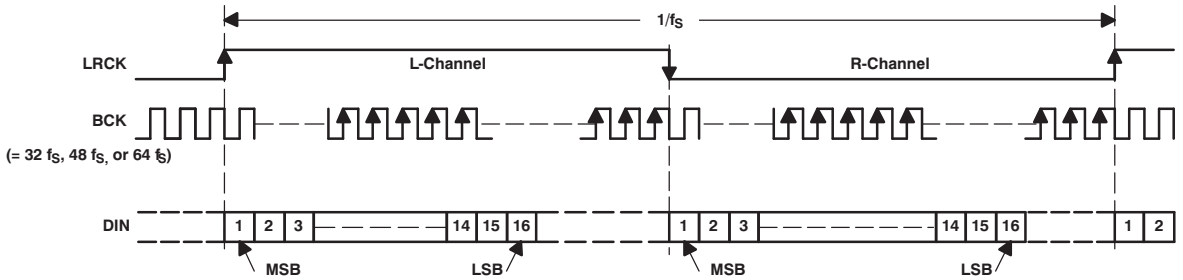
(a) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW, LRPC = 0



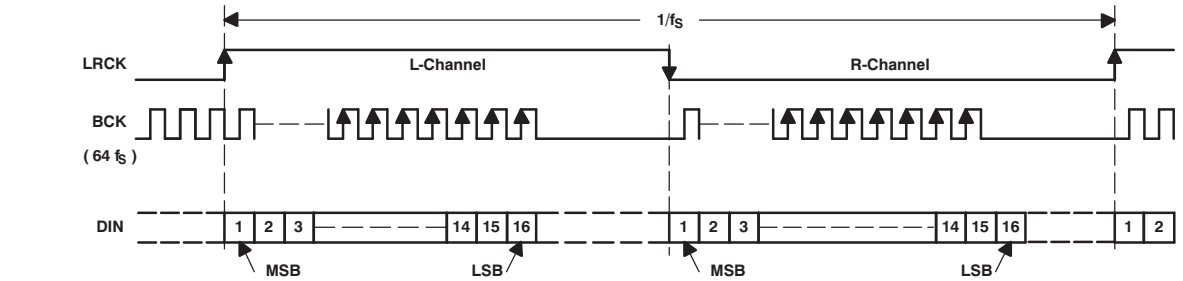
(b) I²S Data Format; L-Channel = LOW, R-Channel = HIGH, LRPC = 0



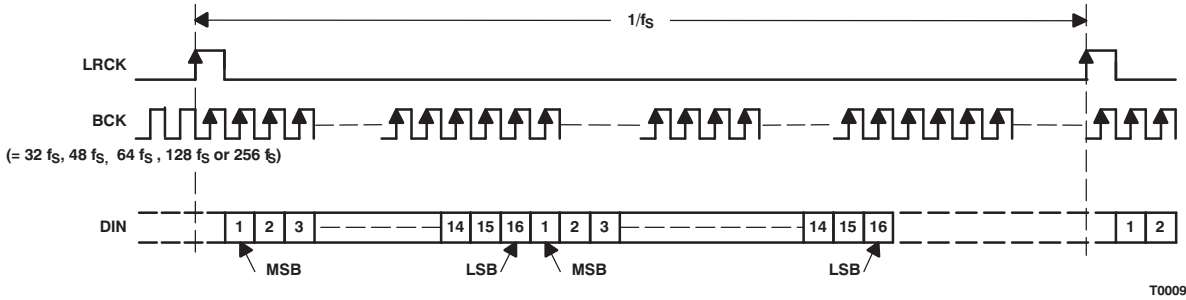
(c) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW, LRPC = 0



(d) Burst BCK Interface Format in Master Mode; L-Channel = HIGH, R-Channel = LOW, LRPC = 0



(e) DSP Format, LRPC = 0



NOTE: All audio interface formats support BCK = 64 f_S in master mode (register 69, MSTR = 1). The f_S of BCK at setting multi-sampling rate (register 85 and 86, NPR[5:0] and MSR[2:0]) is shown in Table 9 and Table 10.

Figure 16. Audio Data Formats

THREE-WIRE INTERFACE (SPI, MODE (PIN 28) = LOW)

All write operations for the serial control port use 16-bit data words. Figure 17 shows the control data word format. The most-significant bit must be 0. There are seven bits, labeled IDX[6:0], that set the register address for the write operation. The least-significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 18 shows the functional timing diagram for writing to the serial control port. To write the data into the mode register, the data is clocked into an internal shift register on the rising edge of the MC clock. The serial data should change on the falling edge of the MC clock, and MS should be LOW during write mode. The rising edge of MS should be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. MC can run continuously between transactions while MS is in the LOW state.

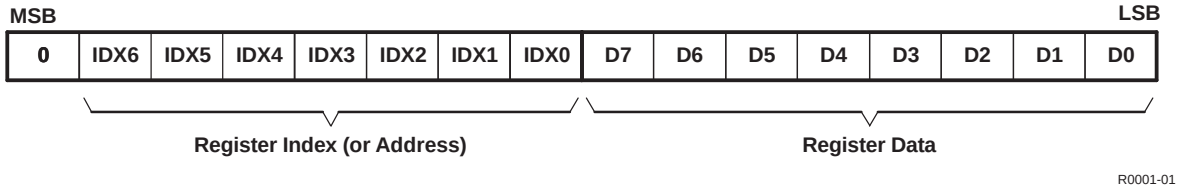


Figure 17. Control Data Word Format for MD

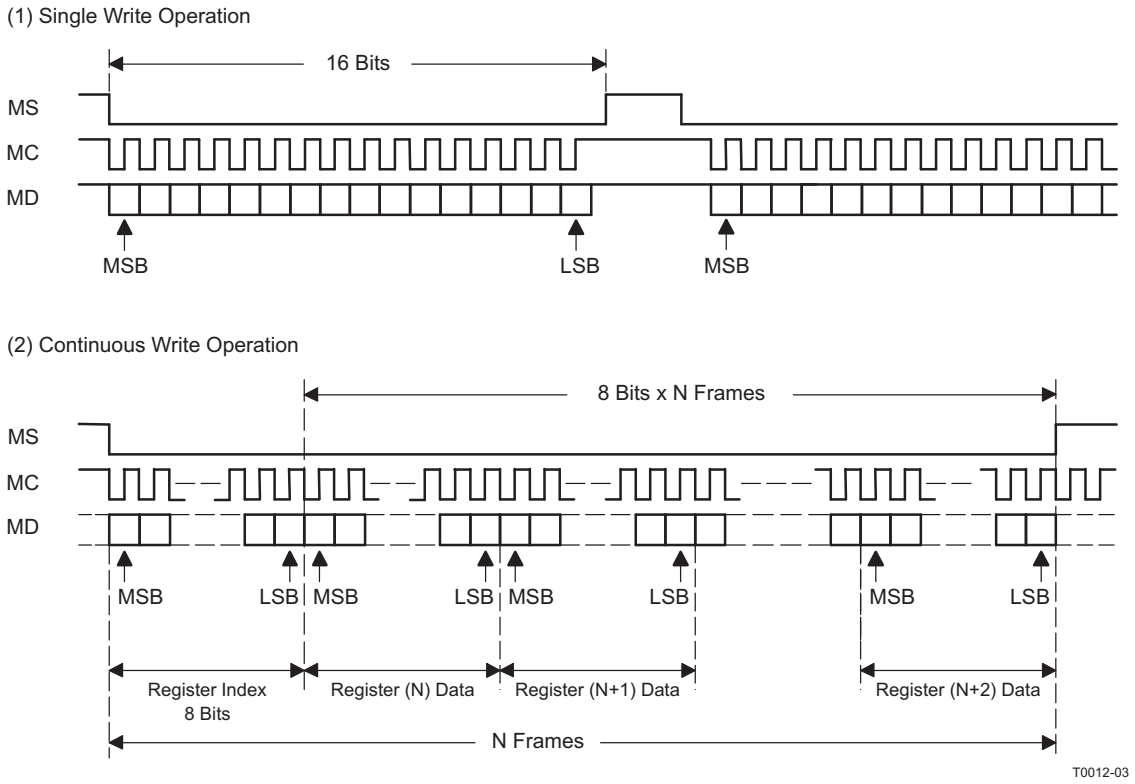
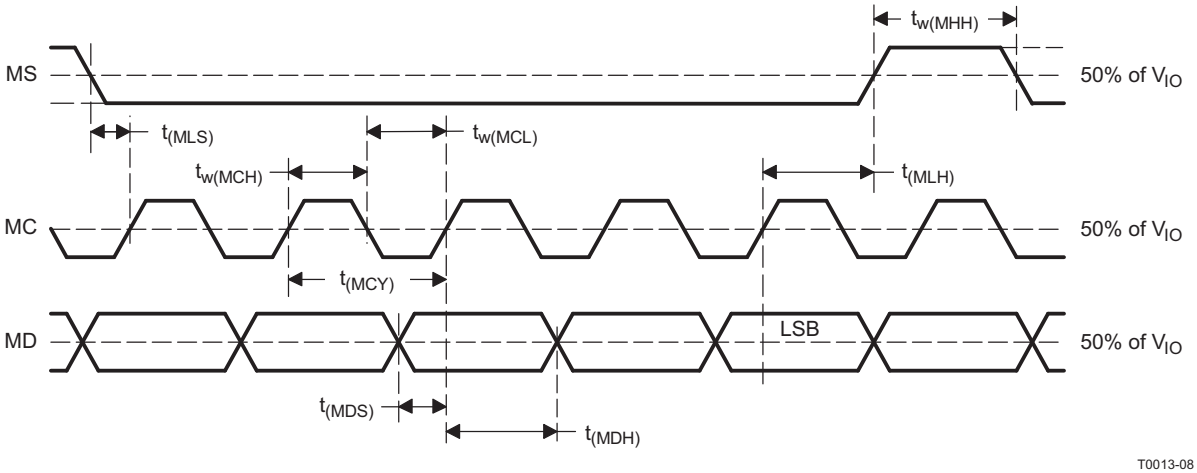


Figure 18. Register Write Operation

Three-Wire Interface (SPI) Timing Requirements

Figure 19 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	500(1)			ns
$t_{w(MCL)}$	MC low level time	50			ns
$t_{w(MCH)}$	MC high level time	50			ns
$t_{w(MHH)}$	MS high level time	See(1)			ns
$t_{(MLS)}$	MS falling edge to MC rising edge	50			ns
$t_{(MLH)}$	MS hold time	20			ns
$t_{(MDH)}$	MD hold time	15			ns
$t_{(MDS)}$	MD setup time	20			ns

(1) 3/(128 f_S) s (min), where f_S is sampling rate.

Figure 19. SPI Interface Timing

TWO-WIRE INTERFACE [I²C, MODE (PIN 28) = HIGH]

The PCM1774 supports the I²C serial bus and the data transmission protocol for the I²C standard as a slave device. This protocol is explained in I²C specification 2.0.

In I²C mode, the control terminals are changed as follows.

TERMINAL NAME	PROPERTY	DESCRIPTION
MS/ADR	Input	I²C address
MD/SDA	Input/output	I²C data
MC/SCL	Input	I²C clock

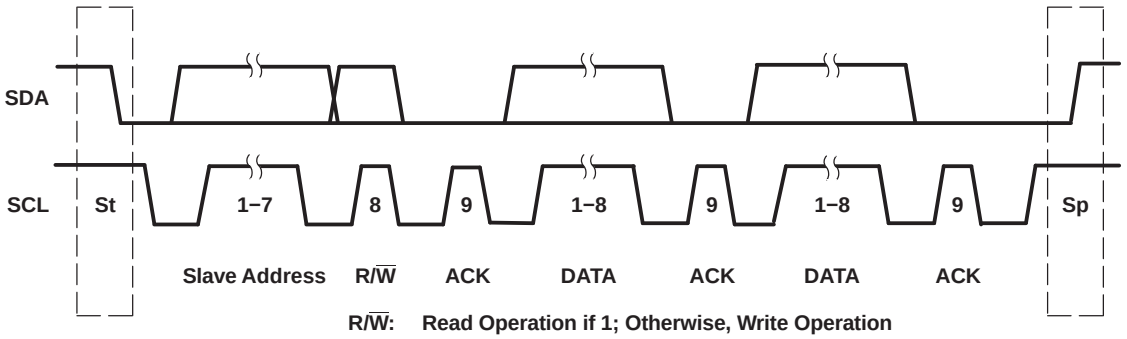
SLAVE ADDRESS

MSB							LSB
1	0	0	0	1	1	ADR	R/$\overline{W}$

The PCM1774 has its own 7-bit slave address. The first six bits (MSBs) of the slave address are factory preset to 100011. The last bit of the address byte is the device select bit, which can be user-defined by the ADR terminal. A maximum of two PCM1774 can be connected on the same bus at one time. The PCM1774 responds when it receives its own slave address.

Packet Protocol

The master device must control packet protocol, which consists of start condition, slave address with read/write bit, data (if write) or acknowledgment (if read), and stop condition. The PCM1774 supports only slave receiver and slave transmitter.



Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*	*M*
Data Type	St	Slave Address	R/$\overline{W}$	ACK	DATA	ACK	DATA	ACK	Sp

Read Operation

Transmitter	*M*	*M*	*M*	*S*	*S*	*M*	*S*	*M*	*M*
Data Type	St	Slave Address	R/$\overline{W}$	ACK	DATA	ACK	DATA	NACK	Sp

M: Master Device *S: Slave Device*
St: Start Condition Sp: Stop Condition

T0049-03

Figure 20. Basic I^{2}C Framework

WRITE OPERATION

The master can write any PCM1774 registers in a single access. The master sends a PCM1774 slave address with a write bit, a register address, and data. When undefined registers are accessed, the PCM1774 does not send any acknowledgment. Figure 21 shows a diagram of the write operation.

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Write Data	ACK	Sp

M: Master Device *S: Slave Device*
St: Start Condition $\overline{W}$: Write ACK: Acknowledge Sp: Stop Condition

R0002-01

Figure 21. Framework for Write Operation

READ OPERATION

The master can read PCM1774 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM1774 slave address with a read bit after storing the register address. Then the PCM1774 transfers the data which the index register specifies. Figure 22 shows a diagram of the read operation.

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*M*	*M*	*S*	*S*	*M*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

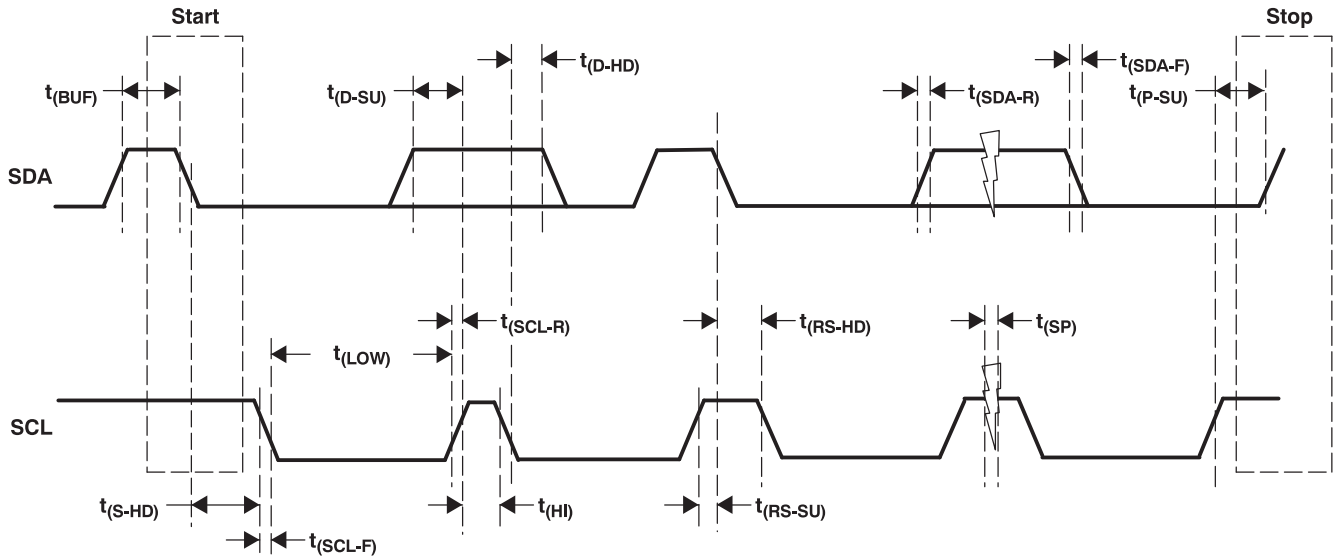
M: Master Device *S: Slave Device* St: Start Condition
Sr: Repeated Start Condition ACK: Acknowledge Sp: Stop Condition NACK: Not Acknowledge
$\overline{W}$: Write R: Read

R0002-02

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

Figure 22. Read Operation

Timing Diagram



T0050-03

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard		100	kHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	Standard	4.7		µs
$t_{(LOW)}$	Low period of the SCL clock	Standard	4.7		µs
$t_{(HI)}$	High period of the SCL clock	Standard	4		µs
$t_{(RS-SU)}$	Setup time for START condition	Standard	4.7		µs
$t_{(S-HD)}$	Hold time for START condition	Standard	4		µs
$t_{(D-SU)}$	Data setup time	Standard	250		ns
$t_{(D-HD)}$	Data hold time	Standard	0	900	ns
$t_{(SCL-R)}$	Rise time of SCL signal	Standard	20 + 0.1 C_B	1000	ns
$t_{(SCL-R1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard	20 + 0.1 C_B	1000	ns
$t_{(SCL-F)}$	Fall time of SCL signal	Standard	20 + 0.1 C_B	1000	ns
$t_{(SDA-R)}$	Rise time of SDA signal	Standard	20 + 0.1 C_B	1000	ns
$t_{(SDA-F)}$	Fall time of SDA signal	Standard	20 + 0.1 C_B	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	Standard	4		µs
C_B	Capacitive load for SDA and SCL line			400	pF
$t_{(SP)}$	Pulse duration of suppressed spike			25	ns

Figure 23. I^2C Interface Timing

USER-PROGRAMMABLE MODE CONTROLS

Register Map

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 6. Mode Control Register Map

REGISTER	IDX[6:0] (B14–B8)	DESCRIPTION	B7	B6	B5	B4	B3	B2	B1	B0
Register 64	40h	Volume for HPA (L-ch)	RSV	HMUL	HLV5	HLV4	HLV3	HLV2	HLV1	HLV0
Register 65	41h	Volume for HPA (R-ch)	RSV	HMUR	HRV5	HRV4	HRV3	HRV2	HRV1	HRV0
Register 68	44h	DAC digital attenuation and soft mute (L-ch)	RSV	PMUL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 69	45h	DAC digital attenuation and soft mute (R-ch)	RSV	PMUR	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 70	46h	DAC over sampling, de-emphasis, audio interface, DGC	DEM1	DEM0	PFM1	PFM0	SPX1	SPX0	RSV	OVER
Register 72	48h	Analog mixer power up/down	RSV	RSV	RSV	RSV	RSV	RSV	PMXR	PMXL
Register 73	49h	DAC and HPA power up/down	PBIS	PDAR	PDAL	RSV	PHPR	PHPL	RSV	RSV
Register 74	4Ah	Analog output configuration select	RSV	RSV	RSV	RSV	HPS1	HPS0	RSV	PCOM
Register 75	4Bh	HPA insertion detection, short protection	RSV	RSV	RSV	RSV	SDHR	SDHL	RSV	RSV
Register 77	4Dh	Shut down status read back	RSV	RSV	RSV	RSV	STHR	STHL	RSV	RSV
Register 82	52h	PG1, 2, 5, 6, power up/down	RSV	RSV	PAIR	PAIL	RSV	RSV	RSV	RSV
Register 84	54h	Master mode	RSV	RSV	RSV	RSV	RSV	MSTR	RSV	BIT0
Register 85	55h	System reset, sampling rate control, data swap	SRST	LRPC	NPR5	NPR4	NPR3	NPR2	NPR1	NPR0
Register 86	56h	BCK configuration, sampling rate control, zero-cross	MBST	MSR2	MSR1	MSR0	RSV	RSV	RSV	ZCRS
Register 87	57h	Analog input select (MUX1, 2, 3, 4)	RSV	RSV	AIR1	AIR0	RSV	RSV	AIL1	AIL0
Register 88	58h	Analog mixing switch (SW1, 2, 3, 4, 5, 6)	RSV	MXR2	MXR1	MXR0	RSV	MXL2	MXL1	MXL0
Register 89	59h	Analog to analog path (PG5, 6) gain	RSV	GMR2	GMR1	GMR0	RSV	GML2	GML1	GML0
Register 90	5Ah	Microphone boost	RSV	RSV	RSV	RSV	RSV	RSV	G20R	G20L
Register 92	5Ch	Bass boost gain level	LPAE	RSV	RSV	LGA4	LGA3	LGA2	LGA1	LGA0
Register 93	5Dh	Middle boost gain level	RSV	RSV	RSV	MGA4	MGA3	MGA2	MGA1	MGA0
Register 94	5Eh	Treble boost gain level	RSV	RSV	RSV	HGA4	HGA3	HGA2	HGA1	HGA0
Register 95	5Fh	Sound effect source select, 3D sound	RSV	3DEN	RSV	3FL0	3DP3	3DP2	3DP1	3DP0
Register 96	60h	digital monaural mixing	RSV	RSV	RSV	RSV	RSV	RSV	RSV	MXEN
Register 124	7Ch	PG1/PG2 additional Gain	RSV	RSV	RSV	RSV	RSV	RSV	G12R	G12L
Register 125	7Dh	Power up/down time control	RSV	PTM1	PTM0	RES4	RES3	RES2	RES1	RES0

HPA: Headphone amplifier DAC: D/A converter
PGx: Analog input buffer

Register Definitions

Registers 64 and 65

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 64	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	HMUL	HLV5	HLV4	HLV3	HLV2	HLV1	HLV0
Register 65	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	HMUR	HRV5	HRV4	HRV3	HRV2	HRV1	HRV0

IDX[6:0]: 100 0000b (40h): Register 64

IDX[6:0]: 100 0001b (41h): Register 65

HMUL: Analog Mute Control for HPL (Line or Headphone L-Channel)

HMUR: Analog Mute Control for HPR (Line or Headphone R-Channel)

Default value: 1

HPOL/LOL and HPOR/LOR can be independently muted to zero level when HMUL and HMUR = 1. These settings take precedence over analog volume level settings.

HMUL, HMUR = 0	Mute disabled
HMUL, HMUR = 1	Mute enabled (default)

HLV[5:0]: Analog Volume for HPL (Headphone L-Channel)

HRV[5:0]: Analog Volume for HPR (Headphone R-Channel)

Default value: 00 0000.

HPOL/LOL and HPOR/LOR can be independently controlled between 6 dB and –70 dB, with step size depending on the gain level as shown in Table 7. Outputs may have zipper noise while changing levels. This noise can be reduced by selecting zero-cross detection (register 86, ZCRS).

Table 7. Headphone Gain Level Setting

HLV[5:0], HRV[5:0]		STEP	GAIN LEVEL SETTING	HLV[5:0], HRV[5:0]		STEP	GAIN LEVEL SETTING	HLV[5:0], HRV[5:0]		STEP	GAIN LEVEL SETTING
11 1111	3F	0.5 dB	6 dB	10 1001	29	0.5 dB	–5 dB	01 0011	13	1 dB	–21 dB
11 1110	3E		5.5 dB	10 1000	28		–5.5 dB	01 0010	12		–22 dB
11 1101	3D		5 dB	10 0111	27		–6 dB	01 0001	11		–23 dB
11 1100	3C		4.5 dB	10 0110	26		–6.5 dB	01 0000	10		–24 dB
11 1011	3B		4 dB	10 0101	25		–7 dB	00 1111	0F	2 dB	–26 dB
11 1010	3A		3.5 dB	10 0100	24		–7.5 dB	00 1110	0E		–28 dB
11 1001	39		3 dB	10 0011	23		–8 dB	00 1101	0D		–30 dB
11 1000	38		2.5 dB	10 0010	22		–8.5 dB	00 1100	0C		–32 dB
11 0111	37		2 dB	10 0001	21		–9 dB	00 1011	0B		–34 dB
11 0110	36		1.5 dB	10 0000	20		–9.5 dB	00 1010	0A		–36 dB
11 0101	35		1 dB	01 1111	1F		–10 dB	00 1001	09		–38 dB
11 0100	34		0.5 dB	01 1110	1E		–10.5 dB	00 1000	08		–40 dB
11 0011	33		0 dB	01 1101	1D		–11 dB	00 0111	07		–42 dB
11 0010	32		–0.5 dB	01 1100	1C	1 dB	–12 dB	00 0110	06	4 dB	–46 dB
11 0001	31		–1 dB	01 1011	1B		–13 dB	00 0101	05		–50 dB
11 0000	30		–1.5 dB	01 1010	1A		–14 dB	00 0100	04		–54 dB
10 1111	2F		–2 dB	01 1001	19		–15 dB	00 0011	03		–58 dB
10 1110	2E		–2.5 dB	01 1000	18		–16 dB	00 0010	02		–62 dB
10 1101	2D		–3 dB	01 0111	17		–17 dB	00 0001	01		–66 dB
10 1100	2C		–3.5 dB	01 0110	16		–18 dB	00 0000	00		–70 dB
10 1011	2B		–4 dB	01 0101	15		–19 dB				
10 1010	2A		–4.5 dB	01 0100	14		–20 dB				

Registers 68 and 69

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 68	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PMUL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 69	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PMUR	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

IDX[6:0]: 100 0100b (44h): Register 68

IDX[6:0]: 100 0101b (45h): Register 69

PMUL: Digital Soft Mute Control for DAL (DAC L-Channel)

PMUR: Digital Soft Mute Control for DAR (DAC R-Channel)

Default value: 0

The digital inputs of the DAC can be independently muted by setting PMUL and PMUR = 1. The digital data is changed from the current attenuation level to mute level by a 1-dB step for every $8/f_S$ time period. When PMUL and PMUR are set to 0, the digital data is changed from the mute level to the current attenuation level by a 1-dB step for every $8/f_S$ time period. In the PCM1774, audible zipper noise can be reduced by selecting zero-cross detection (register 86, ZCRS).

PMUL, PMUR = 0	Mute disabled (default)
PMUL, PMUR = 1	Mute enabled

ATL[5:0]: Digital Attenuation Setting for DAL (DAC L-Channel)

ATR[5:0]: Digital Attenuation Setting for DAR (DAC R-Channel)

Default value: 11 1111b

The digital inputs of the DAC can be independently attenuated. The attenuation of the digital input is changed by a 1-dB step for every $8/f_S$ time period. Audible zipper noise in the PCM1774 can be reduced by selecting zero-cross detection (register 86, ZCRS).

Table 8. Digital Attenuation Setting

ATL[5:0], ATR[5:0]		ATTENUATION LEVEL SETTING	ATL[5:0], ATR[5:0]		ATTENUATION LEVEL SETTING	ATL[5:0], ATR[5:0]		ATTENUATION LEVEL SETTING
11 1111	3F	0 dB (default)	10 1001	29	–22 dB	01 0011	13	–44 dB
11 1110	3E	–1 dB	10 1000	28	–23 dB	01 0010	12	–45 dB
11 1101	3D	–2 dB	10 0111	27	–24 dB	01 0001	11	–46 dB
11 1100	3C	–3 dB	10 0110	26	–25 dB	01 0000	10	–47 dB
11 1011	3B	–4 dB	10 0101	25	–26 dB	00 1111	0F	–48 dB
11 1010	3A	–5 dB	10 0100	24	–27 dB	00 1110	0E	–49 dB
11 1001	39	–6 dB	10 0011	23	–28 dB	00 1101	0D	–50 dB
11 1000	38	–7 dB	10 0010	22	–29 dB	00 1100	0C	–51 dB
11 0111	37	–8 dB	10 0001	21	–30 dB	00 1011	0B	–52 dB
11 0110	36	–9 dB	10 0000	20	–31 dB	00 1010	0A	–53 dB
11 0101	35	–10 dB	01 1111	1F	–32 dB	00 1001	09	–54 dB
11 0100	34	–11 dB	01 1110	1E	–33 dB	00 1000	08	–55 dB
11 0011	33	–12 dB	01 1101	1D	–34 dB	00 0111	07	–56 dB
11 0010	32	–13 dB	01 1100	1C	–35 dB	00 0110	06	–57 dB
11 0001	31	–14 dB	01 1011	1B	–36 dB	00 0101	05	–58 dB
11 0000	30	–15 dB	01 1010	1A	–37 dB	00 0100	04	–59 dB
10 1111	2F	–16 dB	01 1001	19	–38 dB	00 0011	03	–60 dB
10 1110	2E	–17 dB	01 1000	18	–39 dB	00 0010	02	–61 dB
10 1101	2D	–18 dB	01 0111	17	–40 dB	00 0001	01	–62 dB
10 1100	2C	–19 dB	01 0110	16	–41 dB	00 0000	00	Mute
10 1011	2B	–20 dB	01 0101	15	–42 dB			
10 1010	2A	–21 dB	01 0100	14	–43 dB			

Register 70

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 70	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DEM1	DEM0	PFM1	PFM0	SPX1	SPX0	RSV	OVER

IDX[6:0]: 100 0110b (46h): Register 70

DEM[1:0]: De-Emphasis Filter Selection

Default value: 00

A digital de-emphasis filter is in front of the interpolation filter. One of three de-emphasis filters can be selected corresponding to the sampling rate, 32 kHz, 44.1 kHz, or 48 kHz.

DEM[1:0]	De-Emphasis Filter Selection
00	OFF (default)
01	32 kHz
10	44.1 kHz
11	48 kHz

PFM[1:0]: Audio Interface Selection for DAC (Digital Input)

Default value: 00

The audio interface for the DAC digital input has I^2S, right-justified, left-justified, and DSP formats.

PFM[1:0]	Audio Interface Selection for DAC Digital Input
00	I^2S format (default)
01	Right-justified format
10	Left-justified format
11	DSP format

SPX[1:0]: Digital Gain Control for DAC Input

Default value: 00

These bits are used to gain up the digital input data.

SPX[1:0]	Digital Gain Control for DAC input
00	0 dB (default)
01	6 dB
10	12 dB
11	18 dB

OVER: Oversampling Control for Delta-Sigma DAC

Default value: 0

This bit is used to control the oversampling rate of delta-sigma DAC. When the PCM1774 operates at low sampling rates (less than 24 kHz) and the SCKI frequency is less than 12.5 MHz, OVER = 1 is recommended.

OVER = 0	128 f_S (default)
OVER = 1	192 f_S, 256 f_S, 384 f_S

Register 72

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 72	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	PMXR	PMXL

IDX[6:0]: 100 1000b (48h) Register 72

PMXR: Power Up/Down for MXR (Mixer R-Channel)

PMXL: Power Up/Down for MXL (Mixer L-Channel)

Default value: 0

These bits are used to control power up/down for the analog mixer.

PMXL, PMXR = 0	Power down (default)
PMXL, PMXR = 1	Power up

Register 73

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 73	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	PBIS	PDAR	PDAL	RSV	PHPR	PHPL	RSV	RSV

IDX[6:0]: 100 1001b (49h): Register 73

PBIS: Power Up/Down Control for Bias

Default value: 0

This bit is used to control power up/down for the analog bias circuit.

PBIS = 0	Power down (default)
PBIS = 1	Power up

PDAR: Power Up/Down Control for DAR (DAC and R-Channel Digital Filter)

PDAL: Power Up/Down Control for DAL (DAC and L-Channel Digital Filter)

Default value: 0

These bits are used to control power up/down for the DAC and interpolation filter.

PDAR, PDAL = 0	Power down (default)
PDAR, PDAL = 1	Power up

PHPR: Power Up/Down Control for HPR (Line or R-Channel Headphone Output)

PHPL: Power Up/Down Control for HPL (Line or L-Channel Headphone Output)

Default value: 0

These bits are used to control power up/down for the headphone amplifier.

PHPR, PHPL = 0	Power down (default)
PHPR, PHPL = 1	Power up

Register 74

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 74	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	HPS1	HPS0	RSV	PCOM

IDX[6:0]: 100 1010b (4Ah): Register 74

HPS[1:0]: Line or Headphone Output Configuration

Default value: 00

HPOL/LOL and HPOR/LOR can be configured selected as follows.

HPS[1:0]	Line or Headphone Output Configuration
0 0	Stereo output (default)
0 1	Single monaural output
1 0	Differential monaural output
1 1	Reserved

PCOM: Power Up/Down Control for V_{COM}

Default value: 0

This bit is used to control power up/down for V_{COM}.

PCOM = 0	Power down (default)
PCOM = 1	Power up

Register 75

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 75	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	SDHR	SDHL	RSV	RSV

IDX[6:0]: 100 1011b (4Bh): Register 75

SDHR: Short Protection Status for HPR (R-Channel Headphone)

SDHL: Short Protection Status for HPL (L-Channel Headphone)

Default value: 0

Short-circuit protection can be disabled if this function is not needed in an application.

SDHR, SDSL = 0	Enabled (default)
SDHR, SDHL = 1	Disabled

Register 77

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 77	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	STHR	STHL	RSV	RSV

IDX[6:0]: 100 1101b (4Dh): Register 77

STHR: Short Protection Status for HPR (R-Channel Headphone)

STHL: Short Protection Status for HPL (L-Channel Headphone)

These bits can be used to read short protection status through the I^2C interface.

STHR, STHL = 0	Detect short circuit
STHR, STHL = 1	Not detect short circuit

Register 82

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 82	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	PAIR	PAIL	RSV	RSV	RSV	RSV

IDX[6:0]: 101 0010b (52h): Register 82

PAIR: Power Up/Down for PG2 and PG6 (Gain Amplifier for R-Channel Analog Input)

PAIL: Power Up/Down for PG1 and PG5 (Gain Amplifier for L-Channel Analog Input)

Default value: 0

These bits are used to control power up/down for PG2 and PG6 (gain amplifier for analog input).

PAIR, PAIL = 0	Power down (default)
PAIR, PAIL = 1	Power up

Registers 84–86

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 84	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	MSTR	RSV	BIT0
Register 85	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	LRPC	NPR5	NPR4	NPR3	NPR2	NPR1	NPR0
Register 86	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MBST	MSR2	MSR1	MSR0	RSV	RSV	RSV	ZCRS

IDX[6:0]: 101 0100b (54h): Register 84

IDX[6:0]: 101 0101b (55h): Register 85

IDX[6:0]: 101 0110b (56h): Register 86

MSTR: Master or Slave Selection for Audio Interface

Default value: 0

This bit is used to select either master or slave mode for the audio interface. In master mode, the PCM1774 generates LRCK and BCK from the system clock. In slave mode, it receives LRCK and BCK from another device.

MSTR = 0	Slave interface (default)
MSTR = 1	Master interface

BIT0: Bit Length Selection for Audio Interface

Default value: 1

This bit is used to select the data bit length for DAC input.

BIT0 = 0	Reserved
BIT0 = 1	16 bits (default)

SRST: System Reset

Default value: 0

This bit is used to enable system reset. All circuits are reset by setting SRST = 1. After completing the reset sequence, SRST is set to 0 automatically.

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

LRPC: LRCK Polarity Control

Default value: 0

This bit is used to reverse L-channel and R-channel audio data.

LRPC = 0	Normal (default)
LRPC = 1	Reverse

NPR[5:0]: System Clock Rate Selection

Default value: 000000

MSR[2:0]: System Clock Dividing Rate Selection in Master Mode (Register 70)

Default value: 000

These bits are used to select the system clock rate and the dividing rate of the input system clock. See Table 9 for the details.

Table 9. System Clock Frequency for Common-Audio Clock

SYSTEM CLOCK SCK (MHz)	ADC SAMPLING RATE ADC f_S (kHz)	DAC SAMPLING RATE DAC f_S (kHz)	REGISTER SETTINGS(1)		BIT CLOCK BCK (f_S)
			MSR[2:0]	NPR[5:0]	
6.144	24 (SCK/256)		010	00 0000	64
	16 (SCK/384)		011	00 0000	64
	12 (SCK/512)		100	00 0000	64
	8 (SCK/768)		101	00 0000	64
	6 (SCK/1024)		110	00 0000	64
	4 (SCK/1536)		111	00 0000	64
8.192	32 (SCK/256)		010	00 0000	64
	16 (SCK/512)		100	00 0000	64
	8 (SCK/1024)		110	00 0000	64
12.288	48 (SCK/256)		010	00 0000	64
	32 (SCK/384)		011	00 0000	64
	24 (SCK/512)		100	00 0000	64
	16 (SCK/768)		101	00 0000	64
	12 (SCK/1024)		110	00 0000	64
	8 (SCK/1536)		111	00 0000	64
18.432	48 (SCK/384)		011	00 0000	64
	24 (SCK/768)		101	00 0000	64
	12 (SCK/1536)		111	00 0000	64
5.6448	22.05 (SCK/256)		010	00 0000	64
	14.7 (SCK/384)		011	00 0000	64
	11.025 (SCK/512)		100	00 0000	64
	7.35 (SCK/768)		101	00 0000	64
	5.5125 (SCK/1024)		110	00 0000	64
	3.675 (SCK/1536)		111	00 0000	64
11.2896	44.1 (SCK/256)		010	00 0000	64
	29.4 (SCK/384)		011	00 0000	64
	22.05 (SCK/512)		100	00 0000	64
	14.7 (SCK/768)		101	00 0000	64
	11.025 (SCK/1024)		110	00 0000	64
	7.35 (SCK/1536)		111	00 0000	64

(1) Other settings are reserved.

Table 10. System Clock Frequency for Application-Specific Clock

SYSTEM CLOCK SCK (MHz)	ADC SAMPLING RATE ADC f_S (kHz) / DAC SAMPLING RATE DAC f_S (kHz)	REGISTER SETTINGS		BIT CLOCK BCK (f_S)
		MSR[2:0]	NPR[5:0]	
13.5	48.214 (SCK/280)	010	00 0010	70
	44.407 (SCK/304)	010	00 0001	76
	32.142 (SCK/420)	010	10 0010	70
	24.107 (SCK/560)	100	00 0010	70
	22.203 (SCK/608)	100	00 0001	76
	16.071 (SCK/840)	100	10 0010	70
	12.053 (SCK/1120)	110	00 0010	70
	8.035 (SCK/1680)	110	10 0010	70
27	48.214 (SCK/560)	010	01 0010	70
	44.407 (SCK/608)	010	01 0001	76
	32.142 (SCK/840)	010	11 0010	70
	24.107 (SCK/1120)	100	01 0010	70
	22.203 (SCK/1216)	100	01 0001	76
	16.071 (SCK/1680)	100	11 0010	70
	12.053 (SCK/2240)	110	01 0010	70
	8.035 (SCK/3360)	110	11 0010	70
12	48.387 (SCK/248)	010	00 0100	62
	44.117 (SCK/272)	010	00 0011	68
	32.258 (SCK/372)	010	10 0100	62
	24.193 (SCK/496)	100	00 0100	62
	22.058 (SCK/544)	100	00 0011	68
	16.129 (SCK/744)	100	10 0100	62
	12.096 (SCK/992)	110	00 0100	62
	8.064 (SCK/1488)	110	10 0100	62
24	48.387 (SCK/496)	010	01 0100	62
	44.117 (SCK/544)	010	01 0011	68
	32.258 (SCK/744)	010	11 0100	62
	24.193 (SCK/992)	100	01 0100	62
	22.058 (SCK/1088)	100	01 0011	68
	16.129 (SCK/1488)	100	11 0100	62
	12.096 (SCK/1984)	110	01 0100	62
	8.064 (SCK/2976)	110	11 0100	62
19.2	48.484 (SCK/396)	011	00 0110	66
	44.444 (SCK/432)	011	00 0101	72
	32.323 (SCK/594)	011	10 0110	66
	24.242 (SCK/792)	101	00 0110	66
	22.222 (SCK/864)	101	00 0101	72
	16.161 (SCK/1188)	101	10 0110	66
	12.121 (SCK/1584)	111	00 0110	66
	8.080 (SCK/2376)	111	10 0110	66

Table 10. System Clock Frequency for Application-Specific Clock (continued)

SYSTEM CLOCK SCK (MHz)	ADC SAMPLING RATE ADC f_S (kHz) / DAC SAMPLING RATE DAC f_S (kHz)	REGISTER SETTINGS		BIT CLOCK BCK (f_S)
		MSR[2:0]	NPR[5:0]	
38.4	48.484 (SCK/792)	011	01 0110	66
	44.444 (SCK/864)	011	01 0101	72
	32.323 (SCK/1188)	011	11 0110	66
	24.242 (SCK/1584)	101	01 0110	66
	22.222 (SCK/1728)	101	01 0101	72
	16.161 (SCK/2376)	101	11 0110	66
	12.121 (SCK/3168)	111	01 0110	66
	8.080 (SCK/4752)	111	11 0110	66
13	47.794 (SCK/272)	010	00 1000	68
	43.918 (SCK/296)	010	00 0111	74
	31.862 (SCK/408)	010	10 1000	68
	23.897 (SCK/544)	100	00 1000	68
	21.959 (SCK/592)	100	00 0111	74
	15.931 (SCK/816)	100	10 1000	68
	11.948 (SCK/1088)	110	00 1000	68
	7.965 (SCK/1632)	110	10 1000	68
26	47.794 (SCK/544)	010	01 1000	68
	43.918 (SCK/592)	010	01 0111	74
	31.862 (SCK/816)	010	11 1000	68
	23.897 (SCK/1088)	100	01 1000	68
	21.959 (SCK/1184)	100	01 0111	74
	15.931 (SCK/1632)	100	11 1000	68
	11.948 (SCK/2176)	110	01 1000	68
	7.965 (SCK/3264)	110	11 1000	68
19.68	48.235 (SCK/408)	011	00 1010	68
	44.324 (SCK/444)	011	00 1001	74
	32.156 (SCK/612)	011	10 1010	68
	24.117 (SCK/816)	101	00 1010	68
	22.162 (SCK/888)	101	00 1001	74
	16.078 (SCK/1224)	101	10 1010	68
	12.058 (SCK/1632)	111	00 1010	68
	8.039 (SCK/2448)	111	10 1010	68
39.36	48.235 (SCK/816)	011	01 1010	68
	44.324 (SCK/888)	011	01 1001	74
	32.156 (SCK/1224)	011	11 1010	68
	24.117 (SCK/1632)	101	01 1010	68
	22.162 (SCK/1776)	101	01 1001	74
	16.078 (SCK/2448)	101	11 1010	68
	12.058 (SCK/3264)	111	01 1010	68
	8.039 (SCK/4896)	111	11 1010	68

MBST: BCK Output Configuration in Master Mode

Default value: 0

This bit is used to control the BCK output configuration in master mode. In master mode, this bit sets the BCK output configuration to normal mode or burst mode. In normal mode (MBST = 0), the BCK clock runs continuously. In burst mode (MBST = 1), the BCK clock runs intermittently, and the number of clock cycles per LRCK period is reduced to equal the number of bits of audio data being transmitted. Operating in burst mode reduces the power consumption of V_{IO} (I/O cell power supply). This is effective in master mode (register 69 MSTR = 1).

MBST = 0	Normal mode (default)
MBST = 1	Burst mode

ZCRS: Zero-Cross for Digital Attenuation/Mute and Analog Gain Setting

Default value: 0

This bit is used to enable the zero-cross detector, which reduces zipper noise while the digital soft mute, digital attenuation analog gain setting, or analog volume setting is being changed. If no zero-cross data is input for a $512/f_S$ period (10.6 ms at a 48-kHz sampling rate), then a time-out occurs and the PCM1774 starts changing the attenuation, gain, or volume level. The zero-cross detector cannot be used with continuous-zero and dc data.

ZCRS = 0	Zero-cross disabled (default)
ZCRS = 1	Zero-cross enabled

Register 87

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 87	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	AIR1	AIR0	RSV	RSV	AIL1	AIL0

IDX[6:0]: 101 0111b (57h): Register 87

AIL0: AIN1L Selector (MUX1)

Default value: 0

This bit is used to select the analog input, AIN1L.

AIL0	**AIN L-channel Select**
0	Disconnect (default)
1	AIN1L

AIR0: AIN1R Selector (MUX2)

Default value: 0

This bit is used to select one of the three stereo analog inputs, AIN1R.

AIR0	**AIN R-channel Select**
0	Disconnect (default)
1	AIN1R

Register 88

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 88	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	MXR2	MXR1	MXR0	RSV	MXL2	MXL1	MXL0

IDX[6:0]: 101 1000b (58h): Register 88

MXR2: Mixing SW6 to MXR (R-Channel Mixing Amplifier) From L-Channel Analog Input

Default value: 0

This bit is used to mix the analog source into MXR (R-ch mixing amplifier) from the L-ch analog input.

MXR2 = 0	Disable (default)
MXR2 = 1	Enable

MXR1: Mixing SW4 to MXR (R-Channel Mixing Amplifier) From R-Channel Analog Input

Default value: 0

This bit is used to mix the analog source into MXR (R-ch mixing amplifier) from the R-ch analog input.

MXR1 = 0	Disable (default)
MXR1 = 1	Enable

MXR0: Mixing SW5 to MXR (R-Channel Mixing Amplifier) From R-Channel DAC

Default value: 0

This bit is used to mix the analog source into MXR (R-ch mixing amplifier) from the R-ch DAC.

MXR0 = 0	Disable (default)
MXR0 = 1	Enable

MXL2: Mixing SW3 to MXL (L-Channel Mixing Amplifier) From R-Channel Analog Input

Default value: 0

This bit is used to mix the analog source into MXL (L-ch mixing amplifier) from the R-ch analog input.

MXL2 = 0	Disable (default)
MXL2 = 1	Enable

MXL1: Mixing SW1 to MXL (L-Channel Mixing Amplifier) From L-Channel Analog Input

Default value: 0

This bit is used to mix the analog source into MXL (L-ch mixing amplifier) from the L-ch analog input.

MXL1 = 0	Disable (default)
MXL1 = 1	Enable

MXL0: Mixing SW2 to MXL (L-Channel Mixing Amplifier) From L-Channel DAC

Default value: 0

This bit is used to mix the analog source into MXL (L-ch mixing amplifier) from the L-ch DAC.

MXL0 = 0	Disable (default)
MXL0 = 1	Enable

Register 89

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 89	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	GMR2	GMR1	GMR0	RSV	GML2	GML1	GML0

IDX[6:0]: 101 1001b (59h): Register 89

GMR[2:0]: Gain Level Control for PG6 (Gain Amplifier for Analog Input or R-Channel Bypass)

GML[2:0]: Gain Level Control for PG5 (Gain Amplifier for Analog Input or L-Channel Bypass)

Default value: 000

These bits are used for setting the gain level of the analog source to the mixing amplifier. It is recommended to set the gain level to avoid saturation in the analog mixer.

GMR[2:0] GML[2:0]	Gain Level Control for PG6 Gain Level Control for PG5
0 0 0	–21 dB (default)
0 0 1	–18 dB
0 1 0	–15 dB
0 1 1	–12 dB
1 0 0	–9 dB
1 0 1	–6 dB
1 1 0	–3 dB
1 1 1	0 dB

Register 90

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 90	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	G20R	G20L

IDX[6:0]: 101 1010b (5Ah): Register 90

G20R: 20-dB Boost for PG2 (Gain Amplifier for AIN1R)

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

G12R (REGISTER 124)	G20R (REGISTER 90)	PG2 GAIN
0	0	0 dB (default)
0	1	20 dB
1	0	12 dB
1	1	Reserved

G20L: 20-dB Boost for PG1 (Gain Amplifier for AIN1L)

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

G12L (REGISTER 124)	G20L (REGISTER 90)	PG1 GAIN
0	0	0 dB (default)
0	1	20 dB
1	0	12 dB
1	1	Reserved

Register 92

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 92	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	LPAE	RSV	RSV	LGA4	LGA3	LGA2	LGA1	LGA0

IDX[6:0]: 101 1100b (5Ch): Register 92

LPAE: Gain Adjustment for Bass Boost Gain Control

Default value: 0

A gain setting for bass boost may cause digital data saturation, depending on the input data level. Where this could occur, LPAE can be used to set the same attenuation level as the bass boost gain level for the digital input data.

LPAE = 0	Disable (default)
LPAE = 1	Enable

LGA[4:0]: Bass Boost Gain Control

Default value: 0 0000

These bits are used to set the bass boost gain level for the digital data. The detailed characteristics are shown in the *Typical Performance Curves*.

LGA[4:0]	TONE CONTROL GAIN (BASS)	LGA[4:0]	TONE CONTROL GAIN (BASS)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	–1 dB
0 0100	11 dB	1 0001	–2 dB
0 0101	10 dB	1 0010	–3 dB
0 0110	9 dB	1 0011	–4 dB
0 0111	8 dB	1 0100	–5 dB
0 1000	7 dB	1 0101	–6 dB
0 1001	6 dB	1 0110	–7 dB
0 1010	5 dB	1 0111	–8 dB
0 1011	4 dB	1 1000	–9 dB
0 1100	3 dB	1 1001	–10 dB
0 1101	2 dB	1 1010	–11 dB
0 1110	1 dB	1 1011	–12 dB

Register 93

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 93	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	MGA4	MGA3	MGA2	MGA1	MGA0

IDX[6:0]: 101 1101b (5Dh): Register 93

MGA[4:0]: Middle Boost Gain Control

Default value: 0 0000

These bits are used to set the midrange boost gain level for the digital data. The detailed characteristics are shown in the *Typical Performance Curves*.

MGA[4:0]	TONE CONTROL GAIN (MIDRANGE)	MGA[4:0]	TONE CONTROL GAIN (MIDRANGE)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	–1 dB
0 0100	11 dB	1 0001	–2 dB
0 0101	10 dB	1 0010	–3 dB
0 0110	9 dB	1 0011	–4 dB
0 0111	8 dB	1 0100	–5 dB
0 1000	7 dB	1 0101	–6 dB
0 1001	6 dB	1 0110	–7 dB
0 1010	5 dB	1 0111	–8 dB
0 1011	4 dB	1 1000	–9 dB
0 1100	3 dB	1 1001	–10 dB
0 1101	2 dB	1 1010	–11 dB
0 1110	1 dB	1 1011	–12 dB

Register 94

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 94	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	HGA4	HGA3	HGA2	HGA1	HGA0

IDX[6:0]: 101 1110b (5Eh): Register 94

HGA[4:0]: Treble Boost Gain Control (f_C = 5 kHz)

Default value: 0 0000

These bits are used to set the treble boost gain level for the digital data. The detailed characteristics are shown in the *Typical Performance Curves*.

HGA[4:0]	TONE CONTROL GAIN (TREBLE)	HGA[4:0]	TONE CONTROL GAIN (TREBLE)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	–1 dB
0 0100	11 dB	1 0001	–2 dB
0 0101	10 dB	1 0010	–3 dB
0 0110	9 dB	1 0011	–4 dB
0 0111	8 dB	1 0100	–5 dB
0 1000	7 dB	1 0101	–6 dB
0 1001	6 dB	1 0110	–7 dB
0 1010	5 dB	1 0111	–8 dB
0 1011	4 dB	1 1000	–9 dB
0 1100	3 dB	1 1001	–10 dB
0 1101	2 dB	1 1010	–11 dB
0 1110	1 dB	1 1011	–12 dB

Register 95

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 95	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	3DEN	RSV	3FL0	3DP3	3DP2	3DP1	3DP0

IDX[6:0]: 101 1111b (5Fh): Register 95

3DEN: 3-D Sound Effect Enable

Default value: 0

This bit is used for enabling the 3-D sound effect filter. This filter has two independently controlled parameters.

3DEN = 0	Disable (default)
3DEN = 1	Enable

3FL0: Filter Selection for 3-D Sound

Default value: 0

This bit is used for selecting from two types of filter, narrow and wide. These filters have a different 3-D performance effect.

3FL0 = 0	Narrow (default)
3FL0 = 1	Wide

3DP[3:0]: Efficiency for 3-D Sound Effects

Default value: 0000

These bits are used for adjusting the 3-D sound efficiency. Higher percentages have greater efficiency.

3DP[3:0]	**3D Sound Effect Efficiency**
0 0 0 0	0% (default)
0 0 0 1	10%
0 0 1 0	20%
0 0 1 1	30%
0 1 0 0	40%
0 1 0 1	50%
0 1 1 0	60%
0 1 1 1	70%
1 0 0 0	80%
1 0 0 1	90%
1 0 1 0	100%
1 0 1 1	Reserved
:	:
1 1 1 1	Reserved

Register 96

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 96	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RSV	MXEN

IDX[6:0]: 110 0000b (60h): Register 96

MXEN: Digital Monaural Mixing

Default value: 0

This bit is used to enable or disable monaural mixing in the section that combines L-ch data and R-ch data.

MXEN = 0	Stereo (default)
MXEN = 1	Monaural Mixing

Register 124

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 124	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	G12R	G12L

IDX[6:0]: 111 1100b (7Ch): Register 124

G12R: 12 dB Boost for PG2 (Gain Amp for AIN1R and AIN2R)

G12L: 12 dB Boost for PG1 (Gain Amp for AIN1L and AIN2L)

Default value: 0

This bit is used to boost a small analog signal, microphone input. See Register 90 information for the detail settings.

Register 125

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 125	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PTM1	PTM0	RES4	RES3	RES2	RES1	RES0

IDX[6:0]: 111 1101b (7Dh): Register 125

PTM[1:0]: Power-Up/Down Time Control

Default value: 00

RES[4:0]: Resister Value Control

Default value: 1 1100

These bits are used to optimize audible pop noise and ramp up time for headphone output at device power on/off.

Table 11. Power Up/Down Time Control

RES[1:0]	V_{COM} REGISTER VALUE
1 0000	60 kΩ
1 1000	24 kΩ
1 1100	12 kΩ
1 1110	6 kΩ
Others	Reserved

V_{COM} CAPACITOR [µF]	RES[4:0]	PTM[1:0]	POWER-UP TIME [ms]	POWER-DOWN TIME [ms]	NOTE
10	1 1110	00	450	750	
	1 1100	11	900	1500	
	1 1000	Do not set.	–	–	
	1 0000	Do not set.	–	–	
4.7	1 1110	01	250	400	
	1 1100	00	450	750	Default
	1 1000	11	900	1500	
	1 0000	Do not set.	–	–	
2.2	1 1110	10	100	300	
	1 1100	01	250	400	
	1 1000	00	450	750	
	1 0000	11	900	1500	
1	1 1110	Do not set.	–	–	
	1 1100	10	100	300	
	1 1000	01	250	400	
	1 0000	00	450	750	

CONNECTION DIAGRAMS

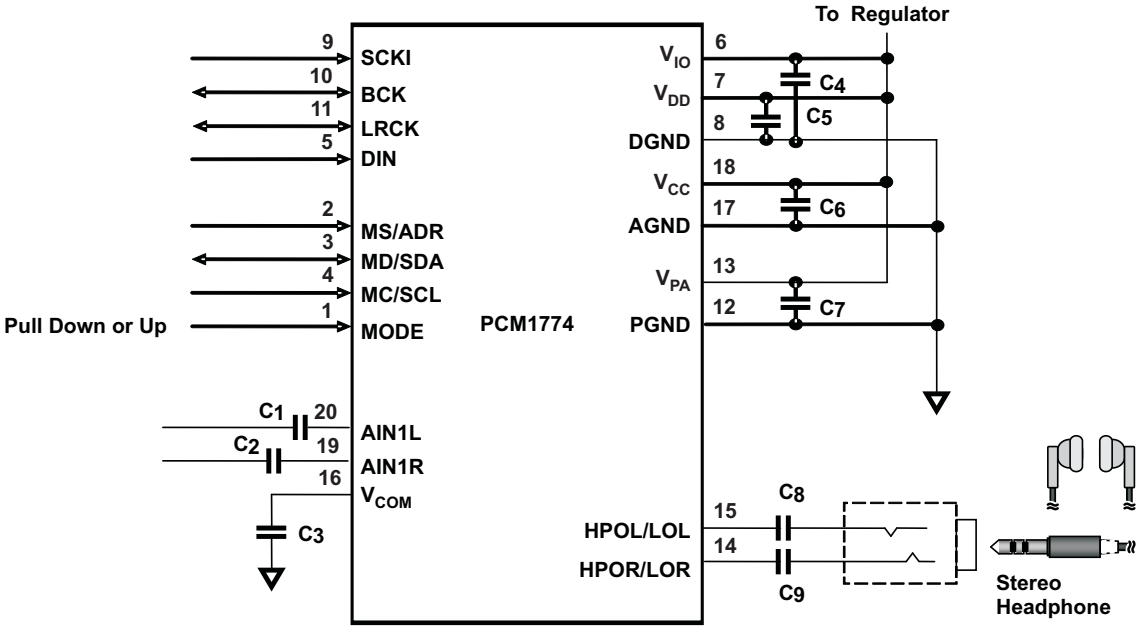
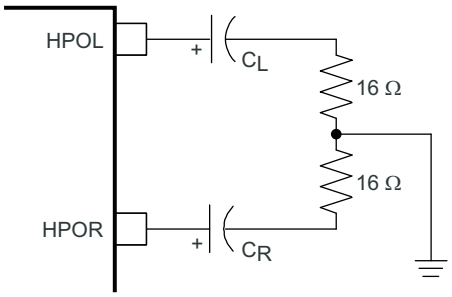


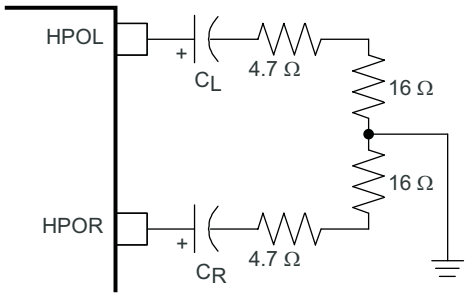
Figure 24. Connection Diagram

Table 12. Recommended External Parts

C_1–C_2	1 µF
C_3	1–4.7 µF
C_4	0.1 µF
C_5, C_6, C_7	1–4.7 µF
C_8, C_9	10–220 µF



C_L, C_R – µF	f_C – Hz
10	995
47	212
100	100
220	45



C_L, C_R – µF	f_C – Hz
10	770
47	163
100	77
220	35

S0223-01

Figure 25. High-Pass Filter for Headphone Output

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCM1774RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1774	Samples
PCM1774RGPRG4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1774	Samples
PCM1774RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1774	Samples
PCM1774RGPTG4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1774	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

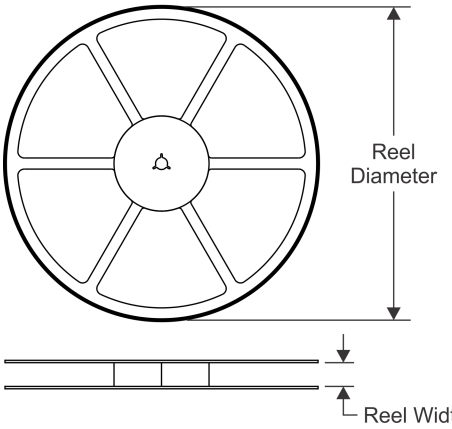
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

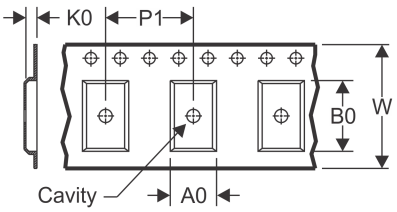
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

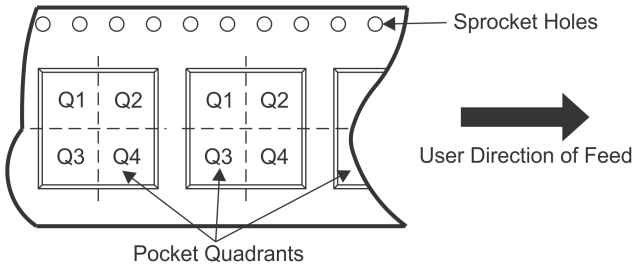


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

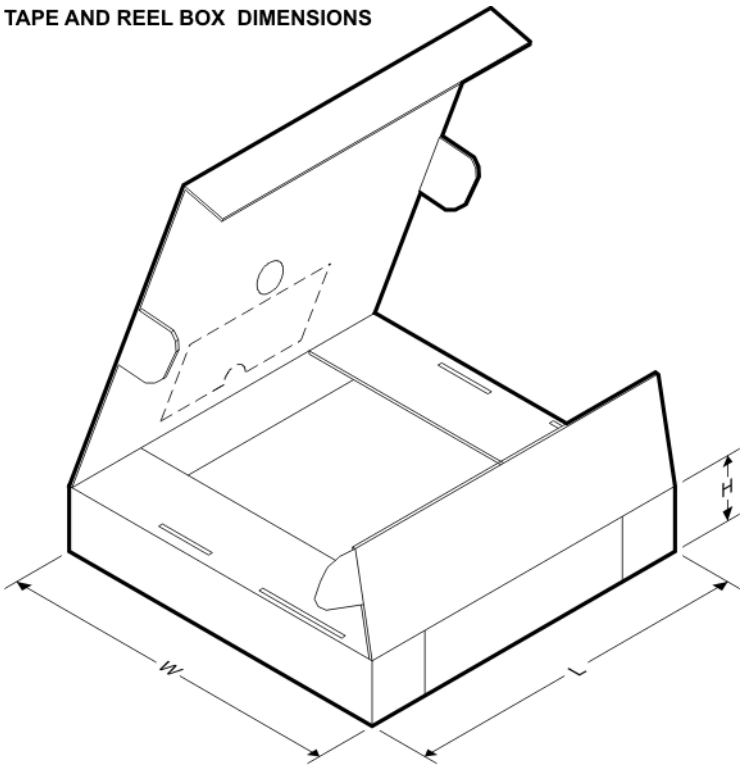
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1774RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCM1774RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCM1774RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCM1774RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

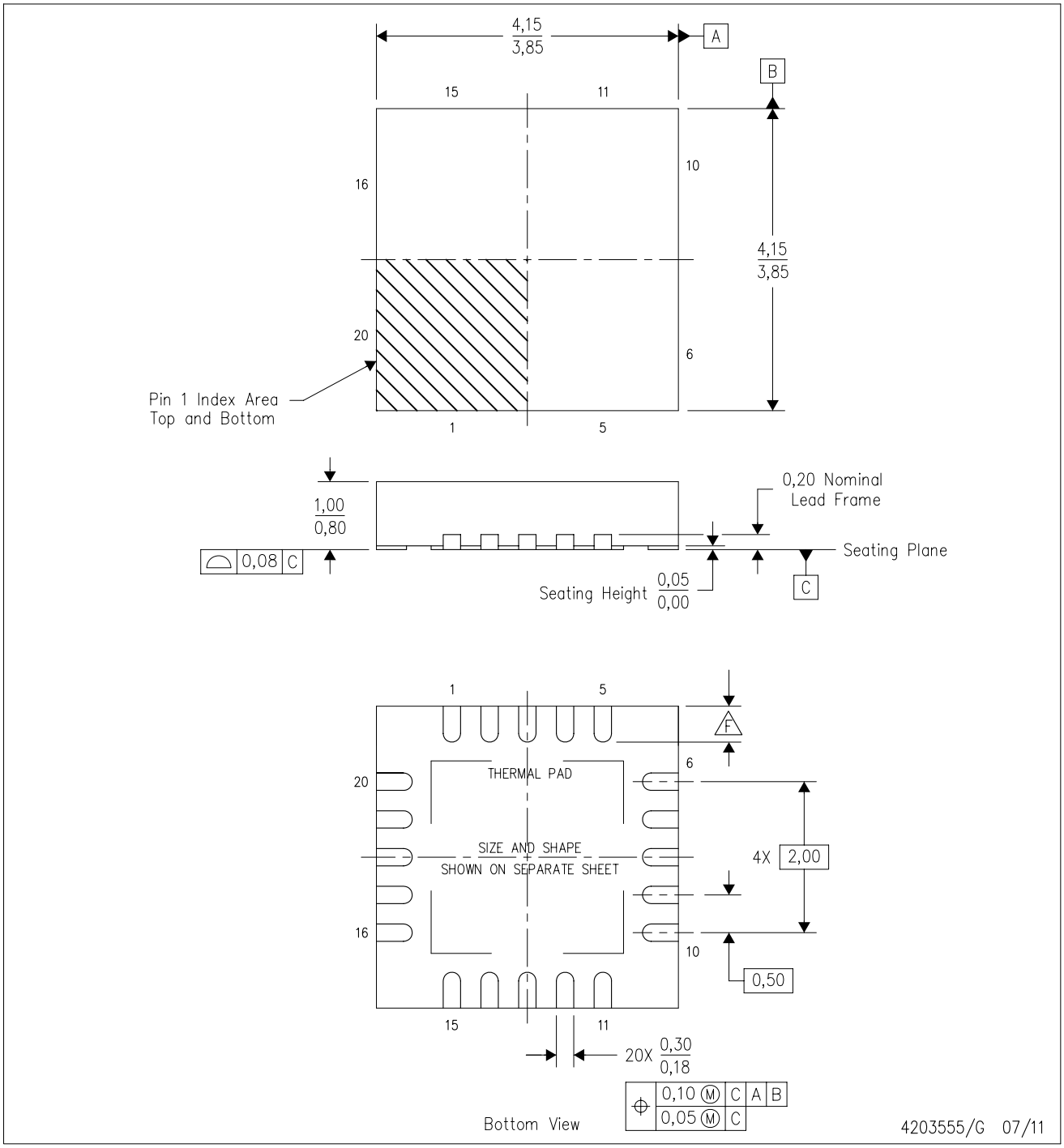
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1774RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
PCM1774RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
PCM1774RGPT	QFN	RGP	20	250	210.0	185.0	35.0
PCM1774RGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

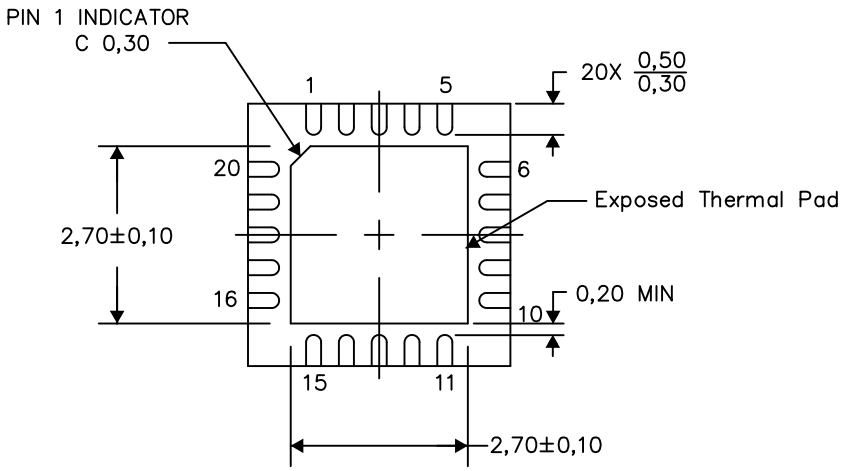
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



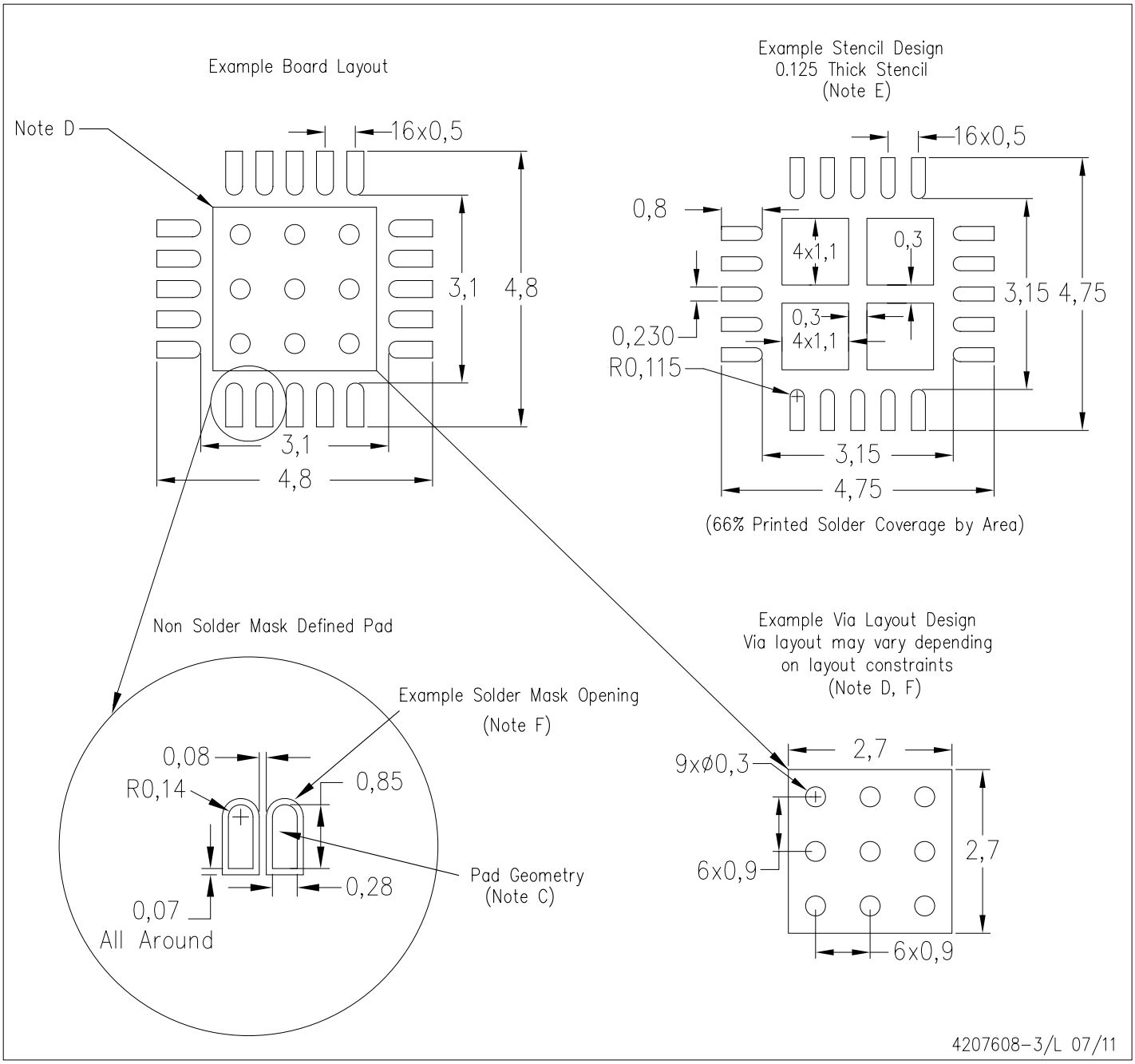
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/Z 04/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

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