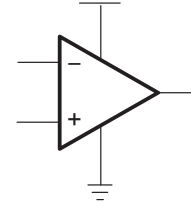


TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

- Supply Current . . . 23 μ A/Channel
- Gain-Bandwidth Product . . . 220 kHz
- Output Drive Capability . . . ± 10 mA
- Input Offset Voltage . . . 20 μ V (typ)
- V_{DD} Range . . . 2.7 V to 6 V
- Power Supply Rejection Ratio . . . 106 dB
- Ultralow-Power Shutdown Mode
 I_{DD} . . . 16 nA/ch
- Rail-To-Rail Input/Output (RRIO)
- Ultrasmall Packaging
 - 5 or 6 Pin SOT-23 (TLV2450/1)
 - 8 or 10 Pin MSOP (TLV2452/3)

Operational Amplifier



description

The TLV245x is a family of rail-to-rail input/output operational amplifiers that sets a new performance point for supply current and ac performance. These devices consume a mere 23 μ A/channel while offering 220 kHz of gain-bandwidth product, much higher than competitive devices with similar supply current levels. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower rail-to-rail input/output operational amplifiers. The TLV245x can swing to within 250 mV of each supply rail while driving a 2.5-mA load. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV245x family ideal for portable medical equipment, patient monitoring systems, and data acquisition circuits.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2450	1	8	8	6	—	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2451	1	8	8	5	—	—	—	
TLV2452	2	8	8	—	—	8	—	
TLV2453	2	14	14	—	—	10	Yes	
TLV2454	4	14	14	—	14	—	—	
TLV2455	4	16	16	—	16	—	Yes	

A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	BW (MHz)	SLEW RATE (V/ μ s)	I_{DD} (per channel) (μ A)	RAIL-TO-RAIL
TLV245X	2.7 – 6.0	0.22	0.11	23	I/O
TLV247X	2.7 – 6.0	2.8	1.5	600	I/O
TLV246X	2.7 – 6.0	6.4	1.6	550	I/O
TLV277X	2.5 – 6.0	5.1	10.5	1000	O

† All specifications measured at 5 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



WWW.TI.COM
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1998–2005, Texas Instruments Incorporated

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

description (continued)

Three members of the family (TLV2450/3/5) offer a shutdown terminal for conserving battery life in portable applications. During shutdown, the outputs are placed in a high-impedance state and the amplifier consumes only 16 nA/channel. The family is fully specified at 3 V and 5 V across an expanded industrial temperature range (-40°C to 125°C). The singles and duals are available in the SOT23 and MSOP packages, while the quads are available in TSSOP. The TLV2450 offers an amplifier with shutdown functionality all in a 6-pin SOT23 package, making it perfect for high density circuits.

TLV2450 and TLV2451 AVAILABLE OPTIONS

T _A	PACKAGED DEVICES			
	SMALL OUTLINE (D) [†]	SOT-23		PLASTIC DIP (P)
		(DBV)	SYMBOL	
0°C to 70°C	TLV2450CD TLV2451CD	TLV2450CDBV TLV2451CDBV	VAQC VARC	TLV2450CP TLV2451CP
-40°C to 125°C	TLV2450ID TLV2451ID	TLV2450IDBV TLV2451IDBV	VAQI VARI	TLV2450IP TLV2451IP
	TLV2450AID TLV2451AID	— —	— —	TLV2450AIP TLV2451AIP

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2450CDR).

TLV2452 and TLV2453 AVAILABLE OPTIONS

T _A	PACKAGED DEVICES						
	SMALL OUTLINE (D) [†]	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
		(DGK) [†]	SYMBOL [‡]	(DGS) [†]	SYMBOL [‡]		
0°C to 70°C	TLV2452CD TLV2453CD	TLV2452CDGK —	xxTIABI —	— TLV2453CDGS	— xxTIABK	— TLV2453CN	TLV2452CP —
-40°C to 125°C	TLV2452ID TLV2453ID	TLV2452IDGK —	xxTIABJ —	— TLV2453IDGS	— xxTIABL	— TLV2453IN	TLV2452IP —
	TLV2452AID TLV2453AID	— —	— —	— —	— —	— TLV2453AIN	TLV2452AIP —

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2452CDR).

[‡] xx represents the device date code.

TLV2454 and TLV2455 AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		
	SMALL OUTLINE (D) [†]	PLASTIC DIP (N)	TSSOP (PW) [†]
0°C to 70°C	TLV2454CD TLV2455CD	TLV2454CN TLV2455CN	TLV2454CPW TLV2455CPW
-40°C to 125°C	TLV2454ID TLV2455ID	TLV2454IN TLV2455IN	TLV2454IPW TLV2455IPW
	TLV2454AID TLV2455AID	TLV2454AIN TLV2455AIN	TLV2454AIPW TLV2455AIPW

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2454CDR).

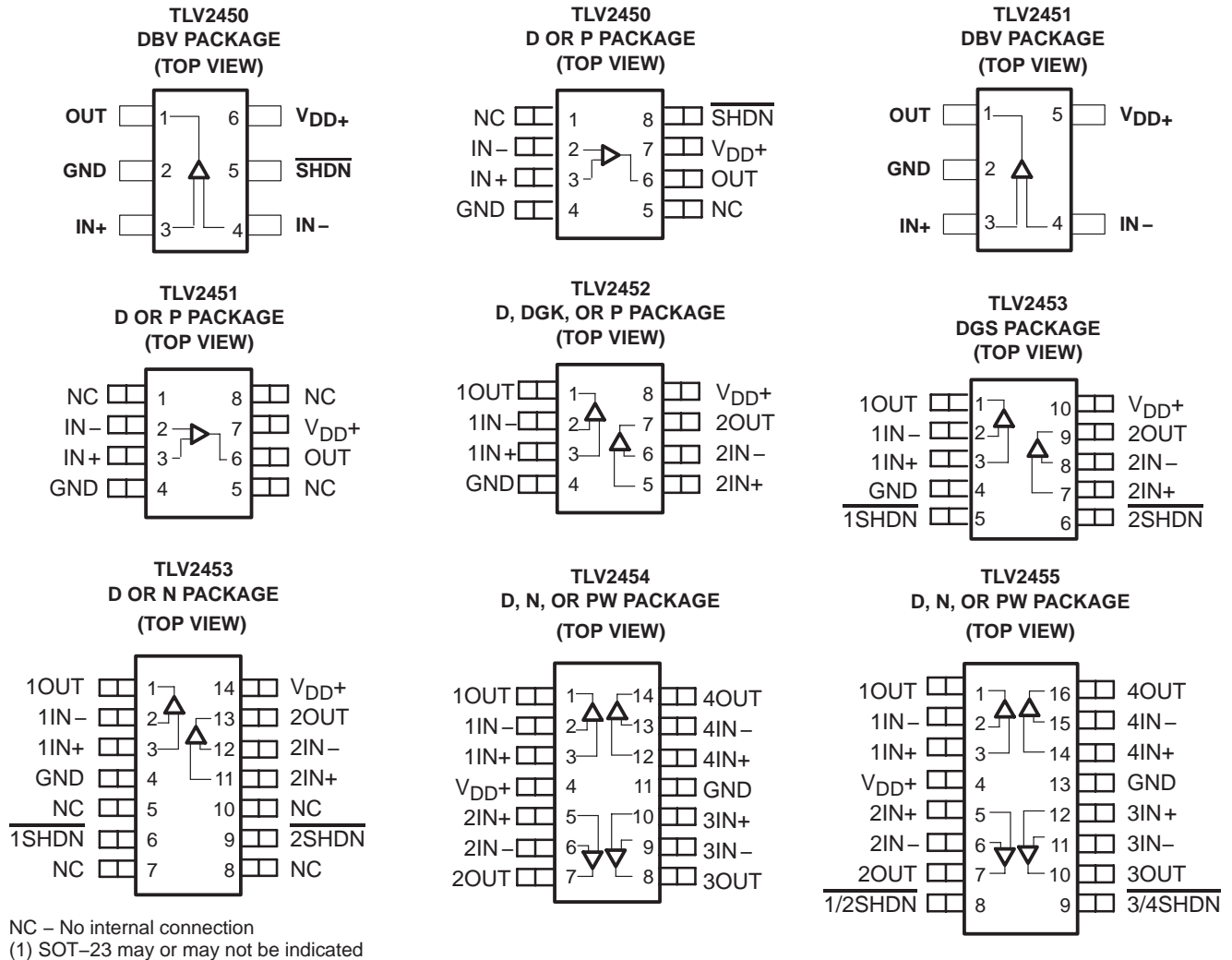
NOTE: For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.



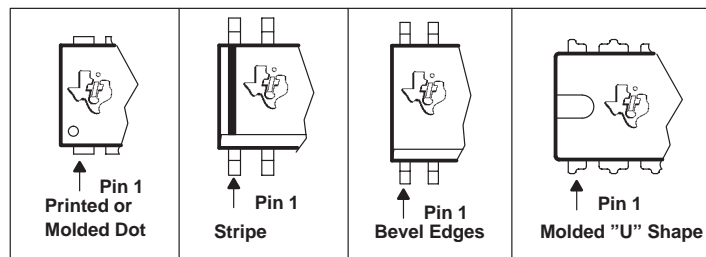
TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TLV245x PACKAGE PINOUTS(1)



TYPICAL PIN 1 INDICATORS



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA

FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	7 V
Differential input voltage, V_{ID}	$\pm V_{DD}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	-40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.2	259.9	481 mW
DGS (10)	54.1	257.7	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	± 1.35	± 3	
Common-mode input voltage range, V_{ICR}		0	V_{DD}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	-40	125	
Shutdown on/off voltage level [‡]	V_{IH}	2		V
	V_{IL}	$V_{DD} = 5V$	0.8	
		$V_{DD} = 3V$	0.5	V

[‡] Relative to voltage on the GND terminal of the device.



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x	$V_{DD} = \pm 1.5\text{ V}$ $V_{IC} = 0,$ $V_O = 0,$ $R_S = 50\ \Omega$	25°C	300	1500		μV
				Full range		2000		
		TLV245xA		25°C	300	1000		
				Full range		1300		
α_{VIO}	Temperature coefficient of input offset voltage					0.3		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current			25°C		0.3	4.5	nA
				Full range			5.5	
I_{IB}	Input bias current			25°C		0.9	5	nA
				Full range			7	
V_{OH}	High-level output voltage	$V_{IC} = 1.5\text{ V},$	$I_{OH} = -500\ \mu\text{A}$	25°C	2.85	2.95		V
				Full range	2.83			
V_{OL}	Low-level output voltage	$V_{IC} = 1.5\text{ V},$	$I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.16	V
				Full range			0.2	
I_{OS}	Short-circuit output current	Sourcing		25°C	4	12		mA
				Full range	3			
		Sinking		25°C	2	7		
				Full range	1			
I_O	Output current	$V_O = 0.5\text{ V}$ from rail		25°C		± 4		mA
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = 1\text{ V},$	$R_L = 10\text{ k}\Omega$	25°C	96	110		dB
				Full range	91			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
C_{IC}	Common-mode input capacitance	$f = 10\text{ kHz}$		25°C		4.5		pF
z_o	Closed-loop output impedance	$f = 10\text{ kHz},$	$A_V = 10$	25°C		80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }3\text{ V},$ $R_S = 50\ \Omega$	TLV245xC	25°C	70	80		dB
				Full range	66			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }6\text{ V},$ No load	$V_{IC} = V_{DD}/2,$	25°C	76	89		dB
				Full range	74			
		$V_{DD} = 3\text{ V to }5\text{ V},$ No load	$V_{IC} = V_{DD}/2,$	25°C	88	106		
				Full range	84			
I_{DD}	Supply current (per channel)	$V_O = 1.5\text{ V},$ No load	TLV245xC	25°C		23	35	μA
				Full range			40	
				TLV245xl	Full range			
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)	$\overline{\text{SHDN}} = -V_{DD}$	TLV245xC	25°C		12	65	nA
				Full range			70	
				TLV245xl	Full range			

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for l suffix.



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	MIN	TYP	MAX	UNIT	
SR	Slew rate at unity gain	$V_{O(PP)} = 0.8\text{ V}$, $R_L = 10\text{ k}\Omega$	$C_L = 150\text{ pF}$	25°C	0.05	0.11		V/ μ s	
				Full range	0.02				
V_n	Equivalent input noise voltage	f = 100 Hz		25°C	49			nV/ $\sqrt{\text{Hz}}$	
		f = 1 kHz		25°C	51				
I_n	Equivalent input noise current	f = 1 kHz		25°C	3.5			pA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 1.5\text{ V}$, $R_L = 10\text{ k}\Omega$, f = 1 kHz	$A_V = 1$	25°C	0.04%				
					$A_V = 10$	0.3%			
						$A_V = 100$	1.5%		
$t_{(on)}$	Amplifier turnon time	$A_V = 5$, $R_L = \text{OPEN}$,		25°C	59		μ s		
$t_{(off)}$	Amplifier turnoff time	Measured at 50% point		25°C	836		ns		
Gain-bandwidth product		f = 10 kHz,	$R_L = 10\text{ k}\Omega$	25°C	200			kHz	
t_s	Settling time	$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%	25°C	26		μ s		
			0.01%		31				
		$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 56\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%		26				
			0.01%		31				
ϕ_m	Phase margin	$R_L = 10\text{ k}\Omega$,	$C_L = 1000\text{ pF}$	25°C	56°				
Gain margin		$R_L = 10\text{ k}\Omega$,	$C_L = 1000\text{ pF}$	25°C	7			dB	

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix.



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	MIN	TYP	MAX	UNIT	
V_{IO}	Input offset voltage			25°C		300	1500	μ V	
				Full range			2000		
				25°C		300	1000		
				Full range			1300		
α_{VIO}	Temperature coefficient of input offset voltage		$V_{DD} = \pm 2.5$ V $V_{IC} = 0$, $V_O = 0$, $R_S = 50$ Ω			0.3		μ V/°C	
I_{IO}	Input offset current			25°C		0.3	4.5	nA	
				Full range			5.5		
I_{IB}	Input bias current			25°C		0.5	5	nA	
				Full range			7		
V_{OH}	High-level output voltage		$V_{IC} = 2.5$ V, $I_{OH} = -500$ μ A	25°C	4.87	4.97		V	
				Full range	4.85				
V_{OL}	Low-level output voltage		$V_{IC} = 2.5$ V, $I_{OL} = 500$ μ A	25°C		0.07	0.15	V	
				Full range			0.16		
I_{OS}	Short-circuit output current			Sourcing		25°C	20	32	mA
				Full range		18			
				Sinking		25°C	12	18	
				Full range		10			
I_O	Output current		$V_O = 0.5$ V from rail	25°C		± 10		mA	
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)} = 3$ V, $R_L = 10$ k Ω	25°C	96	103		dB	
				Full range	91				
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω	
C_{IC}	Common-mode input capacitance		$f = 10$ kHz	25°C		4.5		pF	
z_o	Closed-loop output impedance		$f = 10$ kHz, $A_V = 10$	25°C		45		Ω	
CMRR	Common-mode rejection ratio		$V_{IC} = 0$ to 5 V, $R_S = 50$ Ω	25°C	70	80		dB	
				Full range	68				
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		$V_{DD} = 2.7$ V to 6 V, No load $V_{IC} = V_{DD}/2$	25°C	76	89		dB	
				Full range	74				
				25°C	88	106			
				Full range	84				
I_{DD}	Supply current (per channel)		$V_O = 2.5$ V, No load	25°C		23	42	μ A	
				Full range			44		
				Full range			46		
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)		$\overline{SHDN} = -V_{DD}$	25°C		16	70	nA	
				Full range			70		
				Full range			80		

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix.



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$	$C_L = 150\text{ pF}$	25°C	0.05	0.11		V/ μ s
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz		25°C		52		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 3\text{ V}$, $R_L = 10\text{ k}\Omega$, f = 1 kHz		25°C		$A_V = 1$	0.02%	
						$A_V = 10$	0.18%	
						$A_V = 100$	0.9%	
$t_{(on)}$	Amplifier turnon time	$A_V = 5$, $R_L = \text{OPEN}$,		25°C		59		μ s
$t_{(off)}$	Amplifier turnoff time	Measured at 50% point		25°C		836		ns
	Gain-bandwidth product	f = 10 kHz,	$R_L = 10\text{ k}\Omega$	25°C		220		kHz
t_s	Settling time	$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%	25°C		24	μ s	
			0.01%			30		
		$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 56\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%			25		
			0.01%			30		
ϕ_m	Phase margin	$R_L = 10\text{ k}\Omega$,	$C_L = 1000\text{ pF}$	25°C		56°		
	Gain margin	$R_L = 10\text{ k}\Omega$,	$C_L = 1000\text{ pF}$	25°C		7		dB

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix.



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Common-mode input voltage vs Free-air temperature	3, 4 7, 8
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5, 6 7, 8
A_{VD}	Differential voltage amplification	vs Frequency	9, 10
	Phase	vs Frequency	9, 10
V_{OL}	Low-level output voltage	vs Low-level output current	11, 13
V_{OH}	High-level output voltage	vs High-level output current	12, 14
Z_o	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
PSRR	Power supply rejection ratio	vs Frequency	18
I_{DD}	Supply current	vs Supply voltage	19
I_{DD}	Supply current	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD + N	Total harmonic distortion plus noise	vs Frequency	22, 23
ϕ_m	Phase margin	vs Load capacitance	24
	Gain-bandwidth product	vs Supply voltage	25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	28
	Crosstalk	vs Frequency	29, 30
	Small-signal follower pulse response	vs Time	31, 33
	Large-signal follower pulse response	vs Time	32, 34
	Shutdown on supply current	vs Time	35
	Shutdown off supply current	vs Time	36
	Shutdown supply current	vs Free-air temperature	37
	Shutdown supply current	vs Time	38 – 41
	Shutdown pulse	vs Time	38 – 41
	Shutdown off pulse response	vs Time	42, 43
	Shutdown on pulse response	vs Time	44, 45
	Shutdown reverse isolation	vs Frequency	46
	Shutdown forward isolation	vs Frequency	47



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

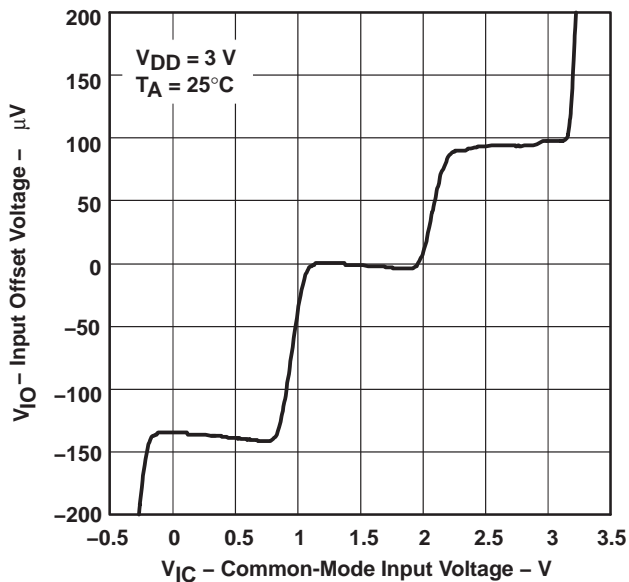


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

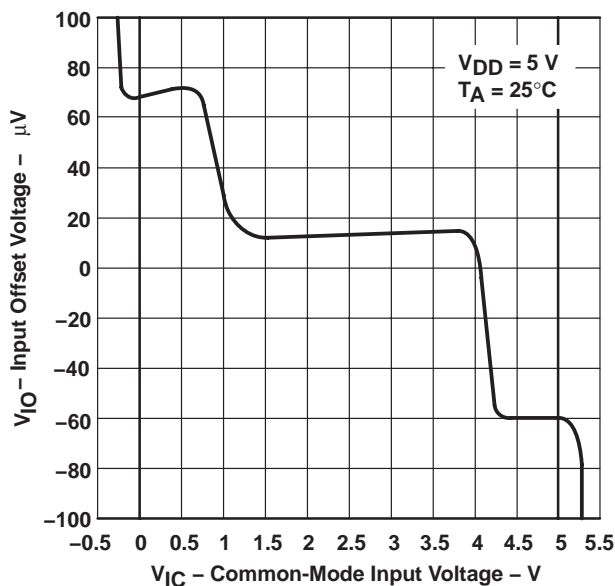


Figure 2

INPUT OFFSET CURRENT
vs
COMMON-MODE INPUT VOLTAGE

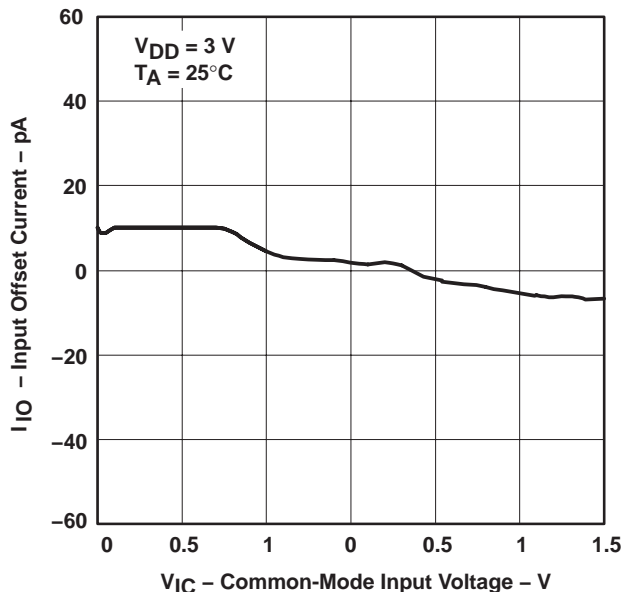


Figure 3

INPUT OFFSET CURRENT
vs
COMMON-MODE INPUT VOLTAGE

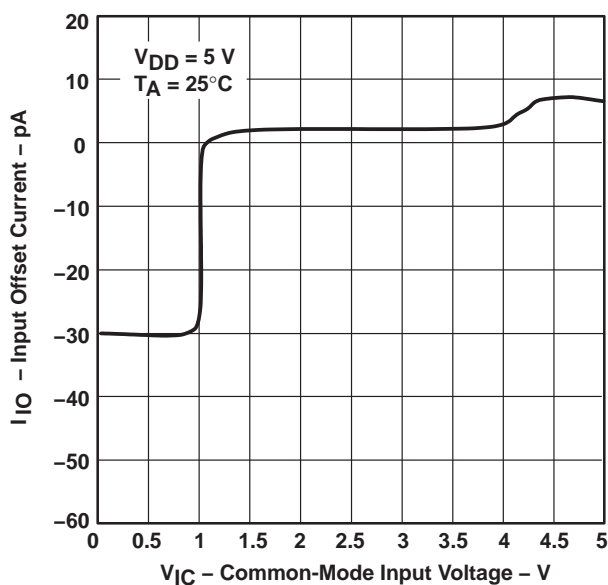


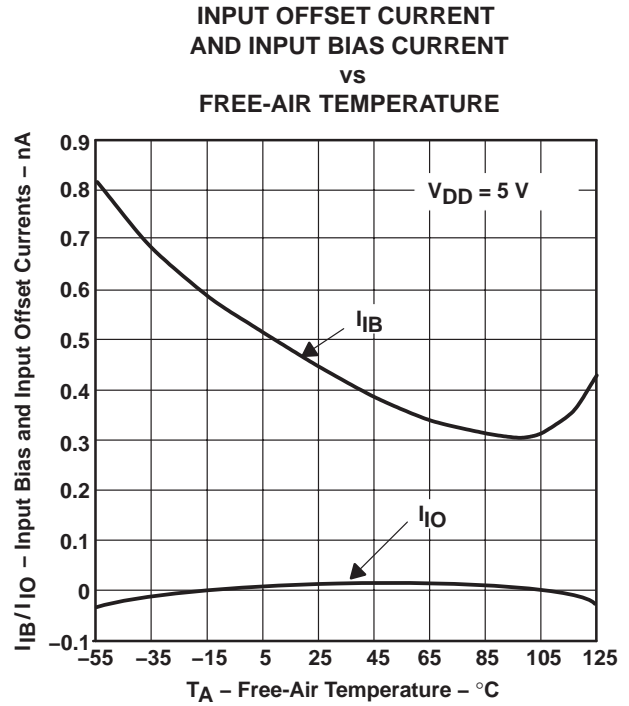
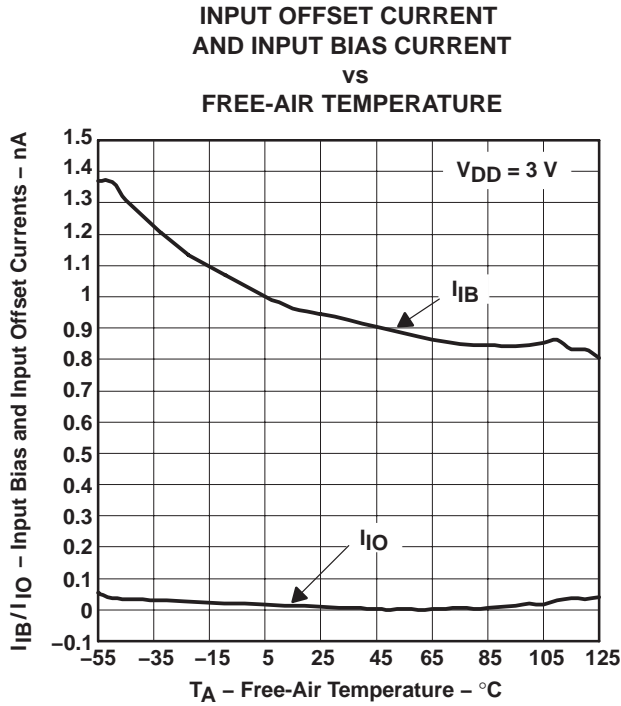
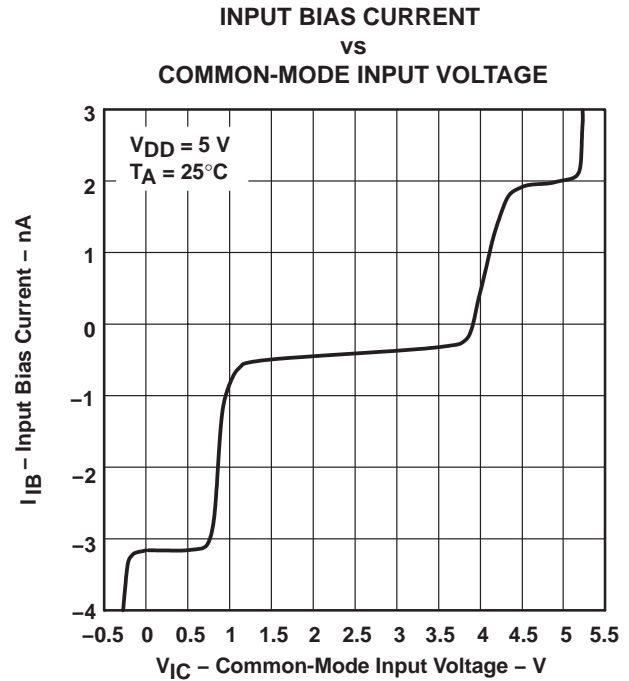
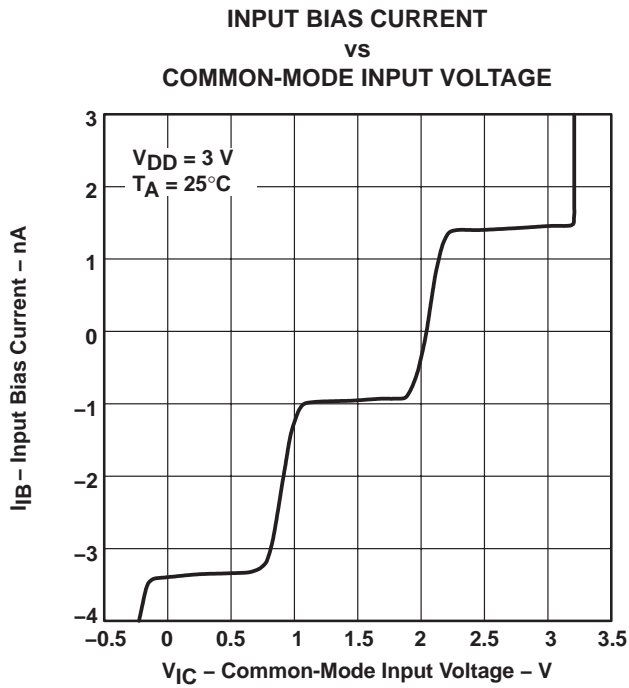
Figure 4



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-KHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE
vs
FREQUENCY



Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE
vs
FREQUENCY



Figure 10



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-KHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

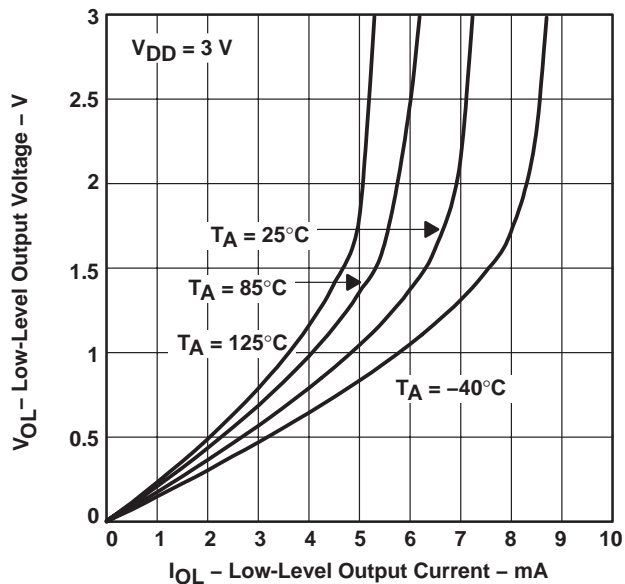


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
 vs
 HIGH-LEVEL OUTPUT CURRENT

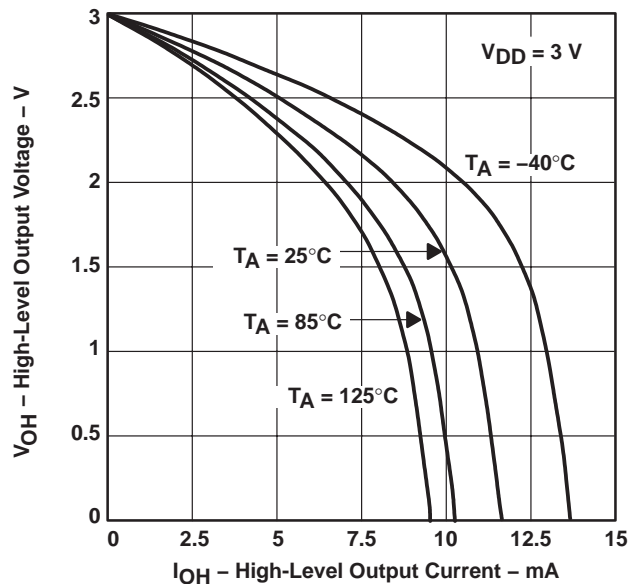


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

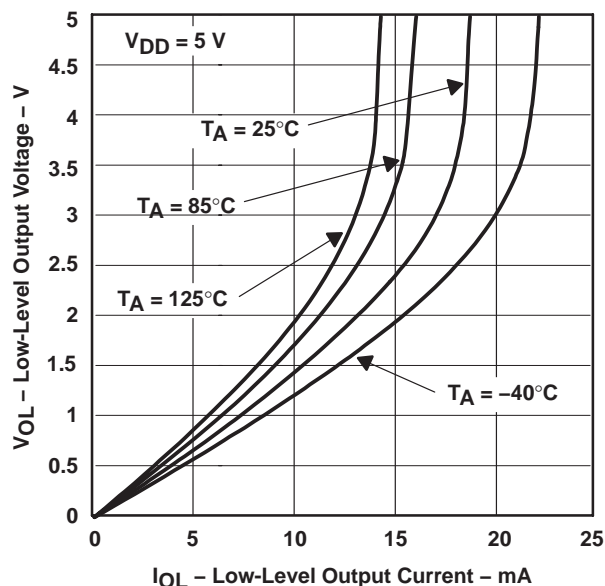


Figure 13

HIGH-LEVEL OUTPUT VOLTAGE
 vs
 HIGH-LEVEL OUTPUT CURRENT

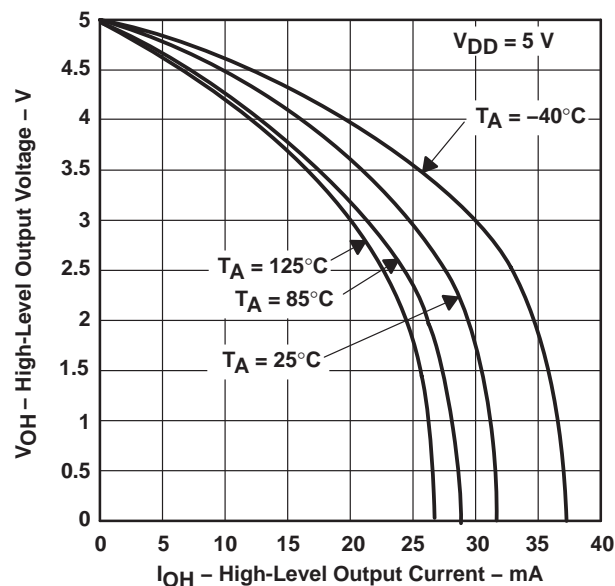


Figure 14

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

**OUTPUT IMPEDANCE
VS
FREQUENCY**

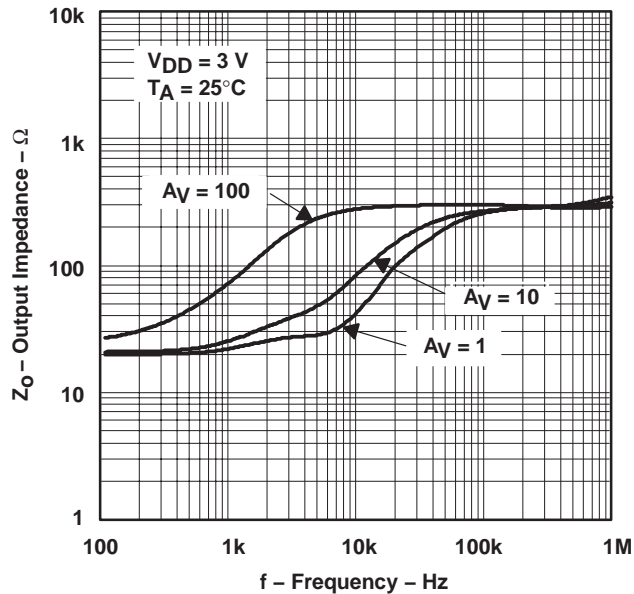


Figure 15

**OUTPUT IMPEDANCE
VS
FREQUENCY**

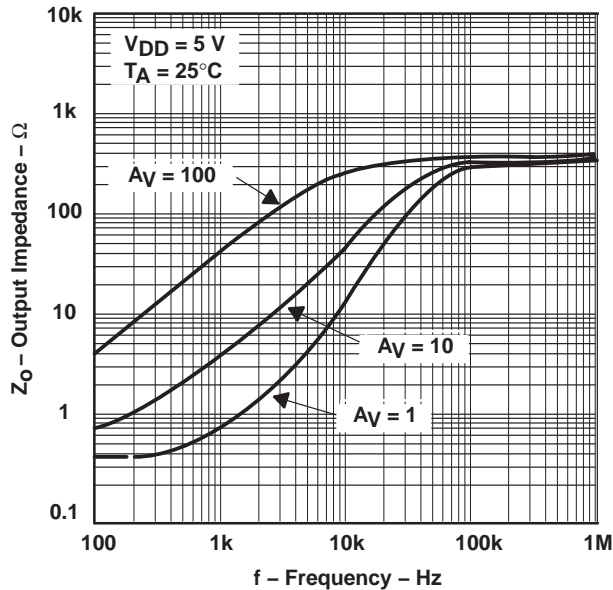


Figure 16

**COMMON-MODE REJECTION RATIO
VS
FREQUENCY**

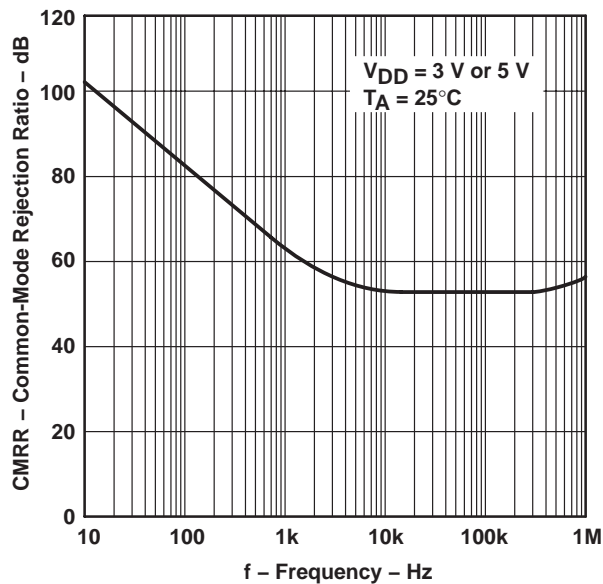


Figure 17



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

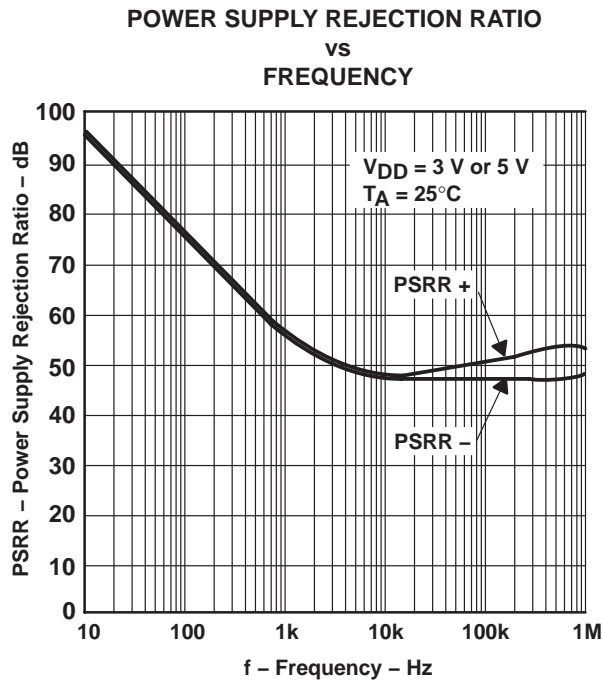


Figure 18

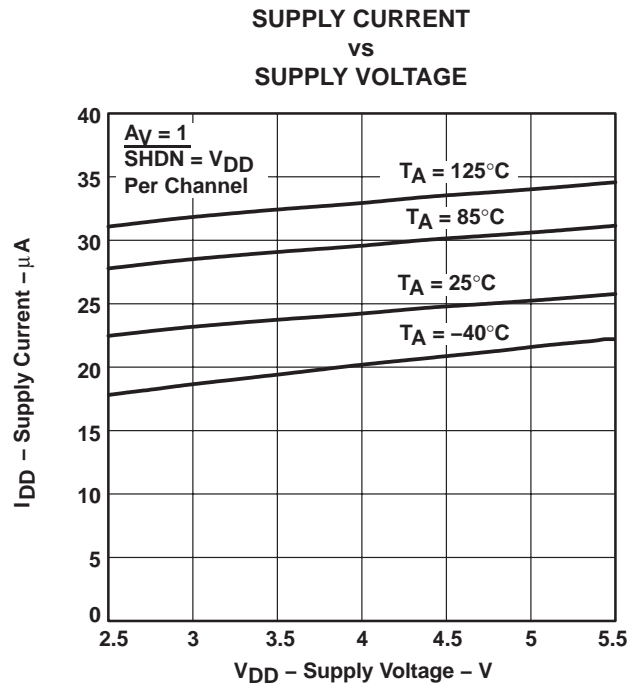


Figure 19

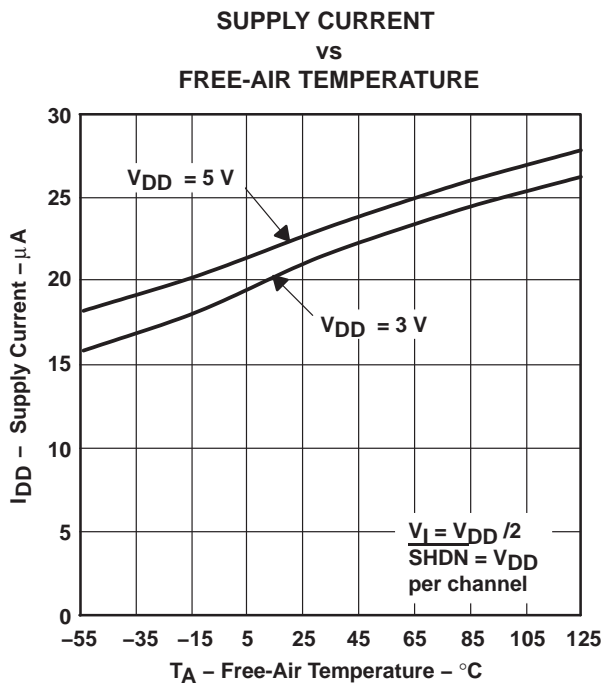


Figure 20

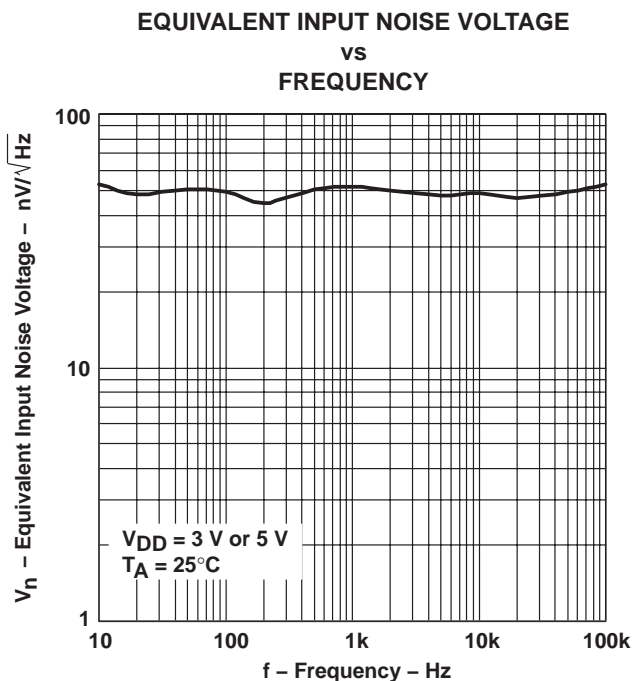


Figure 21



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA

FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION PLUS NOISE
VS
FREQUENCY**



Figure 22

**TOTAL HARMONIC DISTORTION PLUS NOISE
VS
FREQUENCY**



Figure 23

**PHASE MARGIN
VS
LOAD CAPACITANCE**



Figure 24

**GAIN-BANDWIDTH PRODUCT
VS
SUPPLY VOLTAGE**

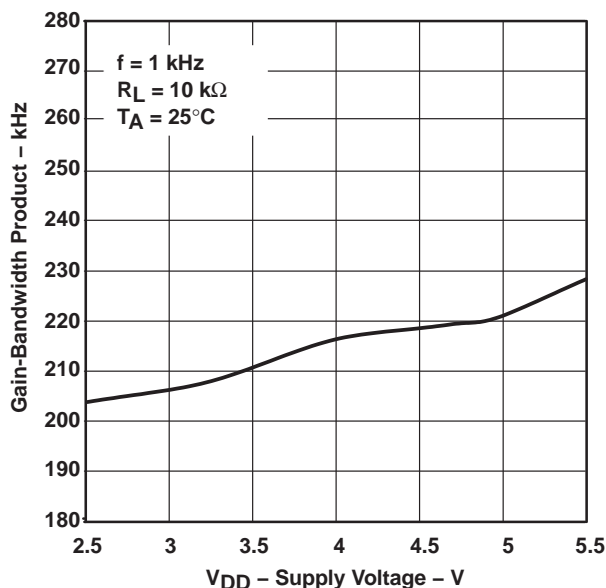


Figure 25

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS



Figure 26



Figure 27

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

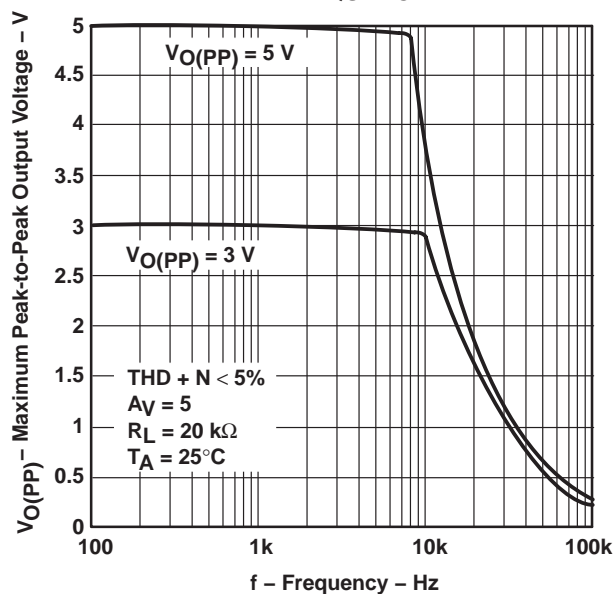


Figure 28



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

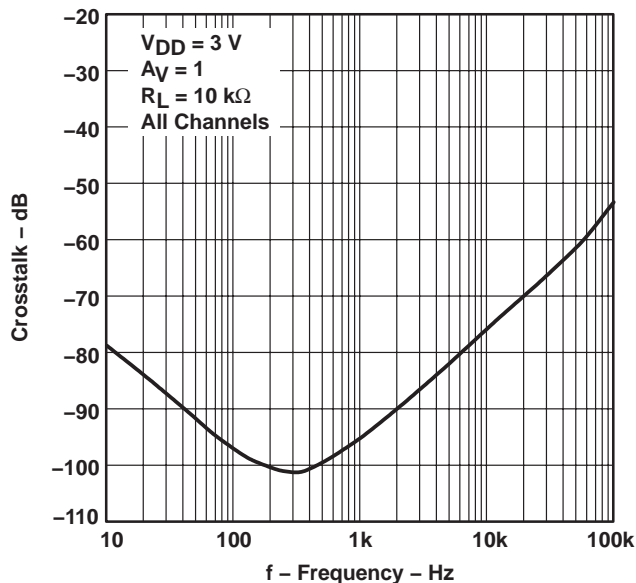


Figure 29

CROSSTALK
vs
FREQUENCY

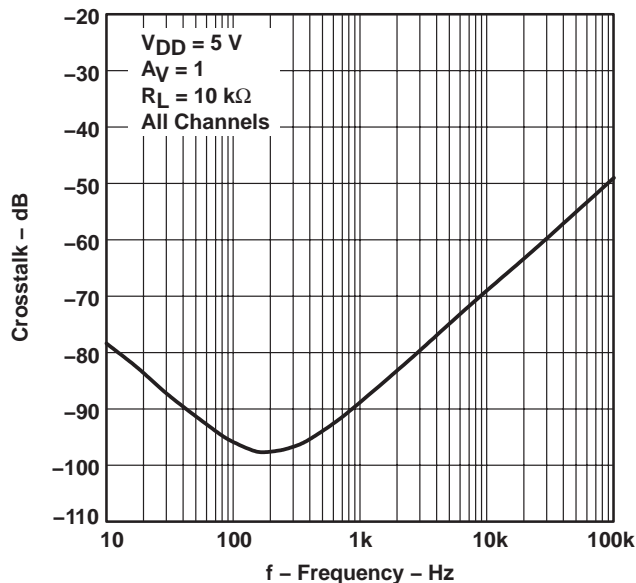


Figure 30

SMALL-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

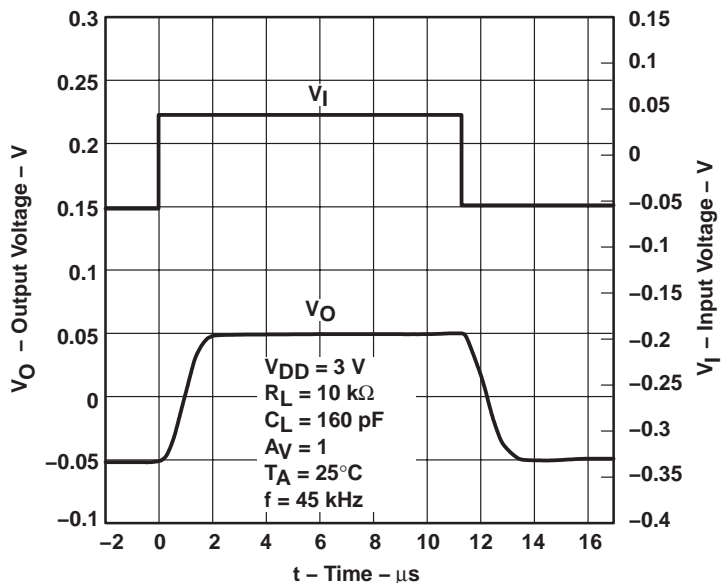


Figure 31



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE
 vs
 TIME



Figure 32

SMALL-SIGNAL FOLLOWER PULSE RESPONSE
 vs
 TIME



Figure 33

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

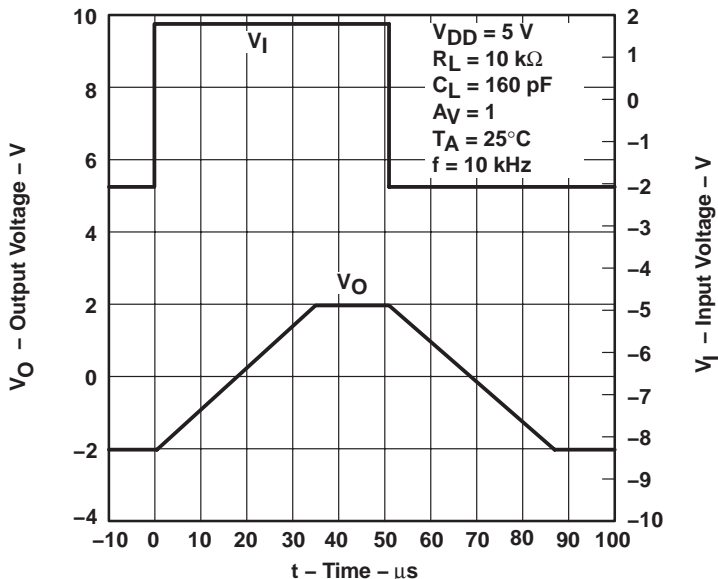


Figure 34

SHUTDOWN ON SUPPLY CURRENT
vs
TIME



Figure 35



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

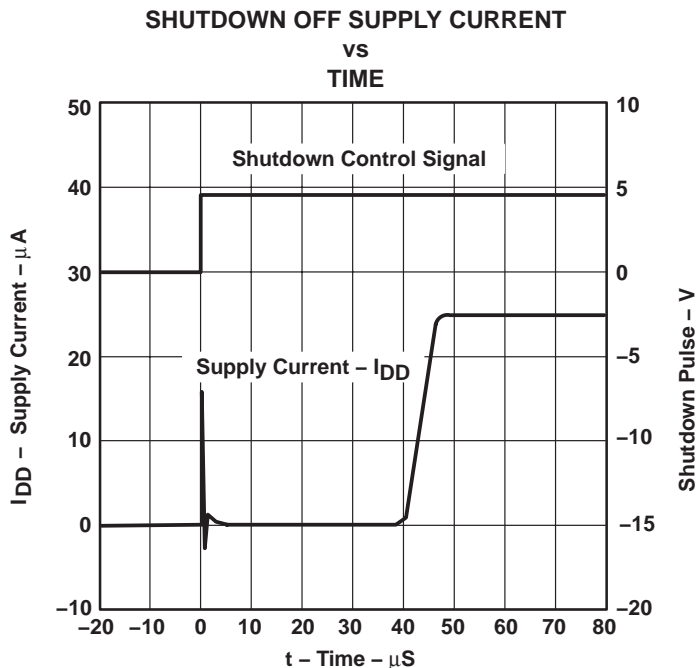


Figure 36



Figure 37

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME



Figure 38

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

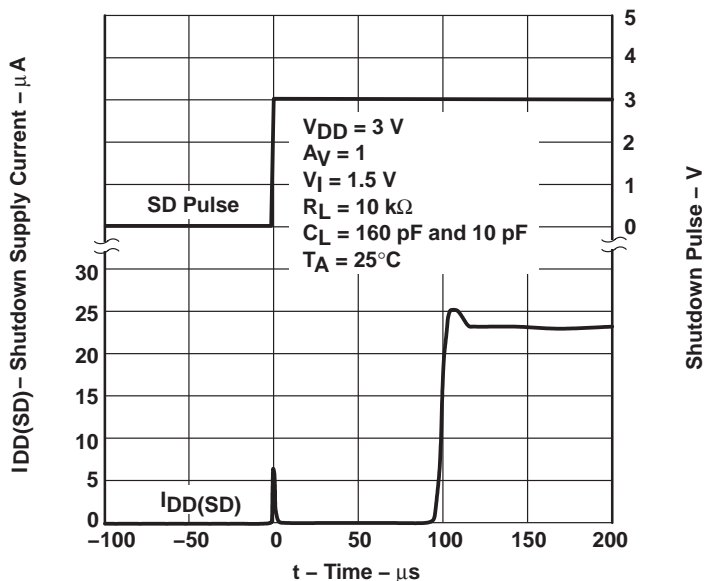


Figure 39

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
 vs
 TIME



Figure 40

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
 vs
 TIME

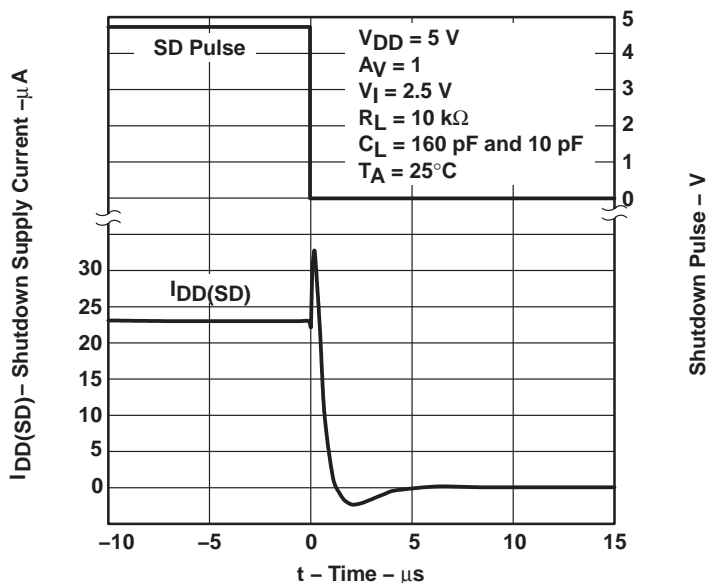


Figure 41

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

SHUTDOWN OFF PULSE RESPONSE
VS
TIME



Figure 42

SHUTDOWN OFF PULSE RESPONSE
VS
TIME

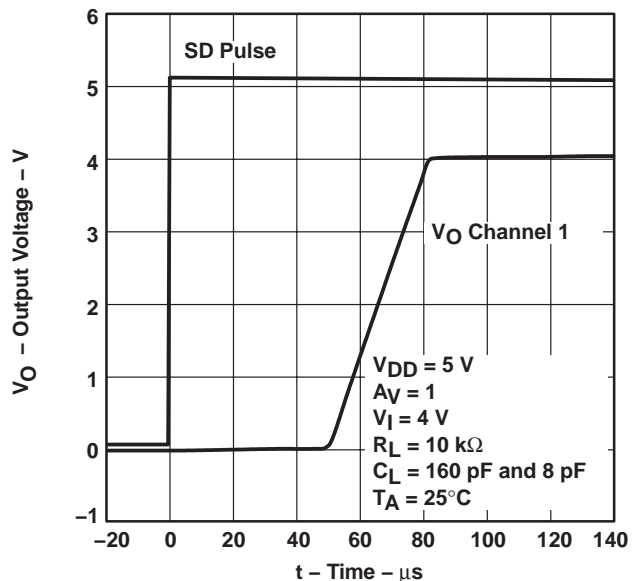


Figure 43

SHUTDOWN ON PULSE RESPONSE
VS
TIME

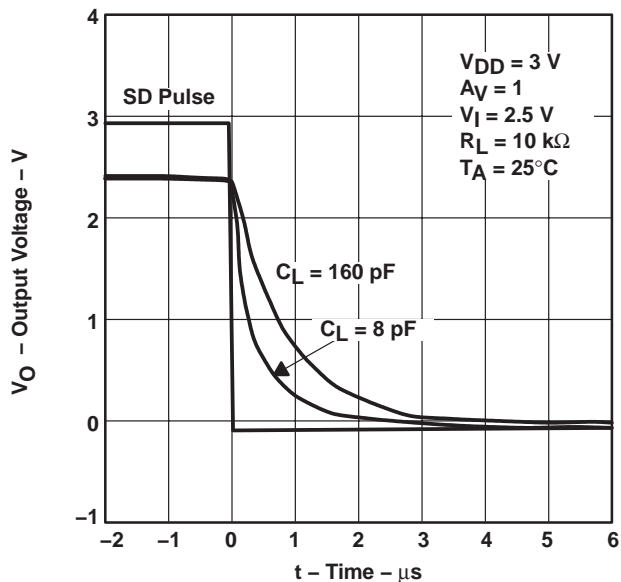


Figure 44

SHUTDOWN ON PULSE RESPONSE
VS
TIME



Figure 45



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
 FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

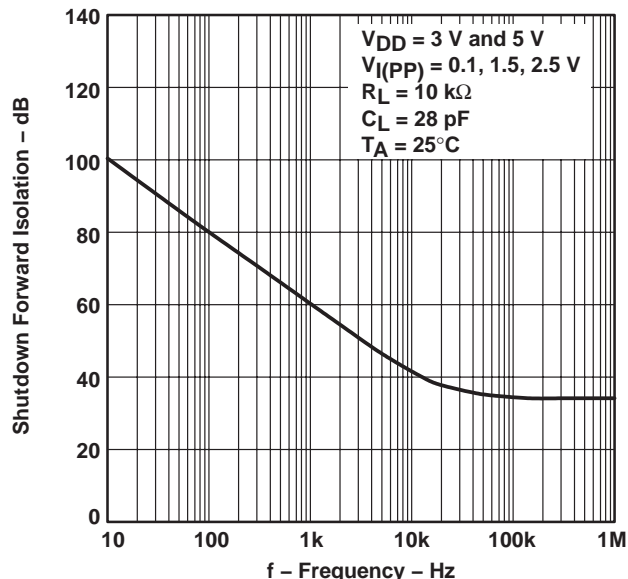
SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

TYPICAL CHARACTERISTICS

SHUTDOWN REVERSE ISOLATION
 VS
 FREQUENCY



SHUTDOWN FORWARD ISOLATION
 VS
 FREQUENCY



PARAMETER MEASUREMENT INFORMATION

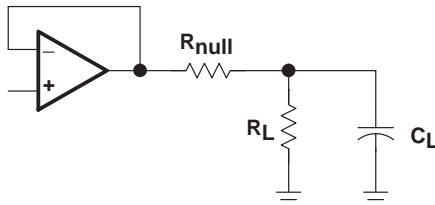


Figure 48

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

APPLICATION INFORMATION

shutdown function

Three members of the TLV245x family (TLV2450/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is pulled to the voltage level on the GND terminal of the device, the supply current is reduced to 16 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal must be pulled high. The shutdown terminal should never be left floating. The shutdown terminal threshold is always referenced to the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g. ± 2.5 V), the shutdown terminal needs to be pulled to V_{DD-} (not system ground) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 42, 43, 44, and 45. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 46 and 47 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ± 1.35 -V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1- V_{PP} , 1.5- V_{PP} , and 2.5- V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.5- V_{PP} input signal with a supply voltage of ± 1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

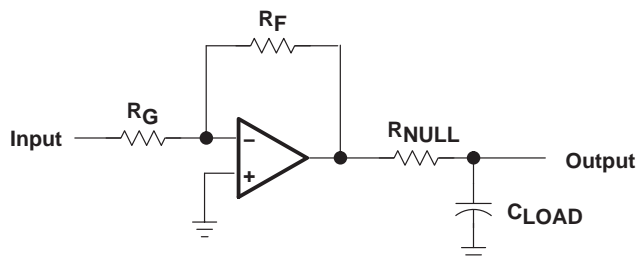


Figure 49. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

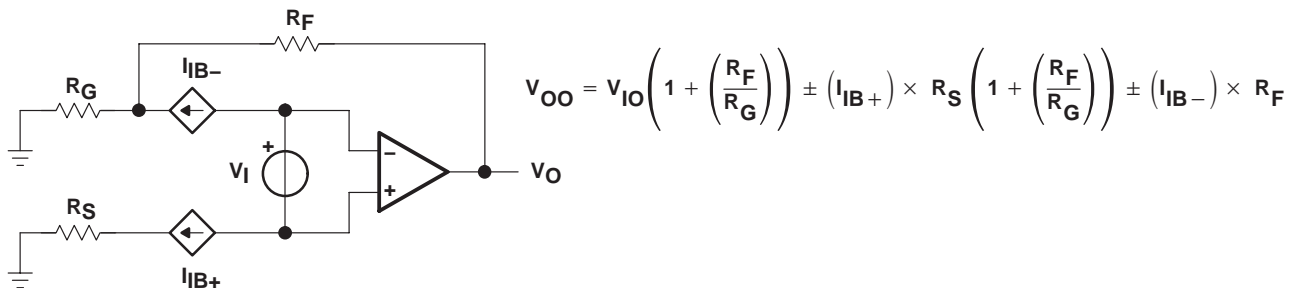


Figure 50. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

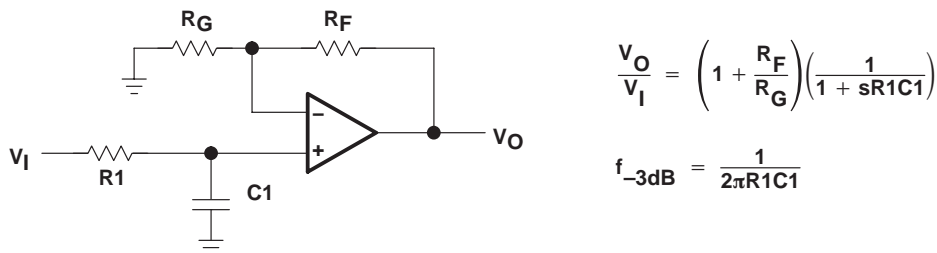


Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

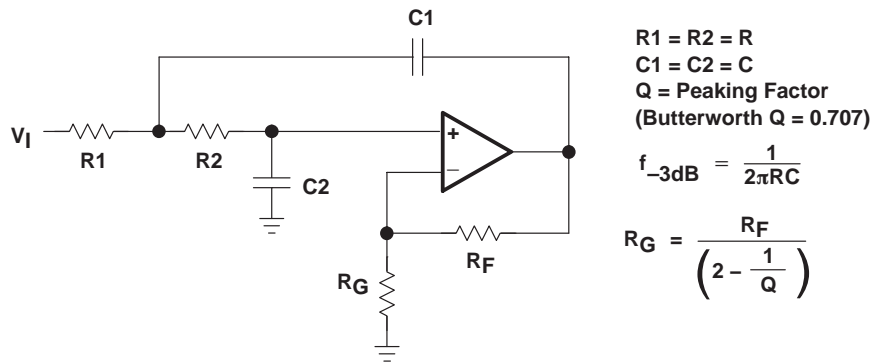


Figure 52. 2-Pole Low-Pass Sallen-Key Filter

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of TLV245x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- θ_{JA} = $\theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23- μ A 220-KHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*[™], the model generation software used with Microsim *PSpice*[™]. The Boyle macromodel (see Note 1) and subcircuit in Figure 54 are generated using the TLV245x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

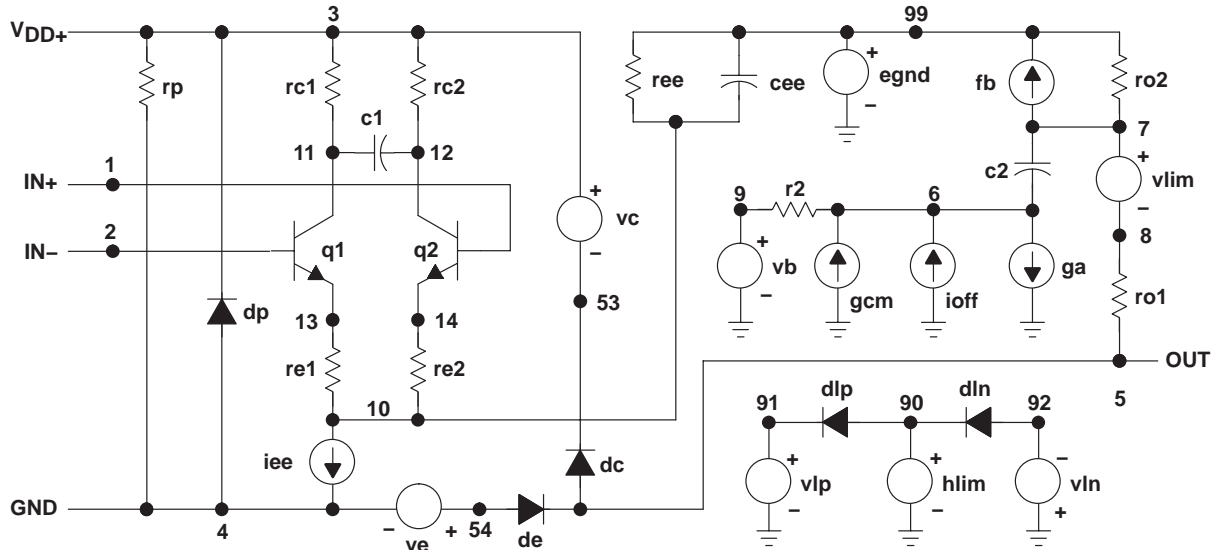
PSpice and *Parts* are trademarks of MicroSim Corporation.



TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23- μ A 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F – DECEMBER 1998 – REVISED JANUARY 2005

APPLICATION INFORMATION



* AMP_TLV2450-X operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 10/12/98 at 11:06
* Parts is a MicroSim product.

* connections: noninverting input
* | inverting input
* | positive power supply
* | negative power supply
* | output
*
* .subckt AMP_TLV2450-X 1 2 3 4 5

C1	11	12	354.48E-15
C2	6	7	7.5000E-12
CEE	10	99	42.237E-15
DC	5	53	dy
DE	54	5	dy
DLP	90	91	dx
DLN	92	90	dx
DP	4	3	dx
EGND	99	0	poly(2) (3,0) (4,0) 0 .5 .5
FB	7	99	poly(5) vb vc ve vlp vln 0
+ 207.31E6 -1E3 1E3 210E6 -210E6			
GA	6	0	11 12 15.254E-6
GCM	0	6	10 99 48.237E-12

IEE	10	4	dc	938.61E-9
HLIM	90	0	vlim	1K
Q1	11	2	13	qx1
Q2	12	1	14	qx2
R2	6	9	100.00E3	
RC1	3	11	65.557E3	
RC2	3	12	65.557E3	
RE1	13	10	10.367E3	
RE2	14	10	10.367E3	
REE	10	99	213.08E6	
RO1	8	5	10	
RO2	7	99	10	
RP	3	4	147.06	
VB	9	0	dc	0
VC	3	53	dc	.82
VE	54	4	dc	.82
VLIM	7	8	dc	0
VLP	91	0	dc	38
VLN	0	92	dc	38
.model dx D(Is=800.00E-18)				
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)				
.model qx1 NPN(Is=800.00E-18 Bf=843.08)				
.model qx2 NPN(Is=800.0000E-18 Bf=843.08)				
.ends				

Figure 54. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2450AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450AI	Samples
TLV2450AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2450AI	Samples
TLV2450CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2450C	Samples
TLV2450CDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAQC	Samples
TLV2450CDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAQC	Samples
TLV2450CDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAQC	Samples
TLV2450CDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAQC	Samples
TLV2450CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2450C	Samples
TLV2450CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2450C	Samples
TLV2450ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450I	Samples
TLV2450IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAQI	Samples
TLV2450IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAQI	Samples
TLV2450IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAQI	Samples
TLV2450IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAQI	Samples
TLV2451AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451AI	Samples
TLV2451AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451AI	Samples
TLV2451AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2451AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2451CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2451C	Samples
TLV2451CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VARC	Samples
TLV2451CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VARC	Samples
TLV2451CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VARC	Samples
TLV2451CDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VARC	Samples
TLV2451CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2451C	Samples
TLV2451CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2451C	Samples
TLV2451CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2451C	Samples
TLV2451CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2451C	Samples
TLV2451CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2451C	Samples
TLV2451ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451I	Samples
TLV2451IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VARI	Samples
TLV2451IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VARI	Samples
TLV2451IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VARI	Samples
TLV2451IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VARI	Samples
TLV2451IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451I	Samples
TLV2451IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451I	Samples
TLV2451IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2451I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2452AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452AI	Samples
TLV2452AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452AI	Samples
TLV2452AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452AI	Samples
TLV2452AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452AI	Samples
TLV2452AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2452AI	Samples
TLV2452CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2452C	Samples
TLV2452CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2452C	Samples
TLV2452CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ABI	Samples
TLV2452CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ABI	Samples
TLV2452CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ABI	Samples
TLV2452CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2452C	Samples
TLV2452CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2452C	Samples
TLV2452ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452I	Samples
TLV2452IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452I	Samples
TLV2452IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ABJ	Samples
TLV2452IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ABJ	Samples
TLV2452IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ABJ	Samples
TLV2452IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ABJ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2452IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452I	Samples
TLV2452IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2452IP	Samples
TLV2452IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2452IP	Samples
TLV2453CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2453C	Samples
TLV2453CDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ABK	Samples
TLV2453CDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ABK	Samples
TLV2453CDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ABK	Samples
TLV2453CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2453C	Samples
TLV2453IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABL	Samples
TLV2453IDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABL	Samples
TLV2453IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABL	Samples
TLV2453IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2453IN	Samples
TLV2454AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454AI	Samples
TLV2454AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454AI	Samples
TLV2454AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2454AI	Samples
TLV2454AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TY2454A	Samples
TLV2454AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TY2454A	Samples
TLV2454AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2454AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454A	Samples
TLV2454CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2454C	Samples
TLV2454CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2454C	Samples
TLV2454CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2454	Samples
TLV2454CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2454	Samples
TLV2454CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2454	Samples
TLV2454ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454I	Samples
TLV2454IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454I	Samples
TLV2454IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454I	Samples
TLV2454IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454I	Samples
TLV2454IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2454I	Samples
TLV2454IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454	Samples
TLV2454IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454	Samples
TLV2454IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454	Samples
TLV2455AID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455AI	Samples
TLV2455AIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455AI	Samples
TLV2455AIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2455AI	Samples
TLV2455AIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2455A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2455AIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2455A	Samples
TLV2455CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2455C	Samples
TLV2455CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2455C	Samples
TLV2455ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455I	Samples
TLV2455IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455I	Samples
TLV2455IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455I	Samples
TLV2455IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2455	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



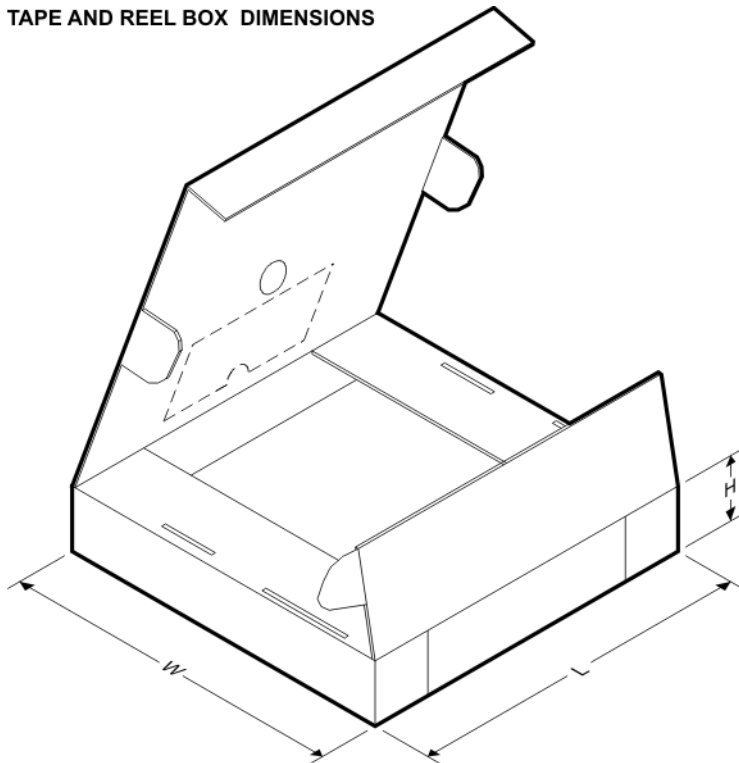
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2450AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2450CDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2450CDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2450IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2450IDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2451CDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451CDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2451CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2451IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2452CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2453CDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2453CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2453IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2454AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2454AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2454CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2454IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2454IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2455AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2455AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2455IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

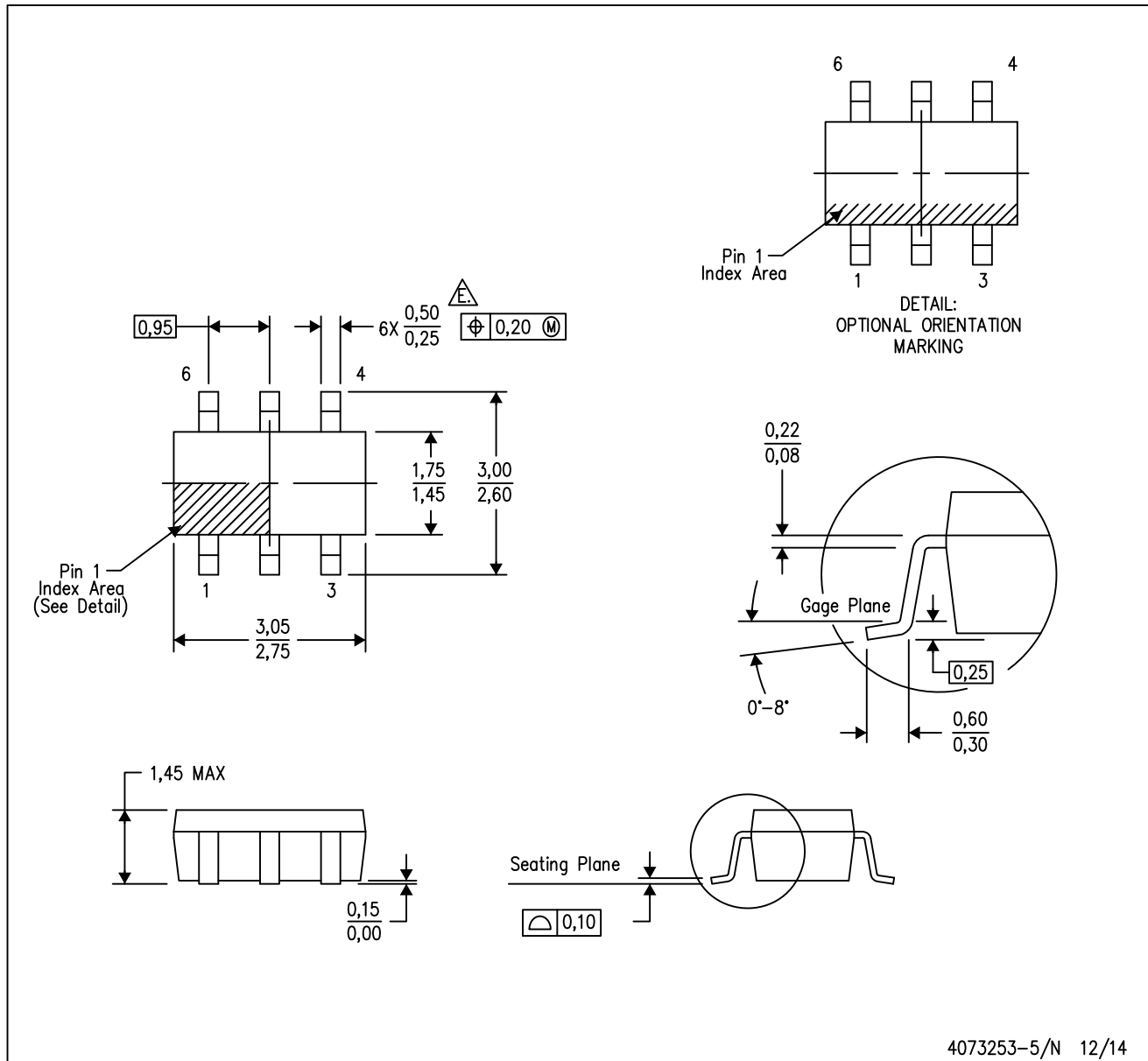
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2450AIDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2450CDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2450CDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2450IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2450IDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2451AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2451CDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2451CDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2451CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2451CDR	SOIC	D	8	2500	367.0	367.0	38.0
TLV2451IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2451IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2451IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2452AIDR	SOIC	D	8	2500	367.0	367.0	38.0
TLV2452AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2452CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2452CDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2452CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2452CDR	SOIC	D	8	2500	367.0	367.0	38.0
TLV2452IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2452IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2452IDR	SOIC	D	8	2500	367.0	367.0	38.0
TLV2452IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2453CDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2453CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2453IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2454AIDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2454AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2454CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2454IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2454IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2455AIDR	SOIC	D	16	2500	367.0	367.0	38.0
TLV2455AIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TLV2455IDR	SOIC	D	16	2500	367.0	367.0	38.0

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

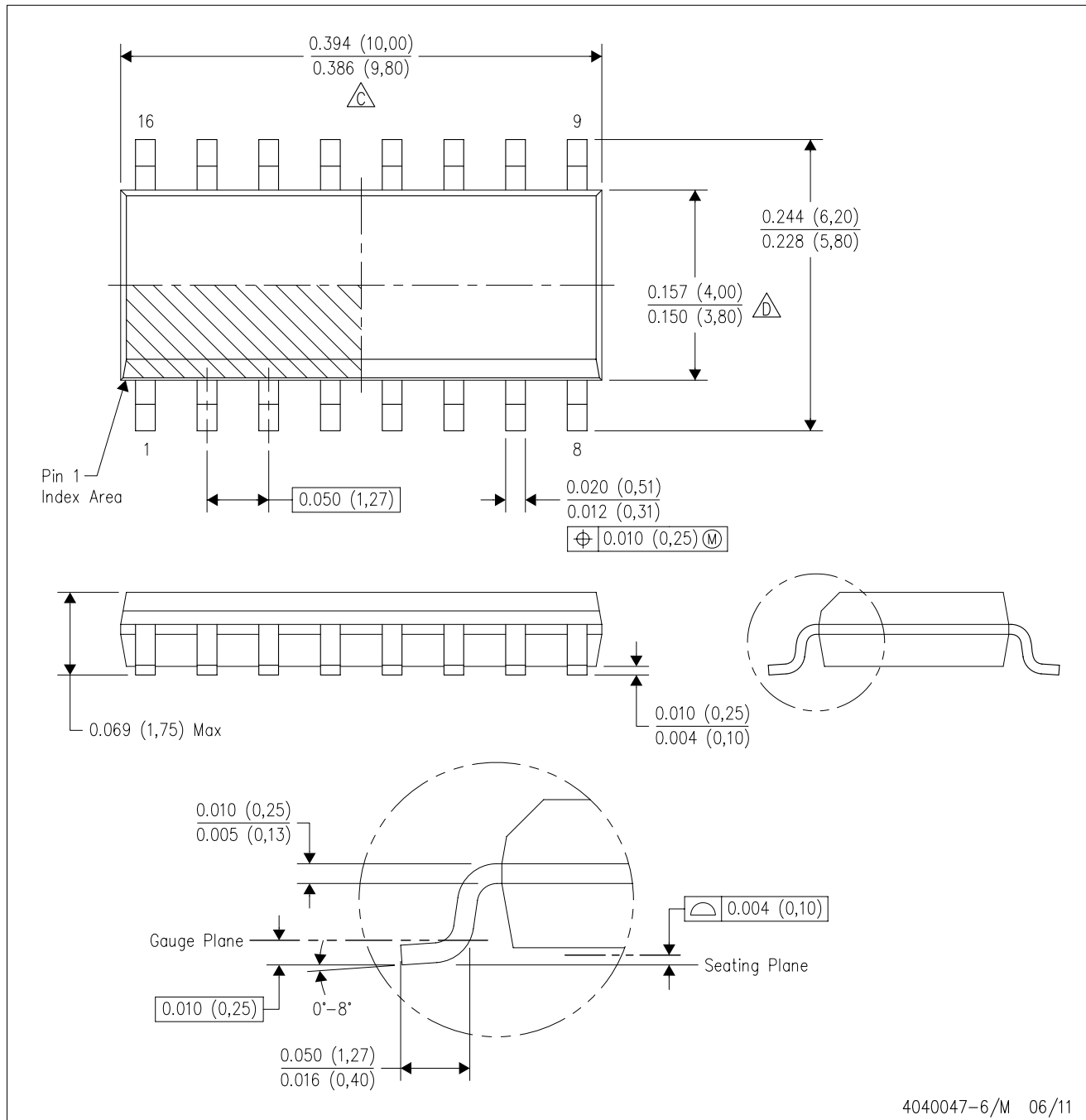
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



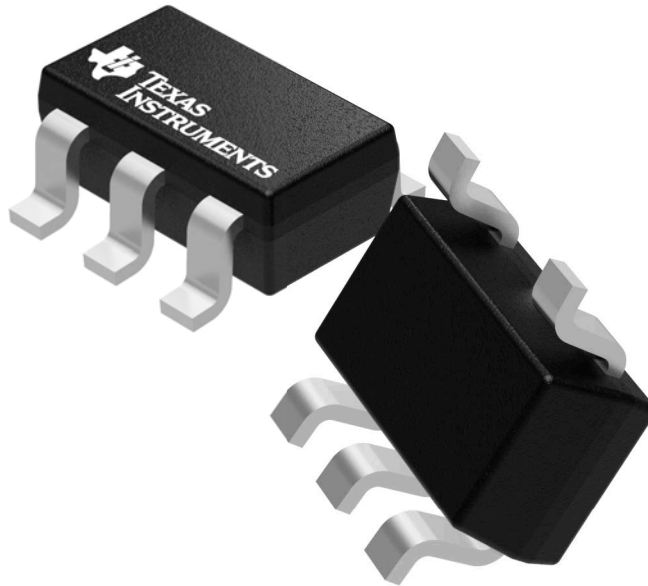
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

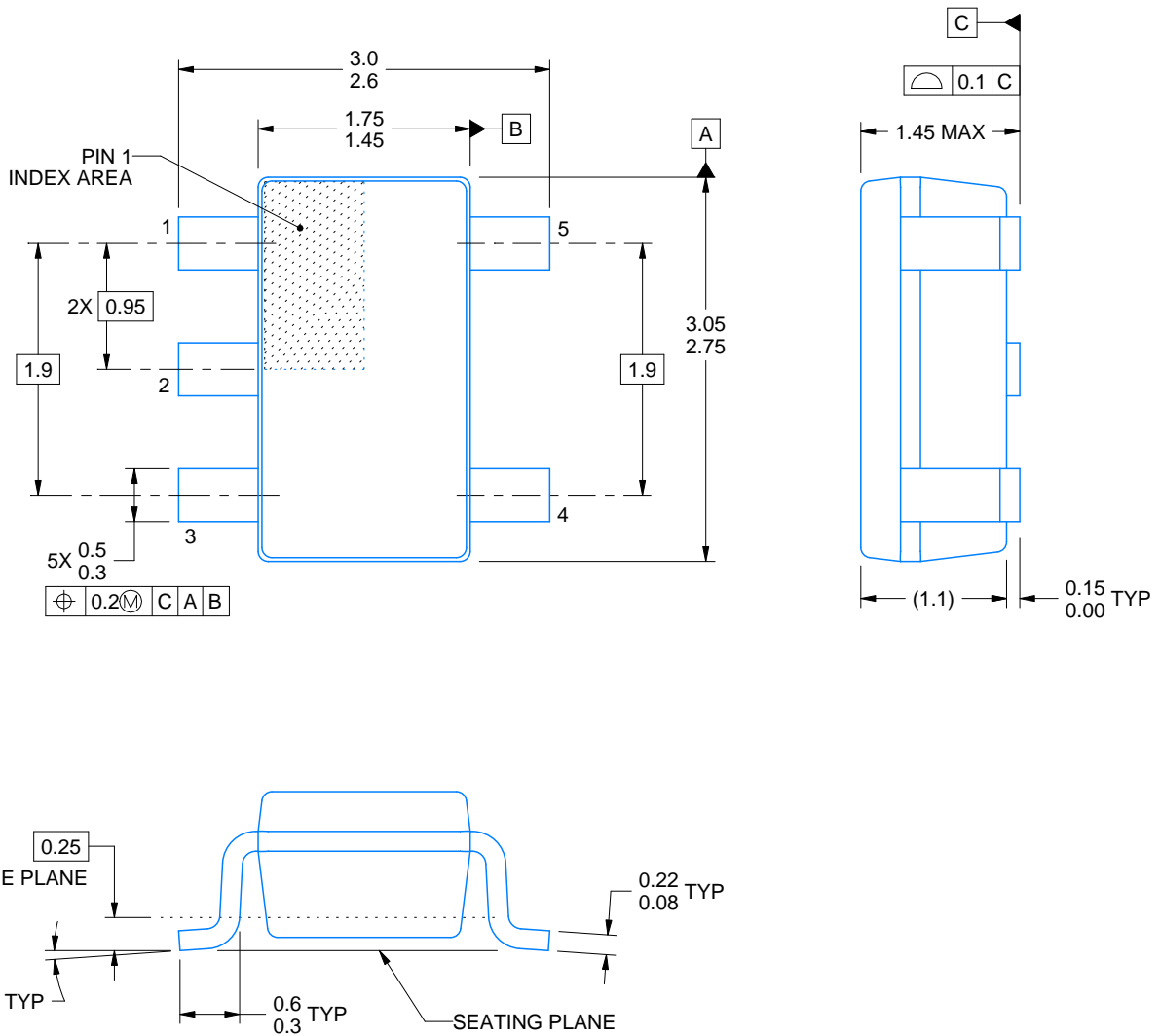
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

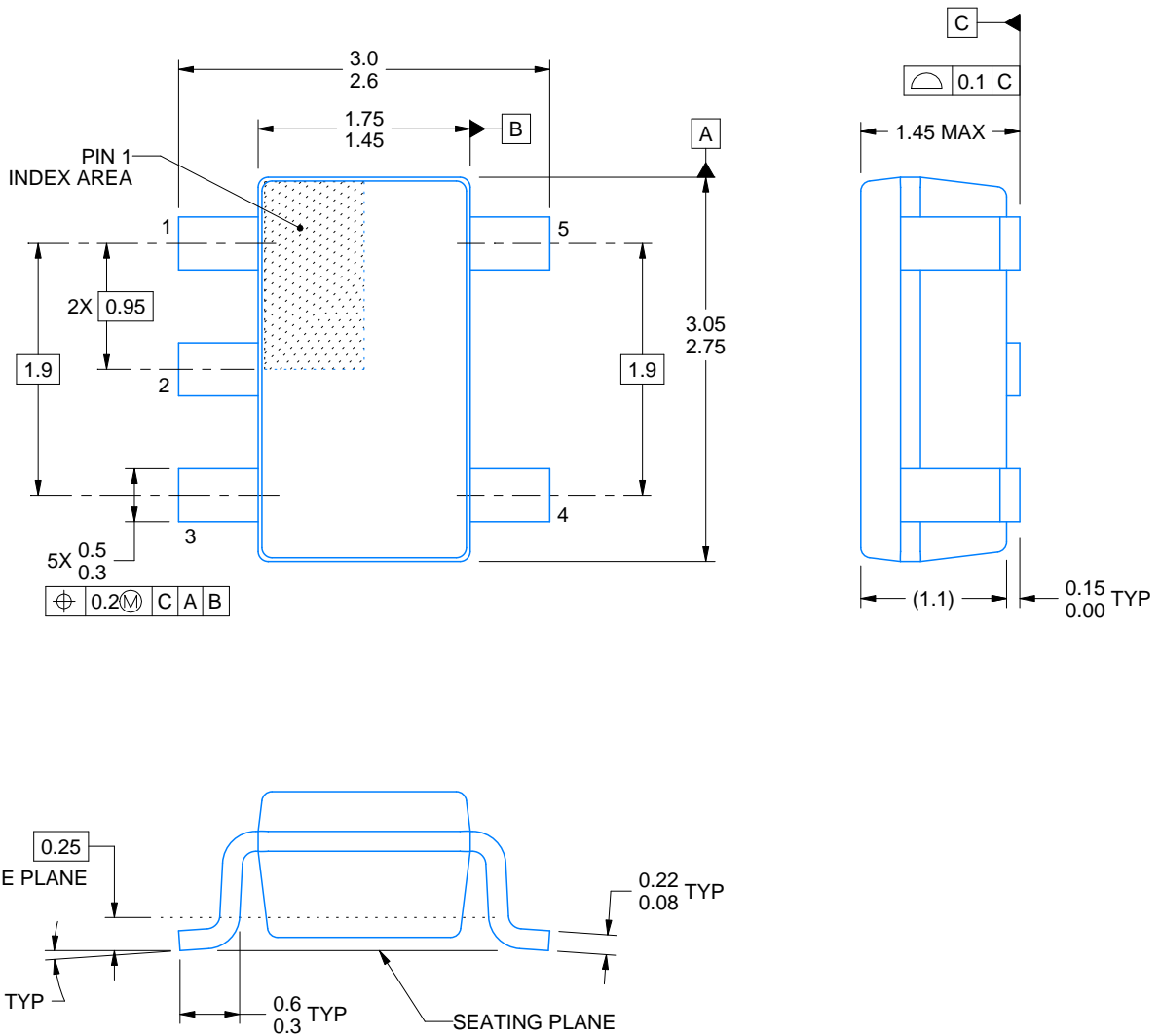
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



4073272/C 02/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.