TS3A44159 0.45-Ω Quad SPDT Analog Switch 4-Channel 2:1 Multiplexer – Demultiplexer With Two Controls

1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance (<0.5 Ω)
- Control Inputs Are 1.8-V Logic Compatible
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 4.3-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - ±2000-V Human-Body Model (A114-B, Class II)
  - ±1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Pins and Peripherals

3 Description

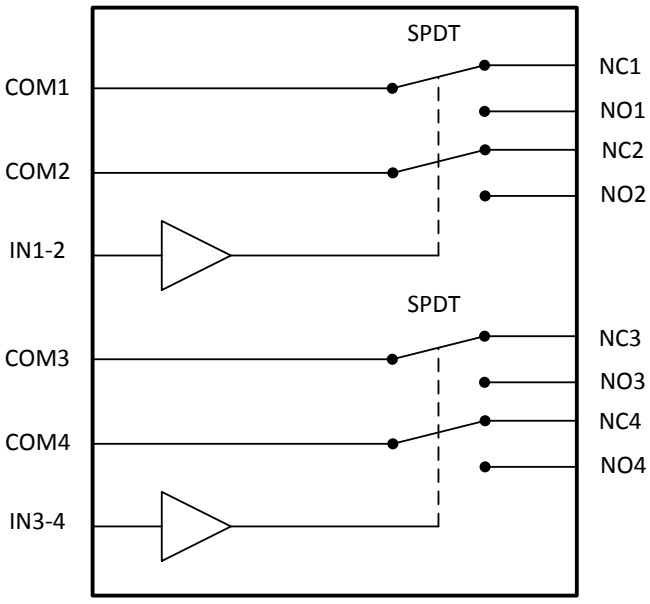
The TS3A44159 is a bidirectional 4-channel single-pole double-throw (SPDT) analog switch with two control inputs, which is designed to operate from 1.65 V to 4.3 V. This device is also known as a 2 channel double-pole double-throw (DPDT) configuration. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature that prevents signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A44159	TSSOP (16)	5.00 mm × 4.40 mm
	VQFN (16)	3.00 mm × 3.00 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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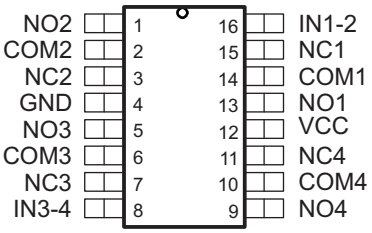
4 Revision History

Changes from Revision B (October 2012) to Revision C **Page**

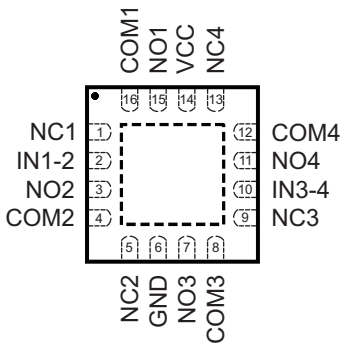
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

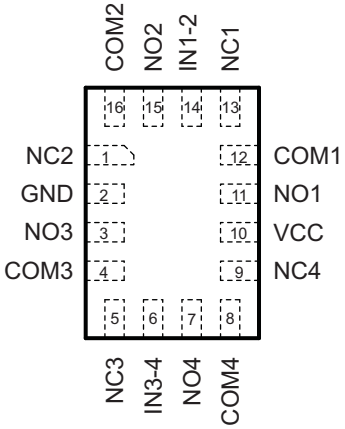
PW PACKAGE
(TOP VIEW)



RGT PACKAGE
(TOP VIEW)



RSV PACKAGE
(TOP VIEW)



Pin Functions

PIN				I/O	DESCRIPTION
PW NO.	RGT NO.	RSV NO.	NAME		
1	3	15	NO2	I/O	Normally Open
2	4	16	COM2	I/O	Common
3	5	1	NC2	I/O	Normally Closed
4	6	2	GND	—	Ground
5	7	3	NO3	I/O	Normally Open
6	8	4	COM3	I/O	Common
7	9	5	NC3	I/O	Normally Closed
8	10	6	IN3-4	I	Digital Control to connect COM to NO or NC
9	11	7	NO4	I/O	Normally Open
10	12	8	COM4	I/O	Common
11	13	9	NC4	I/O	Normally Closed
12	14	10	VCC	I	Power Supply
13	15	11	NO1	I/O	Normally Open
14	16	12	COM1	I/O	Common
15	1	13	NC1	I/O	Normally Closed
16	2	14	IN1-2	I/O	Digital Control to connect COM to NO or NC

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage(3) (4) (5)		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–200	200	mA
	ON-state peak switch current(6)		–400	400	
V_{IN}	Digital input voltage		–0.5	4.6	V
I_{IK}	Digital input clamp current(3) (4)	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 4.6 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	0	4.3	V
V_{NC} V_{NO} V_{COM}	Analog Voltage	0	4.3	V
V_{IN}	Digital Input Voltage	0	4.3	V

6.4 Thermal Information

THERMAL METRIC[1]		TS3A44159			UNIT
		PW	RGT	RSV	
		16 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.0	45.4	107.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.0	58.1	41.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	53.1	18.6	43.6	
ψ_{JT}	Junction-to-top characterization parameter	4.6	1.1	1.1	
ψ_{JB}	Junction-to-board characterization parameter	52.5	18.6	43.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	3.9	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.5	0.7	Ω
				Full				0.8	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.5 V, 0.6 V I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.05	0.07	Ω
				Full				0.1	
$R_{on(flat)}$	ON-state resistance flatness	V_{NO} or V_{NC} = 1.5 V, 0.6 V 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.5	0.7	Ω
				Full				0.8	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = 0.3 V,	See Figure 17	25°C	1.95 V	–10	0.5	10	nA
				Full		–20		20	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = Open,	See Figure 18	25°C	1.95 V	–10	0.1	10	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NO} or V_{NC} = Open, V_{COM} = 0.3V, or V_{NO} or V_{NC} = Open, V_{COM} = 1.65 V,	See Figure 18	25°C	1.95 V	–10	0.1	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN1-2, IN3-4)[2]									
V_{IH}	Input logic high			Full		1		4.3	V
V_{IL}	Input logic low			Full		0		0.4	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 3.6 V or 0		25°C	1.95 V		0.5	10	nA
				Full				50	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	1.8 V		40	70	ns
				Full	1.65 V to 1.95 V			75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	1.8 V		22	45	ns
				Full	1.65 V to 1.95 V			50	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	1.8 V	5	25	70	ns
				Full	1.65 V to 1.95 V	4		75	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF	25°C	1.8 V		64		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	1.8 V		52		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	1.8 V		164		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 19	25°C	1.8 V		164		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND		25°C	1.8 V		2.5		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON	25°C	1.8 V		35		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 100 kHz,	Switch OFF	25°C	1.8 V		–71		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 100 kHz,	Switch ON	25°C	1.8 V		–73		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, V_{COM} = GND to V_{CC}	f = 20 Hz to 20 kHz	25°C	1.8 V		0.1%		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.05	μA
				Full				0.15	

6.6 Electrical Characteristics for 2.1-V Supply

V_{CC} = 2.00 V to 2.20 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
DIGITAL CONTROL INPUTS (IN1-2, IN3-4)								
V_{IH}	Input logic high		Full		1.2		4.3	V
V_{IL}	Input logic low		Full		0		0.5	V

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.7 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.45	0.6	Ω
				Full				0.7	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.045	0.07	Ω
				Full				0.1	
$R_{on(flat)}$	ON-state resistance flatness	V_{NO} or V_{NC} = 1.8 V, 0.8 V I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.06	0.15	Ω
				Full				0.2	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 2.3 V, or V_{NO} or V_{NC} = 2.3 V, V_{COM} = 0.3V,	See Figure 17	25°C	2.7 V	–10	0.5	10	nA
				Full		–20		20	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 2.3 V, V_{COM} = Open,	See Figure 18	25°C	2.7 V	–10	0.1	10	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 2.3 V,	See Figure 18	25°C	2.7 V	–10	0.1	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN1-2, IN3-4)(2)									
V_{IH}	Input logic high			Full		1.2		4.3	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 3.6 V or 0		25°C	2.7 V		0.5	10	nA
				Full				50	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	2.5 V		2.6	47	ns
				Full	2.3 V to 2.7 V			50	
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	2.5 V		16.5	34	ns
				Full	2.3 V to 2.7 V			35	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	2.5 V	4	15	35	ns
				Full	2.3 V to 2.7 V	3		35	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF	25°C	2.5 V		84		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	2.5 V		52		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	2.5 V		163		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND,	See Figure 19	25°C	2.5 V		163		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance	V_I = V_{CC} or GND		25°C	2.5 V		2.5		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON	25°C	2.5 V		35		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 100 kHz,	Switch OFF	25°C	2.5 V		–71		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 100 kHz,	Switch ON	25°C	2.5 V		–73		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, V_{COM} = GND to V_{CC}	f = 20 Hz to 20 kHz	25°C	2.5 V		0.009%		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	2.5 V		0.004	0.1	μA
				Full				0.5	

6.8 Electrical Characteristics for 3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.0 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	3 V		0.37	0.55	Ω
				Full				0.6	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.0 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	3 V		0.06	0.07	Ω
				Full				0.1	
$R_{on(flat)}$	ON-state resistance flatness	V_{NO} or V_{NC} = 2.0 V, 0.8 V I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	3 V		0.05	0.1	Ω
				Full				0.1	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 3.0 V, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = 0.3 V,	See Figure 17	25°C	3.6 V	–15	5	15	nA
				Full		–50		50	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = Open,	See Figure 18	25°C	3.6 V	–15	5	15	nA
				Full		–50		50	
$I_{COM(ON)}$	COM ON leakage current	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 3.0 V,	See Figure 18	25°C	3.6 V	–15	5	15	nA
				Full		–50		50	
DIGITAL CONTROL INPUTS (IN1-2, IN3-4)(2)									
V_{IH}	Input logic high			Full		1.25		4.3	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 3.6 V or 0		25°C	3.6 V		0.5	10	nA
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	3 V		20	38	ns
				Full	3 V to 3.6 V			40	
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	3 V		14	34	ns
				Full	3 V to 3.6 V			35	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	3 V	3	11	35	ns
				Full	3 V to 3.6 V	2		55	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF	25°C	3 V		109		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	3 V		51		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	3 V		162		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 19	25°C	3 V		162		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND		25°C	3 V		2.5		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON	25°C	3 V		35		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 100 kHz,	Switch OFF	25°C	3 V		–71		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 100 kHz,	Switch ON	25°C	3 V		–73		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, V_{COM} = GND to V_{CC}	f = 20 Hz to 20 kHz	25°C	3 V		0.003%		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	3.6 V		0.015	0.2	μA
				Full				0.7	

6.9 Electrical Characteristics for 4.3-V Supply

T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	4.3 V		0.3	0.45	Ω
				Full				0.5	
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	4.3 V		0.05	0.07	Ω
				Full				0.1	
$R_{on(flat)}$	ON-state resistance flatness	V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	4.3 V		0.02	0.1	Ω
				Full				0.1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 4.3-V Supply (continued)

T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NC, NO OFF leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 3.0 V, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = 0.3 V,	See Figure 17	25°C	4.3 V	–20	5	20	nA
				Full		–90		90	
$I_{NO(ON)}$, $I_{NC(ON)}$	NC, NO ON leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = Open,	See Figure 18	25°C	4.3 V	–20	5	20	nA
				Full		–90		90	
$I_{COM(ON)}$	COM ON leakage current	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 3.0 V,	See Figure 18	25°C	4.3 V	–20	5	20	nA
				Full		–90		90	
DIGITAL CONTROL INPUTS (IN1-2, IN3-4)(2)									
V_{IH}	Input logic high			Full	4.3 V	1.5		4.3	V
V_{IL}	Input logic low			Full	4.3 V	0		1	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 3.6 V or 0		25°C	4.3 V		0.5	10	nA
				Full				50	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	4.3 V		17	23	ns
				Full				25	
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	4.3 V		12	32	ns
				Full				35	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF	25°C	4.3 V	2	9	30	ns
				Full		1		35	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF	25°C	4.3 V		139		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO off capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	4.3 V		50		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 19	25°C	4.3 V		160		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 19	25°C	4.3 V		160		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND		25°C	4.3 V		2.5		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON	25°C	4.3 V		35		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 100 kHz,	Switch OFF	25°C	4.3 V		–71		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 100 kHz,	Switch ON	25°C	4.3 V		–73		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, V_{COM} = GND to V_{CC}	f = 20 Hz to 20 kHz	25°C	4.3 V		0.003%		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	4.3 V		0.15	0.4	μA
				Full				1.2	

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.10 Typical Characteristics

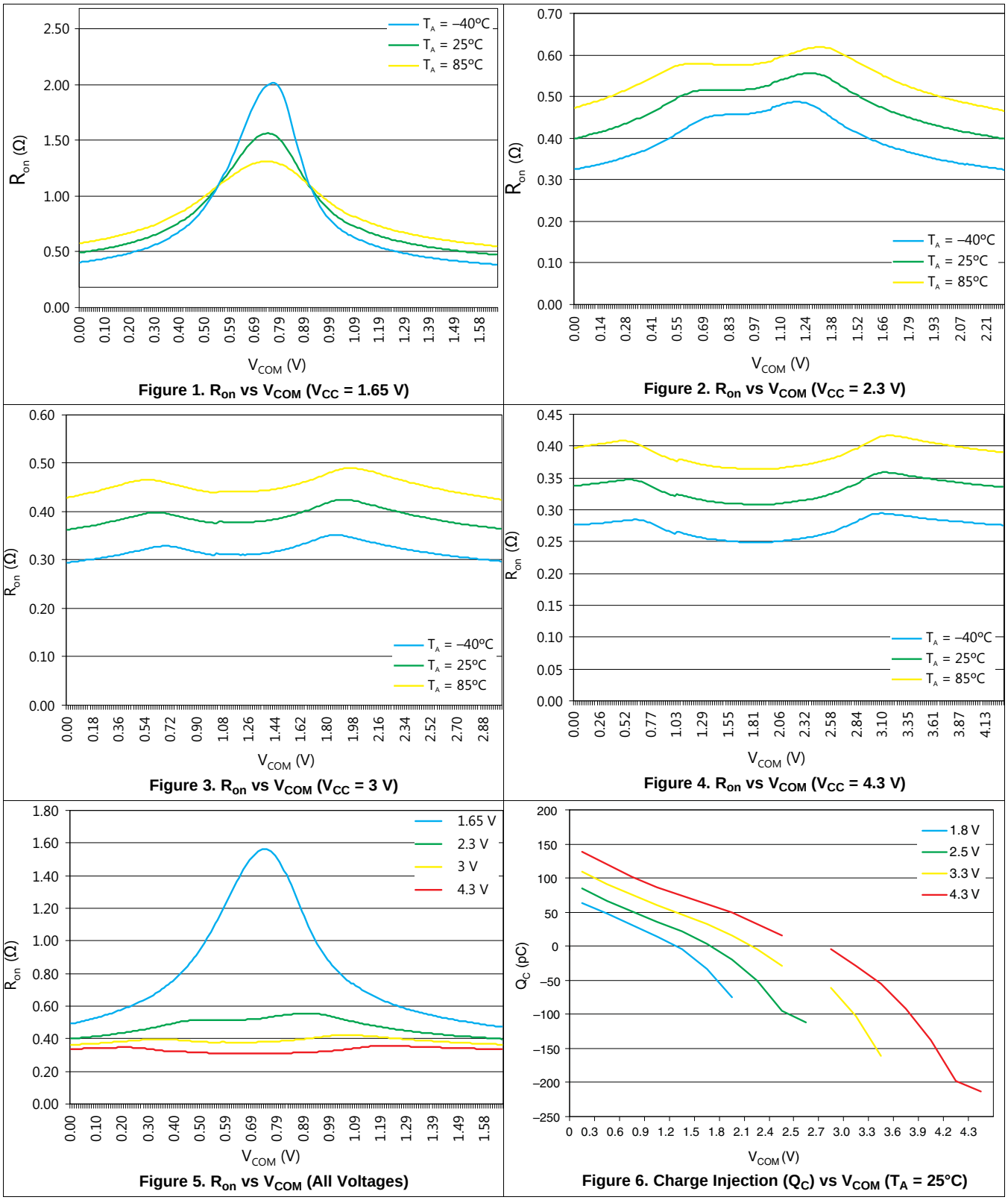


Figure 1. R_{on} vs V_{COM} (V_{CC} = 1.65 V)

Figure 2. R_{on} vs V_{COM} (V_{CC} = 2.3 V)

Figure 3. R_{on} vs V_{COM} (V_{CC} = 3 V)

Figure 4. R_{on} vs V_{COM} (V_{CC} = 4.3 V)

Figure 5. R_{on} vs V_{COM} (All Voltages)

Figure 6. Charge Injection (Q_C) vs V_{COM} (T_A = 25°C)

Typical Characteristics (continued)

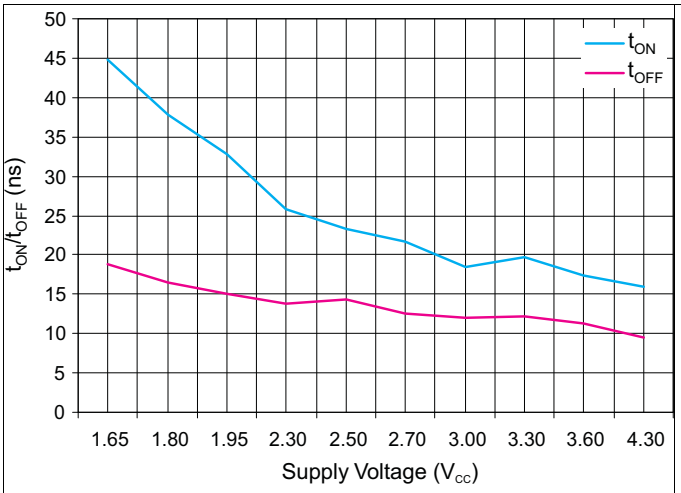


Figure 7. t_{ON} and t_{OFF} vs Supply Voltage (T_A = 25°C)

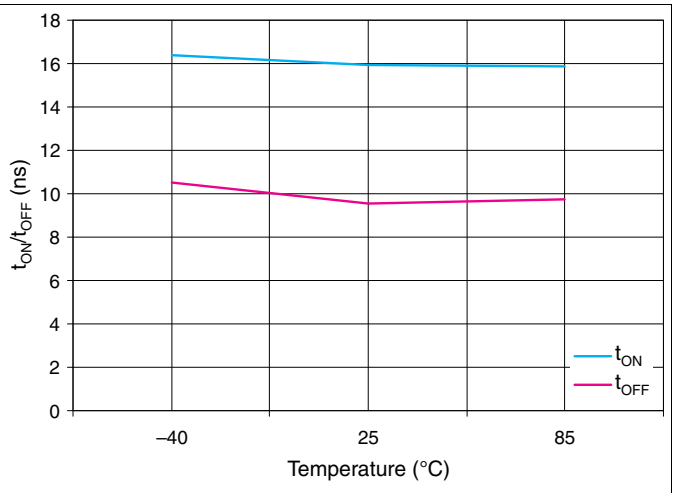


Figure 8. t_{ON} and t_{OFF} vs Temperature (V_{CC} = 4.3 V)

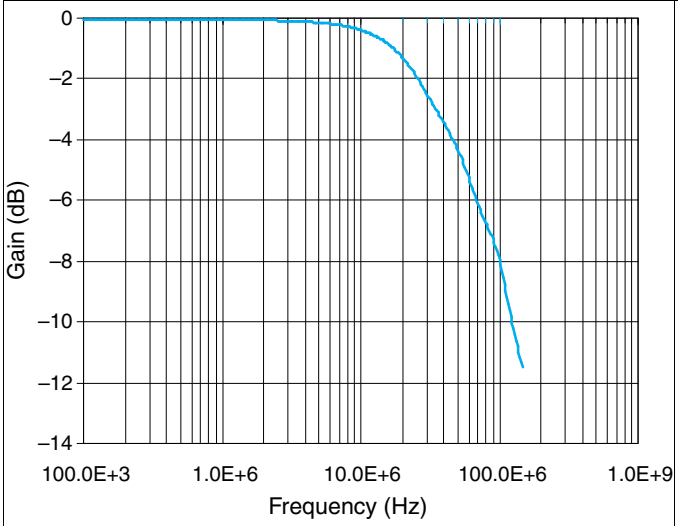


Figure 9. Bandwidth

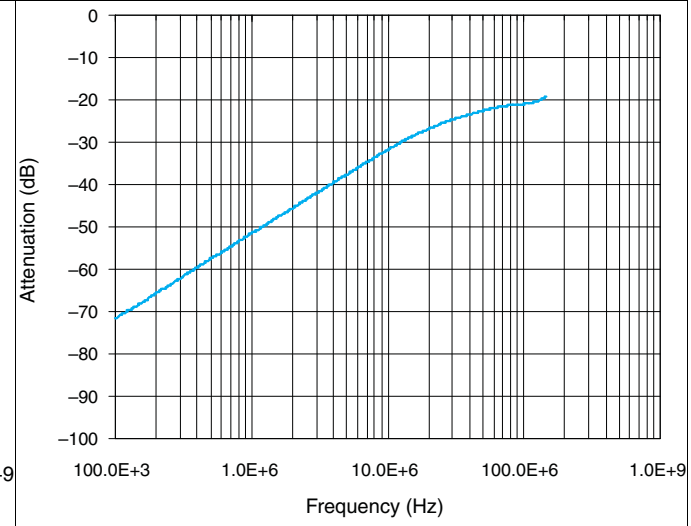


Figure 10. OFF Isolation

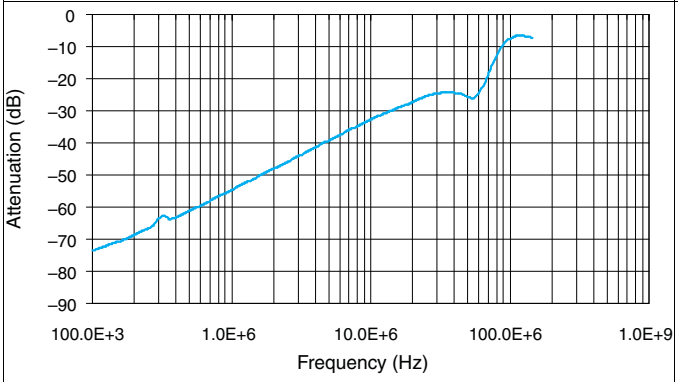


Figure 11. Crosstalk

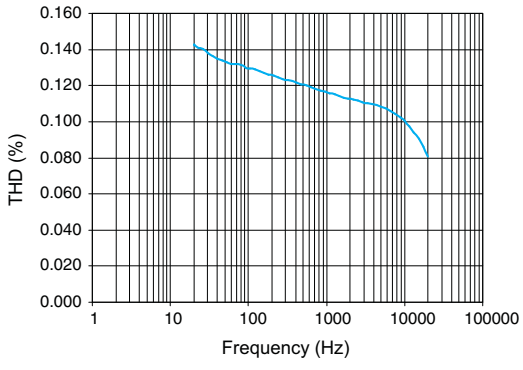


Figure 12. Total Harmonic Distortion vs Frequency (V_{CC} = 1.8 V)

Typical Characteristics (continued)

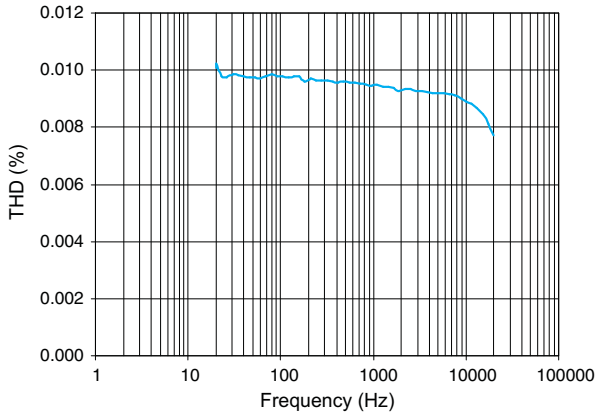


Figure 13. Total Harmonic Distortion vs Frequency (V_{CC} = 2.5 V)

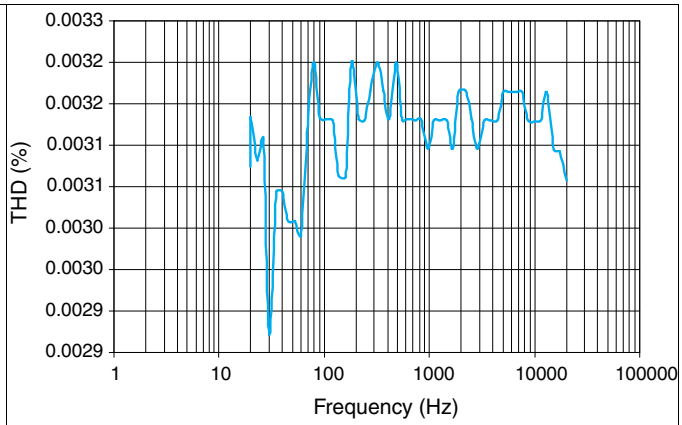


Figure 14. Total Harmonic Distortion vs Frequency (V_{CC} = 3.3 V)

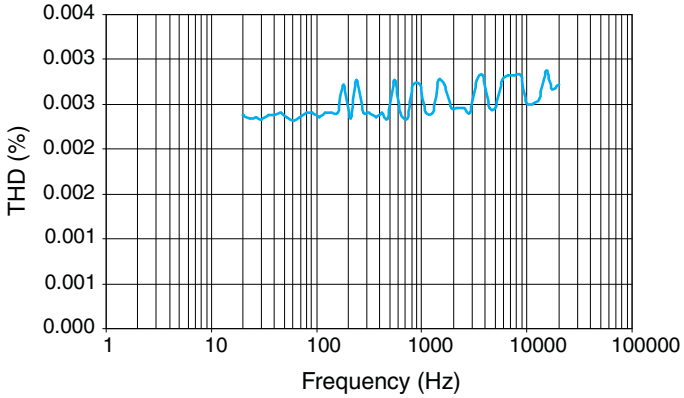


Figure 15. Total Harmonic Distortion vs Frequency (V_{CC} = 4.3 V)

7 Parameter Measurement Information

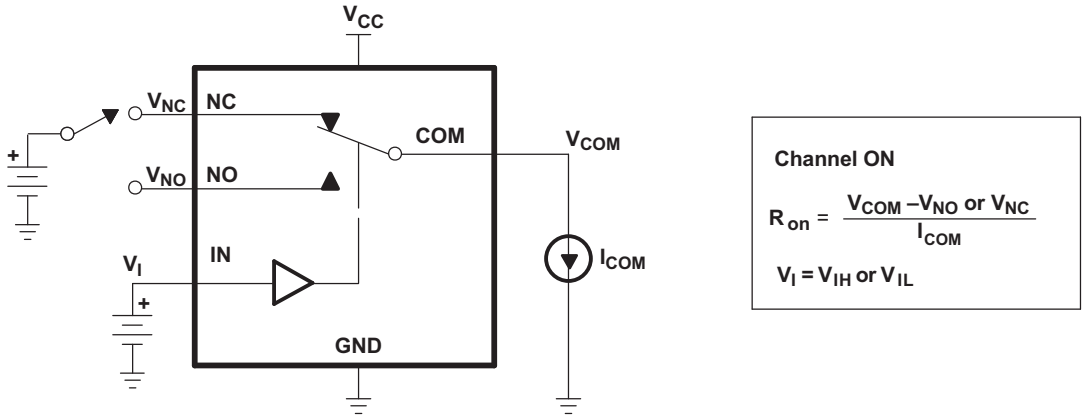


Figure 16. ON-state Resistance (R_{ON})

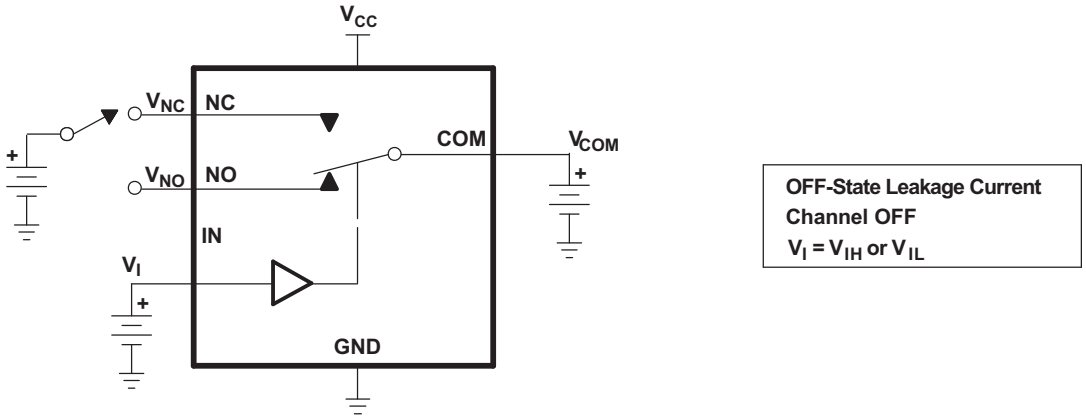


Figure 17. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

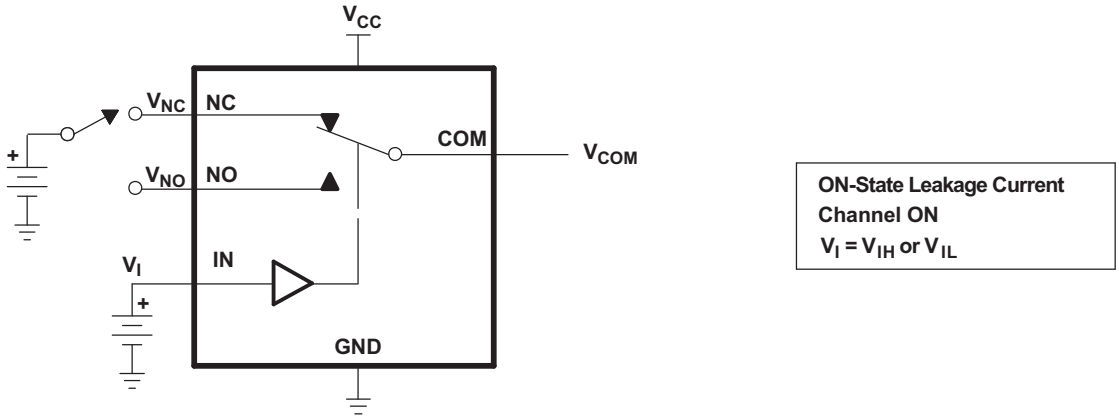


Figure 18. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

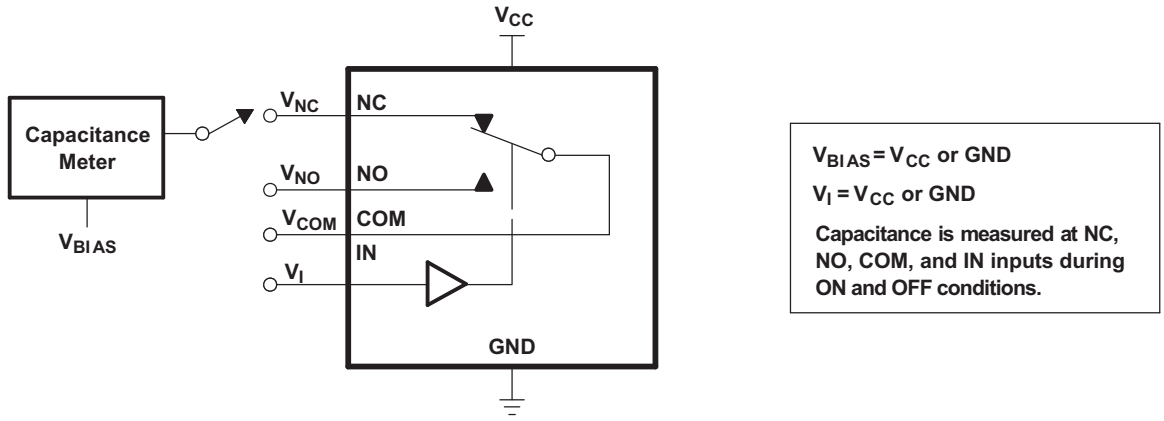
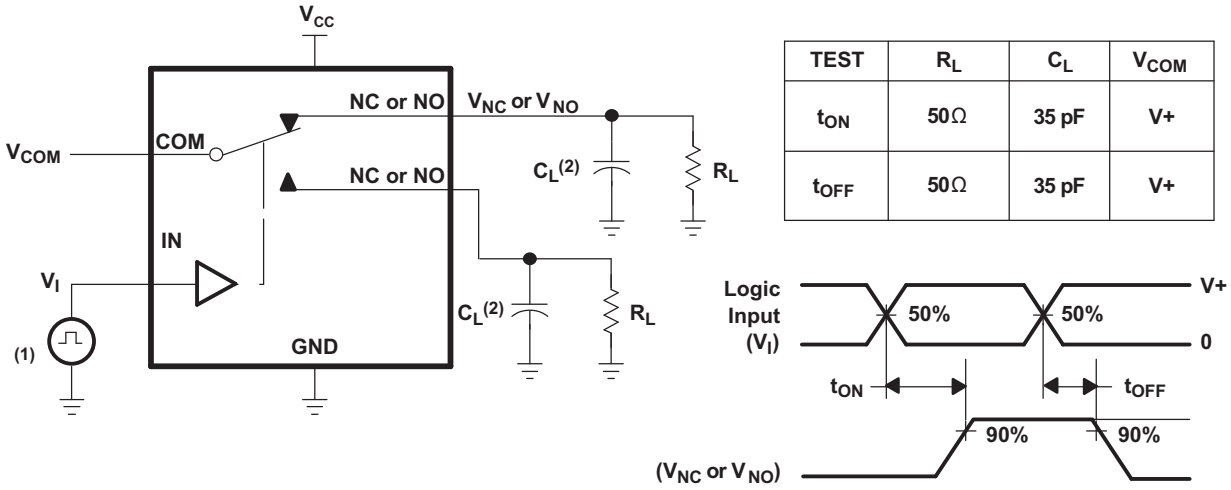


Figure 19. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50Ω	35 pF	V+
t_{OFF}	50Ω	35 pF	V+

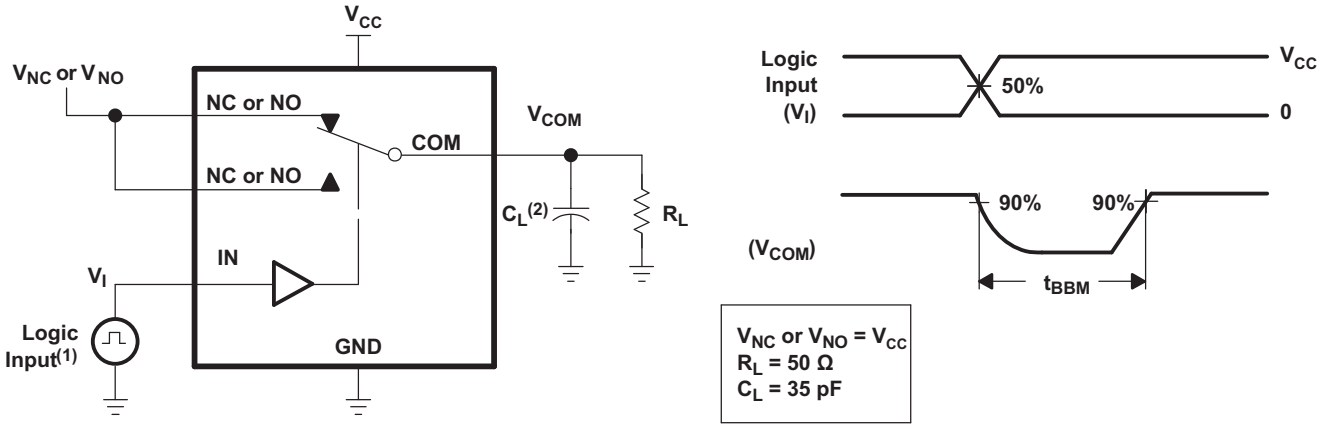
A. All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 20. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 21. Break-Before-Make Time (t_{BBM})

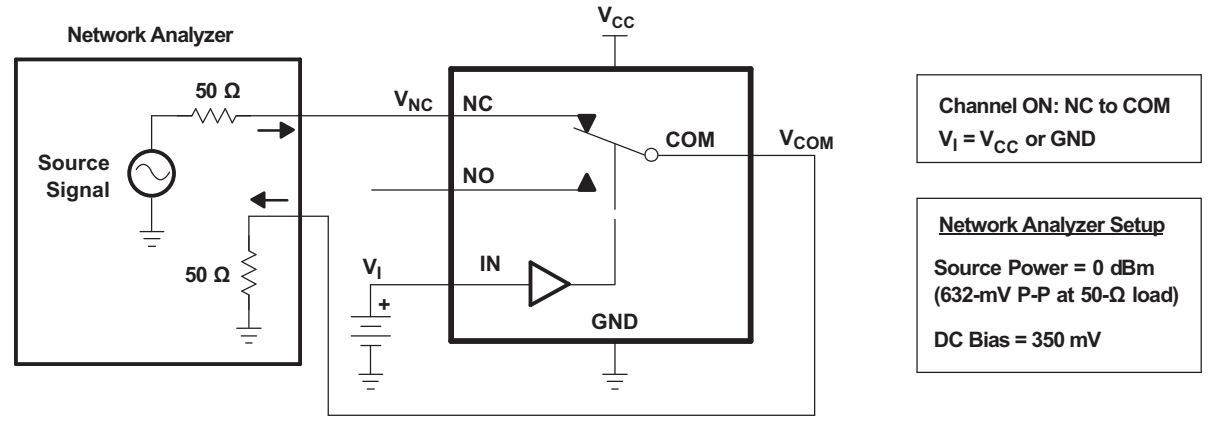


Figure 22. Bandwidth (BW)

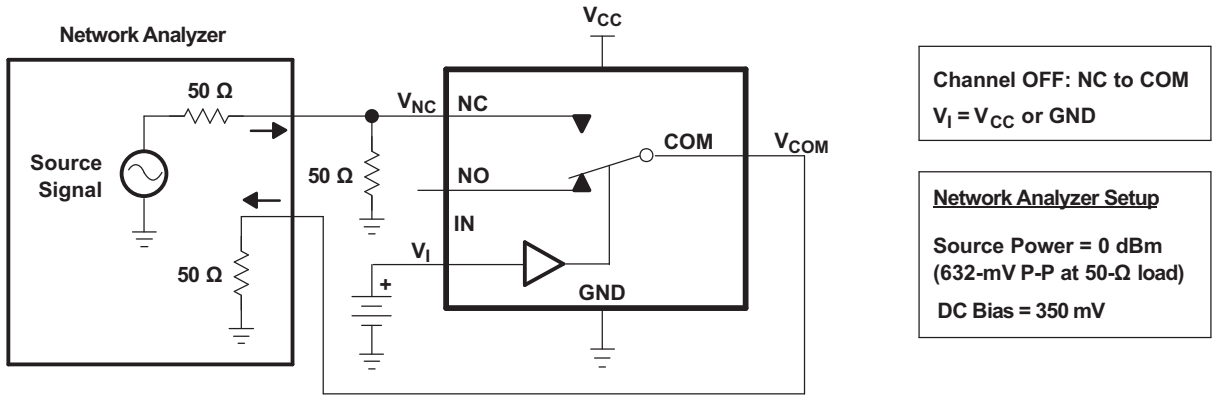


Figure 23. OFF Isolation (O_{ISO})

Parameter Measurement Information (continued)

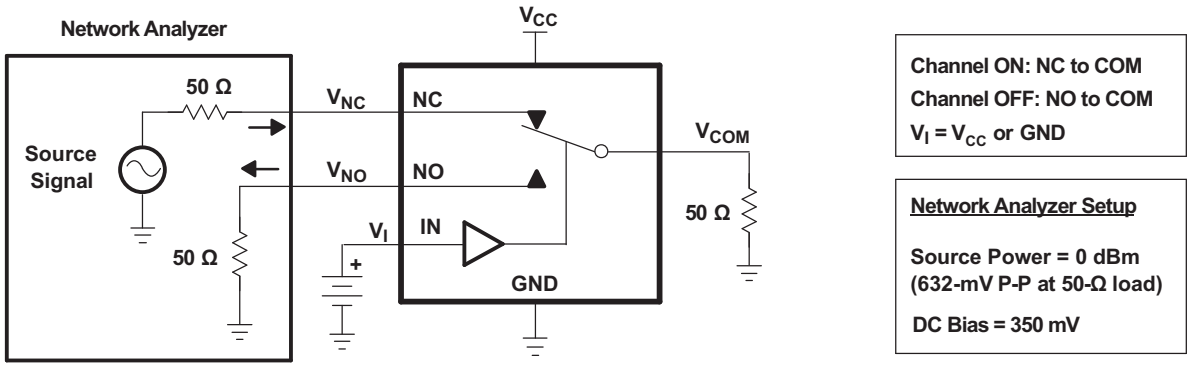
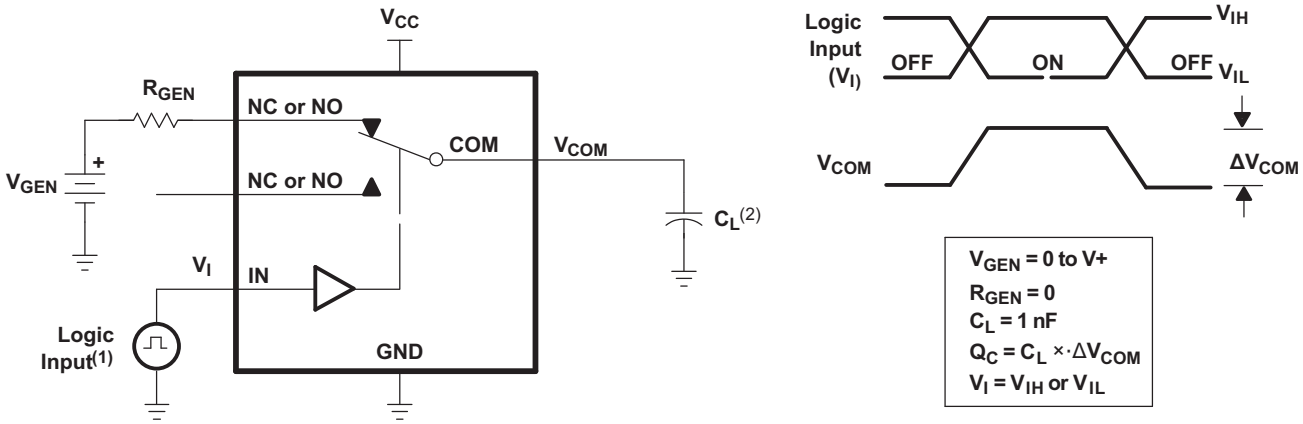


Figure 24. Crosstalk (X_{TALK})



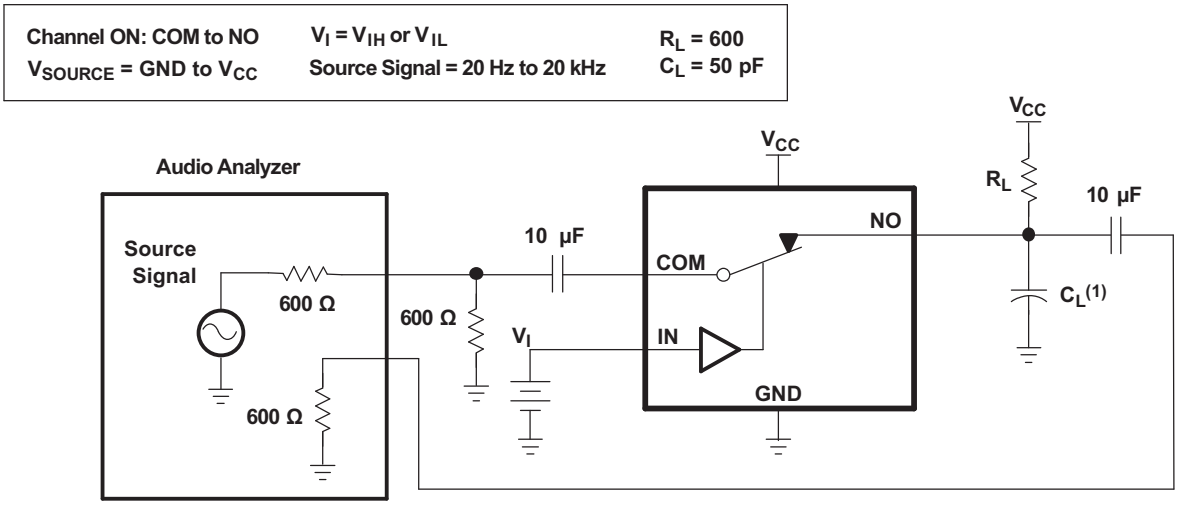
A. All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 25. Charge Injection (Q_C)

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

Figure 26. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A44159 is a bidirectional 4-channel single-pole double-throw (SPDT) analog switch with two control inputs, which is designed to operate from 1.65 V to 4.3 V. This device is also known as a 2-channel, double-pole, double-throw (DPDT) configuration. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature that prevents signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

8.2 Functional Block Diagram

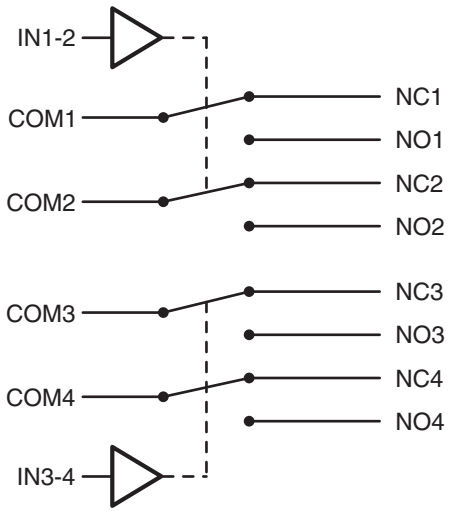


Figure 27. Logic Diagram

8.3 Feature Description

The TS3A44159 is a bidirectional device that has two sets of two single-pole double-throw switches. The four channels of the switch are contorled by two digital signals; one digital contorl for each set of two single-pole double-throw switches.

8.4 Device Functional Modes

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

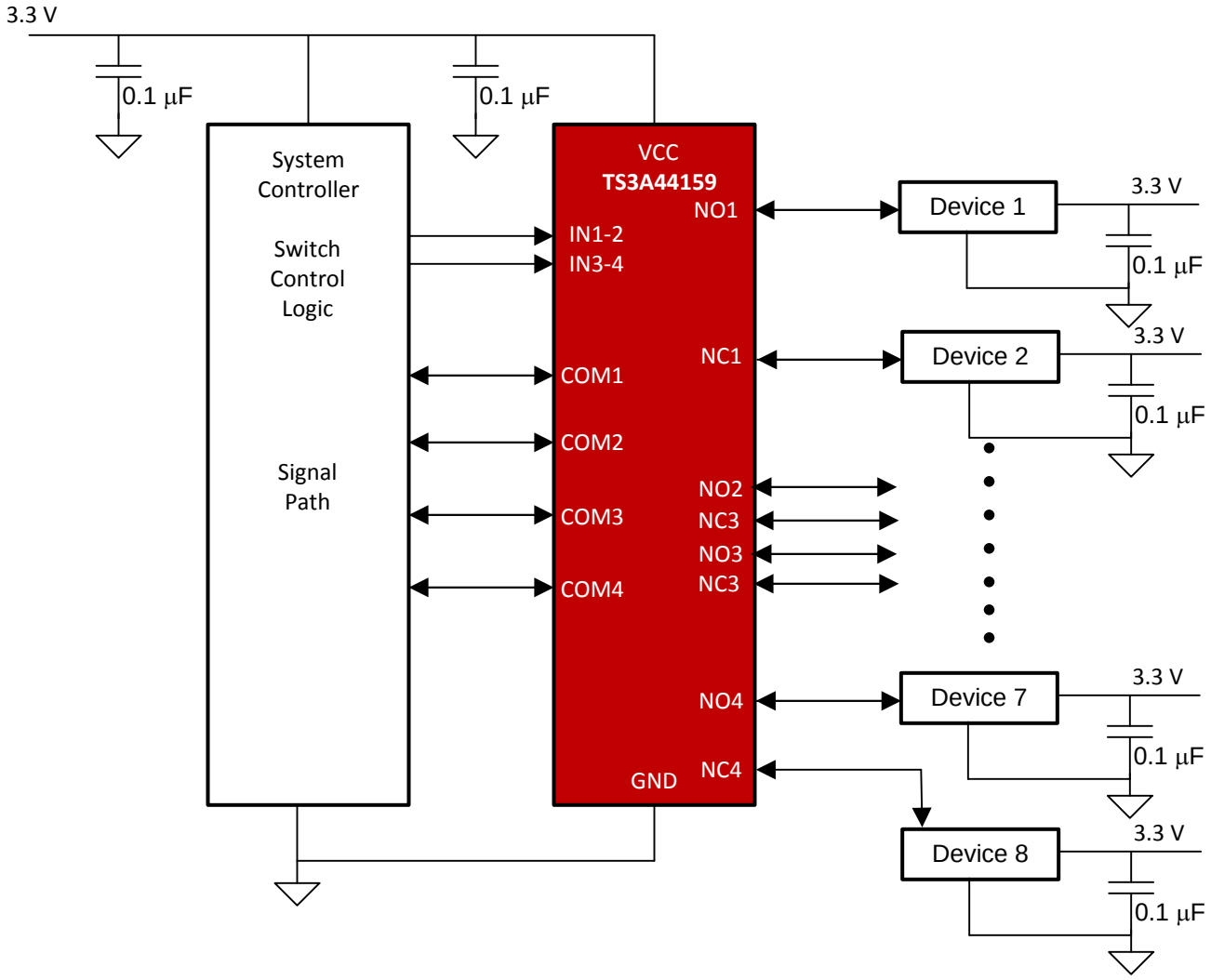


Figure 28. Typical Application Diagram

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are with in the specified ranges to ensure proper performance.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Analog Voltage	4.3 V
Digital Input Voltage	4.3 V

9.2.2 Detailed Design Procedure

The TS3A44159 can be properly operated without any external components. However, TI recommends to connect unused pins to the ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INX) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.3 Application Curve

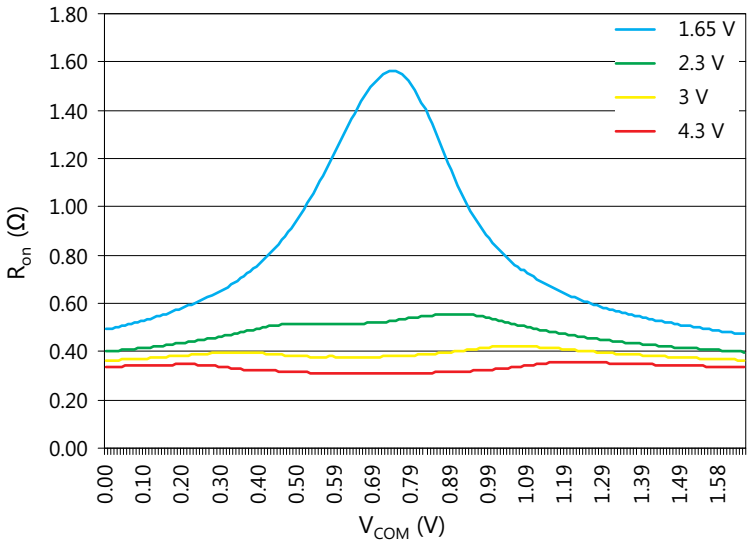


Figure 29. R_{on} vs V_{COM} (All Voltages)

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_{CC} on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-µF capacitor, connected from V_{CC} to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

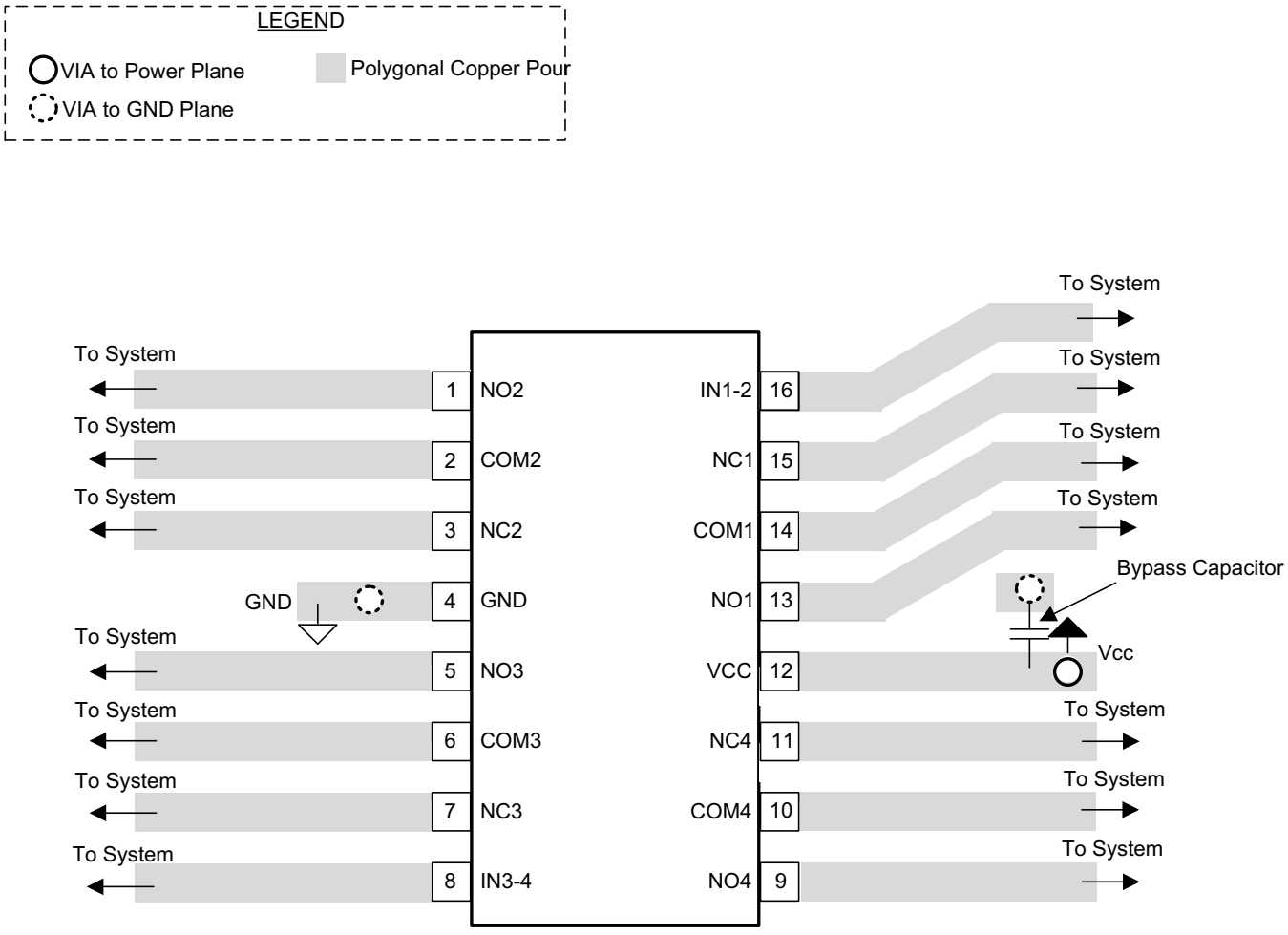


Figure 30. PCB Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A44159PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC4159	Samples
TS3A44159PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC4159	Samples
TS3A44159RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWH	Samples
TS3A44159RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWH	Samples
TS3A44159RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZWH	Samples
TS3A44159RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

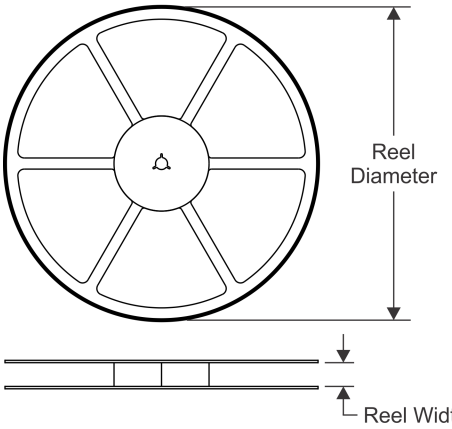
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

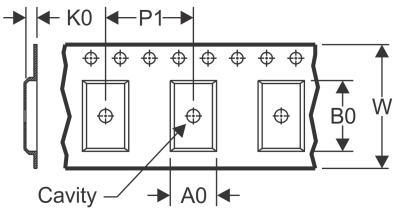
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

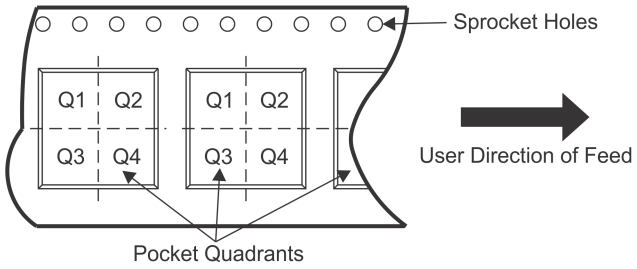


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

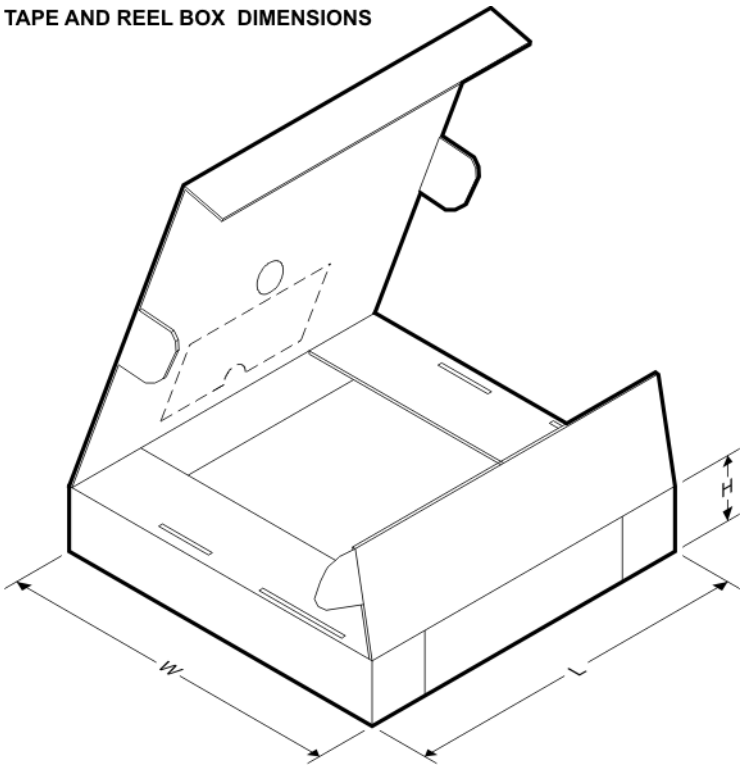
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A44159PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A44159RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TS3A44159RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TS3A44159RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

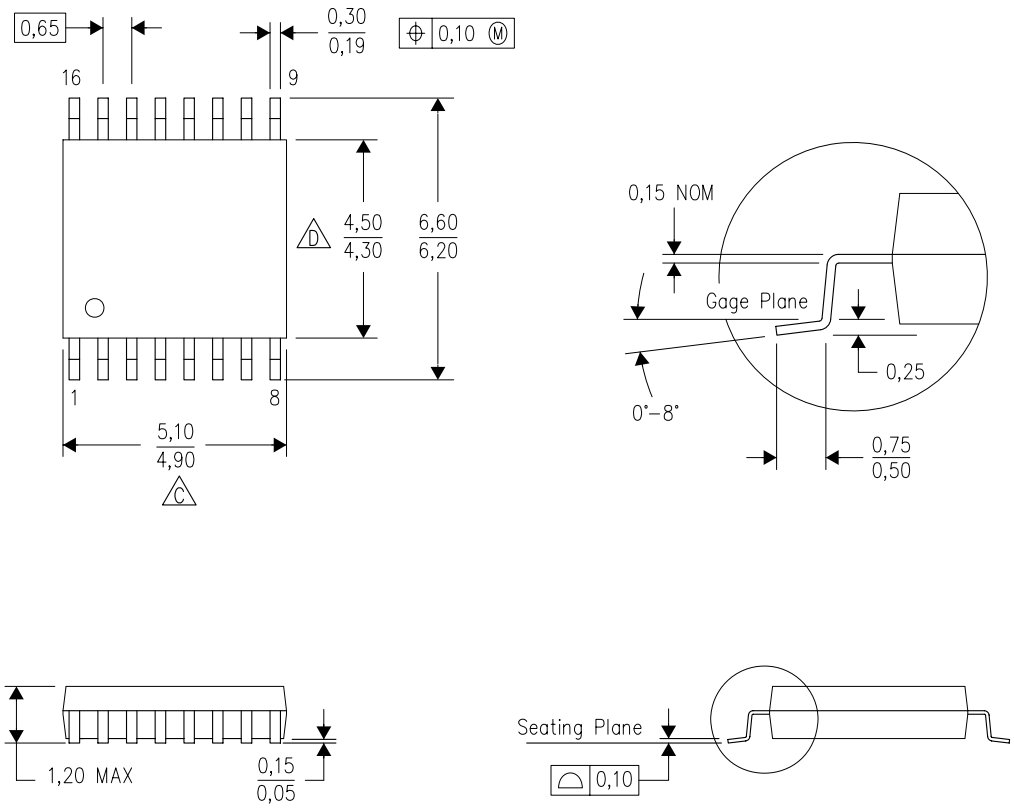
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A44159PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TS3A44159RGTR	QFN	RGT	16	3000	346.0	346.0	35.0
TS3A44159RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0
TS3A44159RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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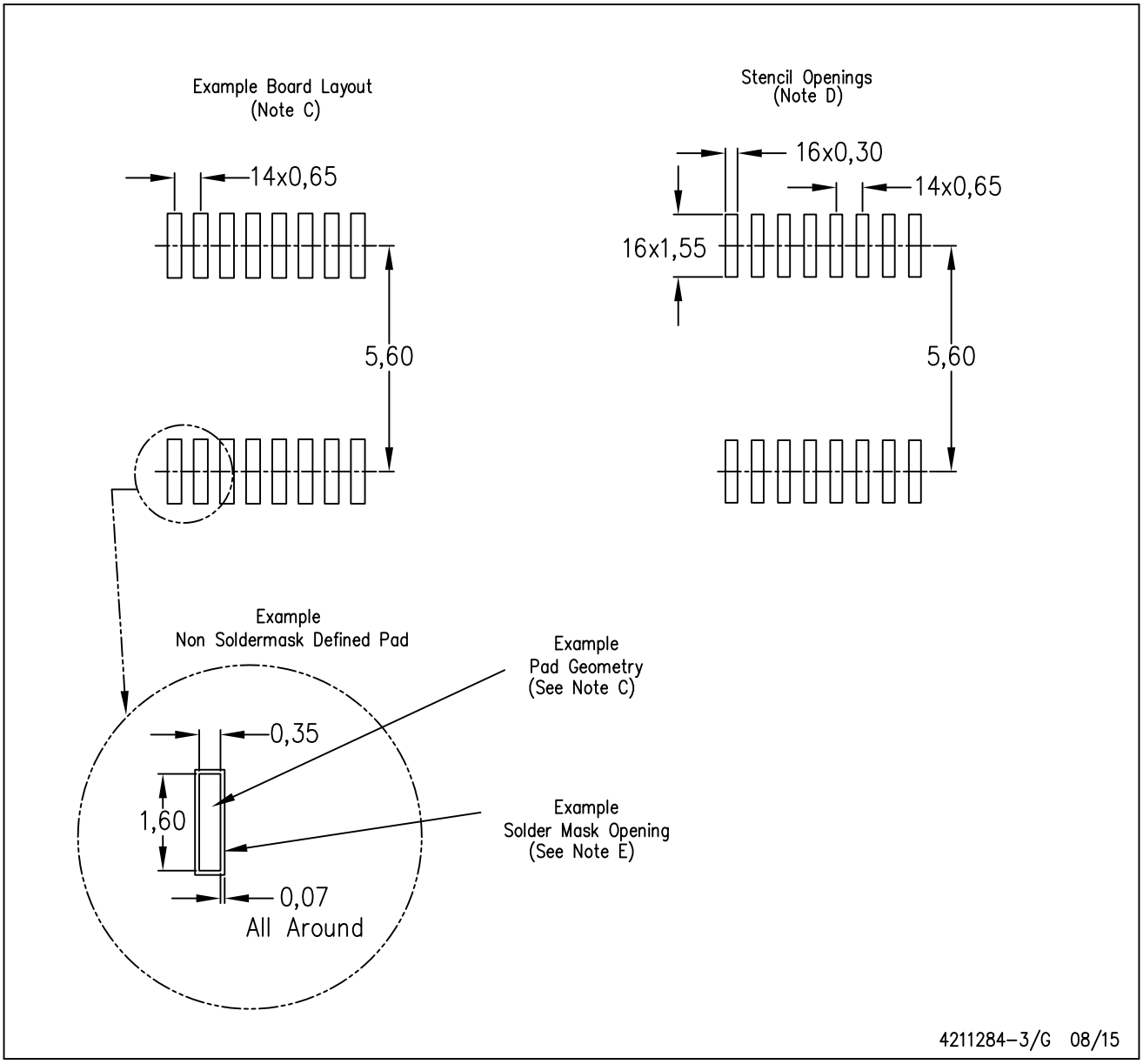
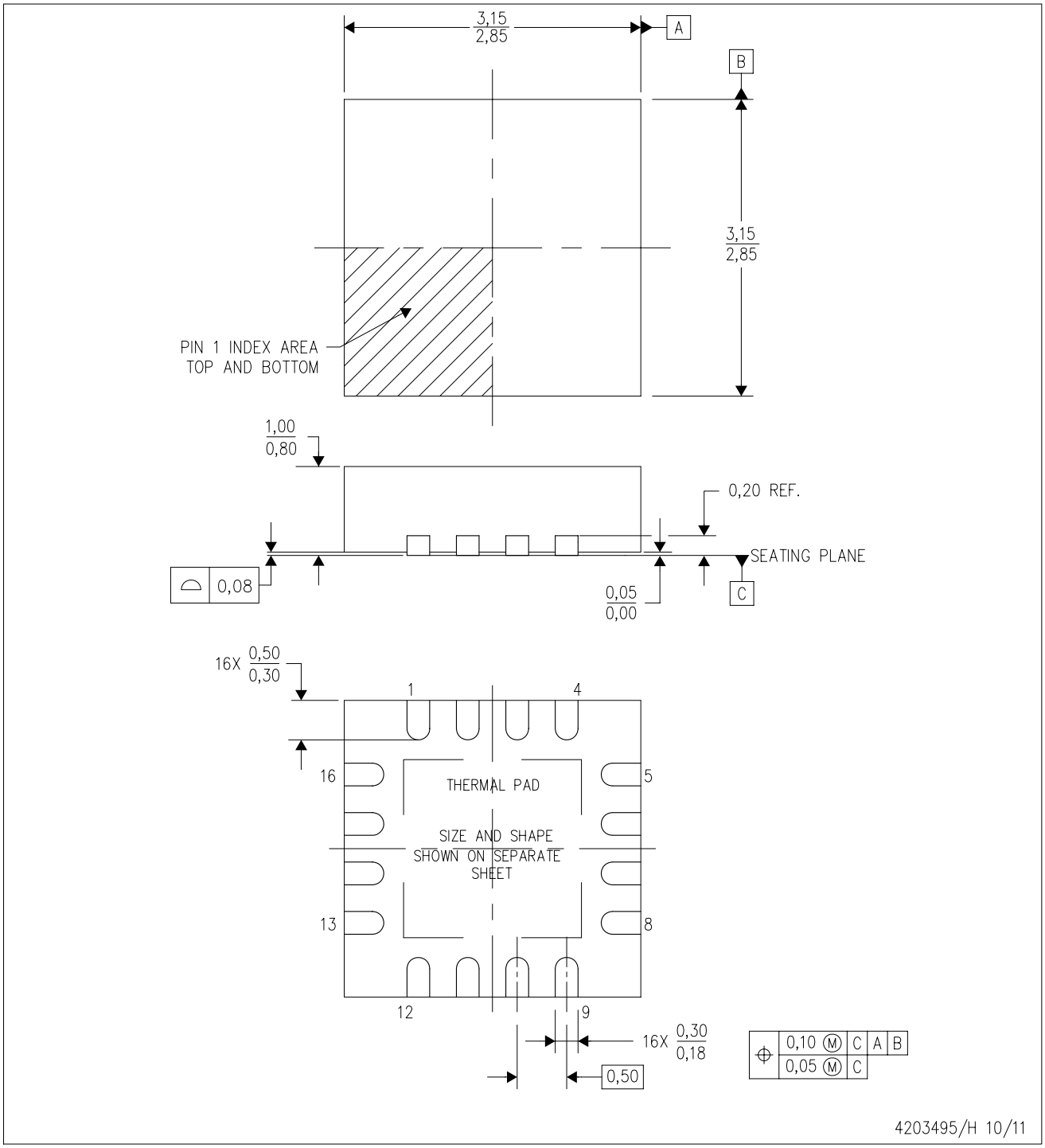
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



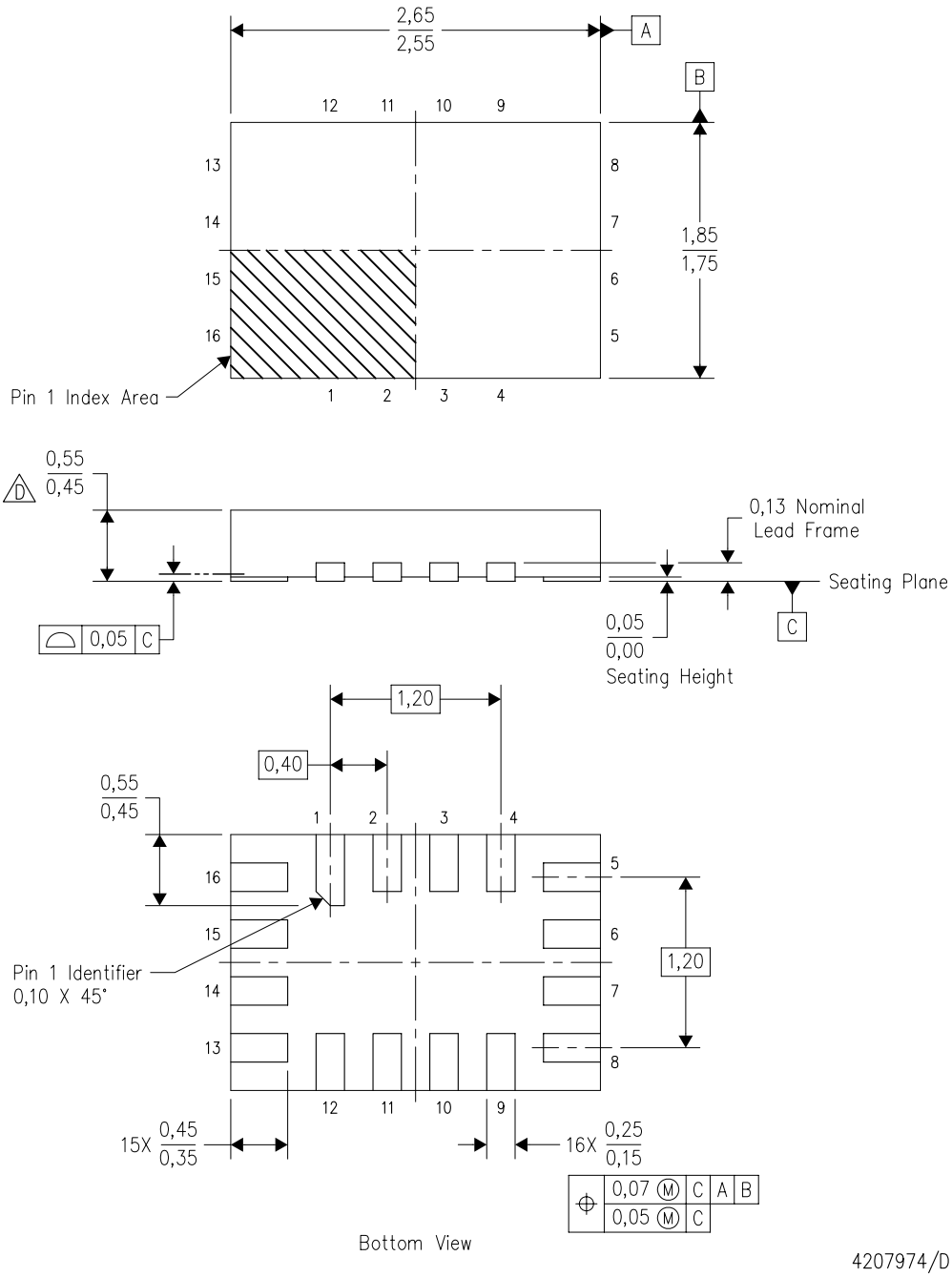
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



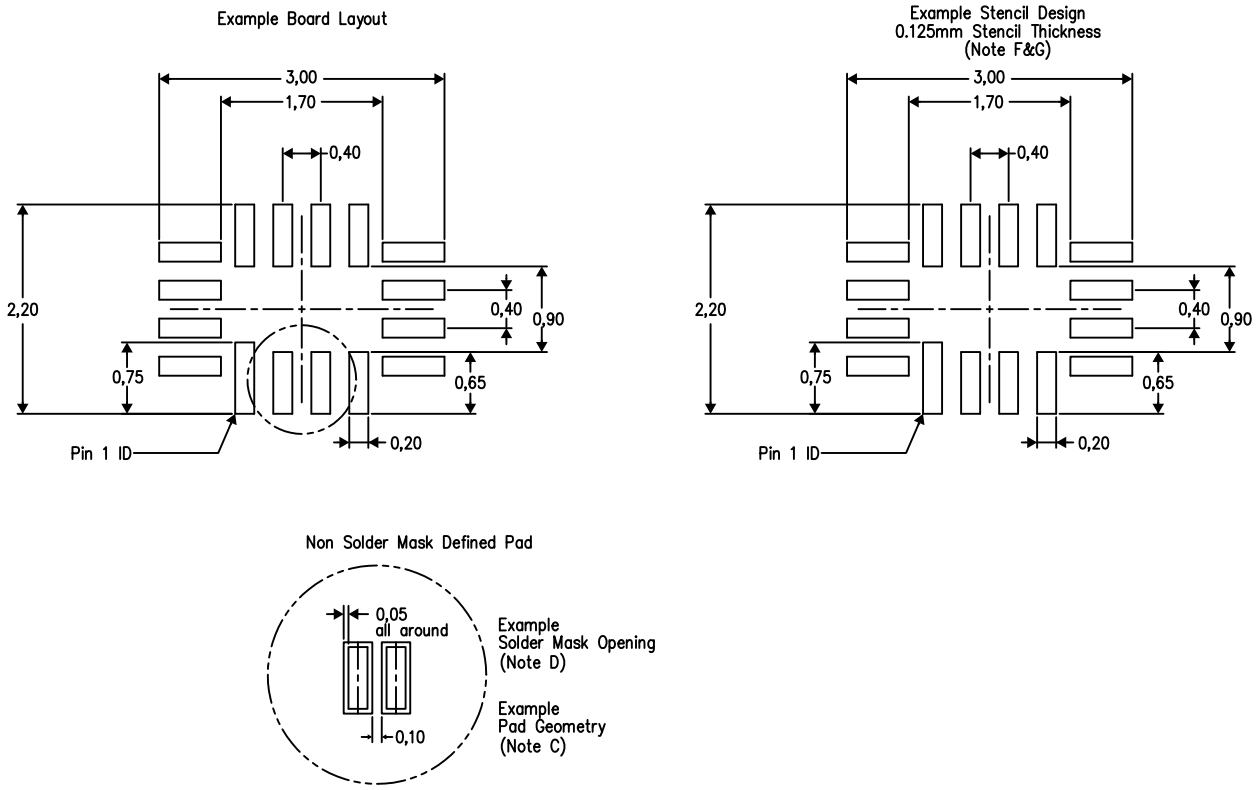
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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