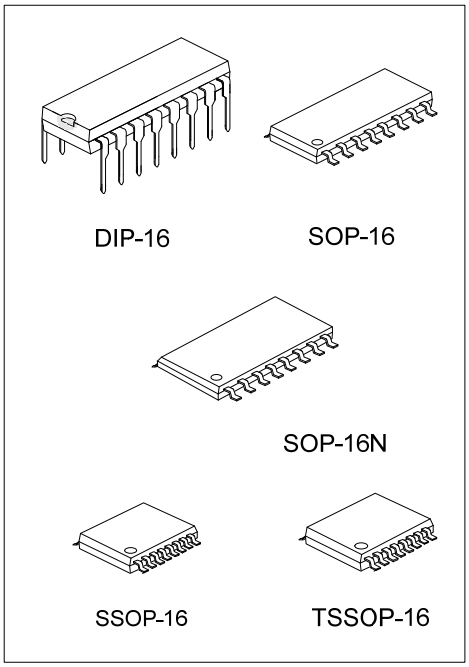
U74HC595A

CMOS IC

8-BIT SERIAL-IN SHIFT REGISTER WITH LATCHED 3-STATE PARALLEL OUTPUTS, PROVIDING SERIAL OUTPUT



■ DESCRIPTION

The UTC **74HC595A** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output. The Serial Data Input (SER) will shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

■ FEATURES

* Operation Voltage Range: 2~6V
* High Noise Immunity
* Output Compatibility with CMOS and TTL
* Specified from -40 ~ +125°C

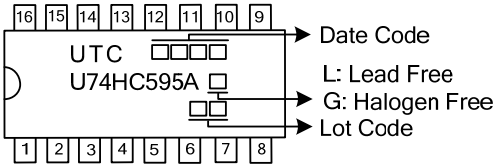
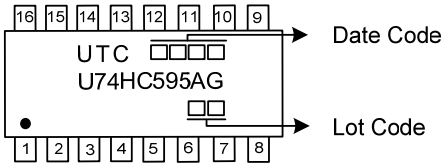
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC595AL-D16-T	U74HC595AG-D16-T	DIP-16	Tube
-	U74HC595AG-S16-R	SOP-16	Tape Reel
U74HC595AL-S16N-R	U74HC595AG-S16N-R	SOP-16N	Tape Reel
-	U74HC595AG-R16-R	SSOP-16	Tape Reel
-	U74HC595AG-P16-R	TSSOP-16	Tape Reel

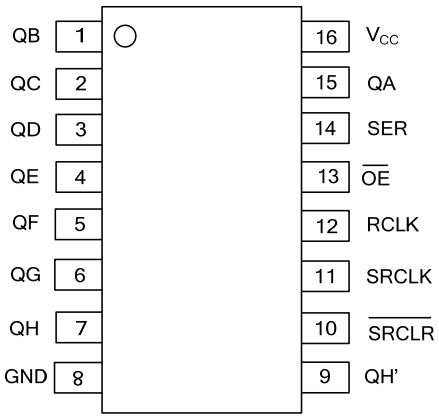
U74HC595AL-D16-T
(1)Packing Type
(2)Package Type
(3)Green Package

(1) T: Tube, R: Tape Reel
(2) D16: DIP-16, S16: SOP-16, S16N: SOP-16N
R16: SSOP-16, P16: TSSOP-16
(3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING

DIP-16	SOP-16 / SOP-16N / SSOP-16 / TSSOP-16
	

■ PIN CONFIGURATION

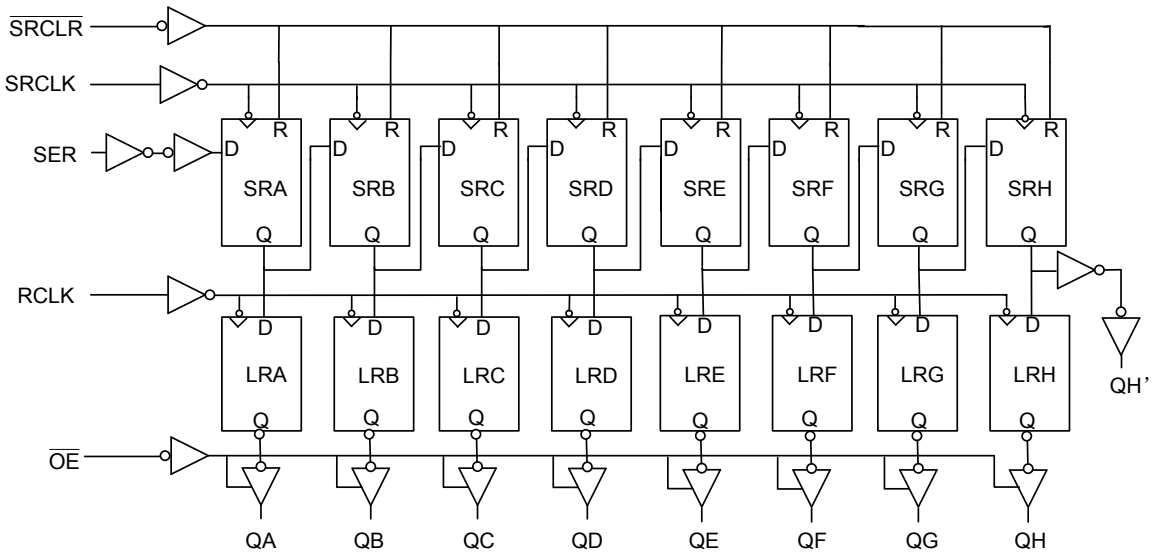


■ FUNCTION TABLE

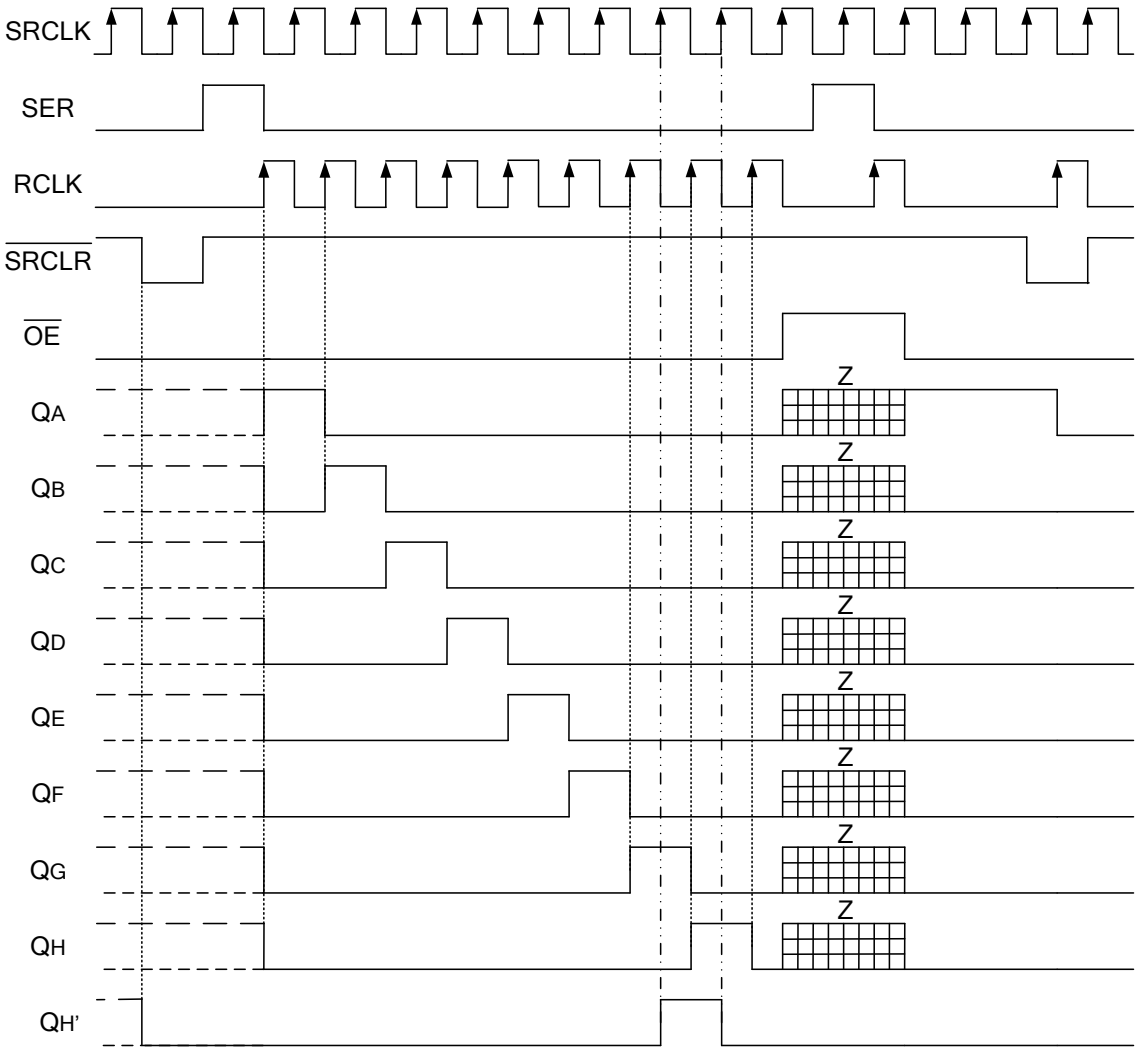
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note:H : HIGH voltage level.
L : LOW voltage level.
X : Don't care.
Z : High impedance OFF-state.
NC: No change.
↑ : Low-to-High transition.
↓ : High-to-Low transition.

■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 2)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5~7.0	V
Input Clamp Current (V_{IN} <0)		I_{IK}	±20	mA
Output Clamp Current (V_{OUT} <0)		I_{OK}	±20	mA
Output Current		I_{OUT}	±35	mA
V_{CC} or GND Current		I_{CC}	±75	mA
Power Dissipation	DIP-16	P_D	750	mW
	SOP-16		500	mW
	SOP-16N		550	mW
	SSOP-16 TSSOP-16		450	mW
Storage Temperature		T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2		6	V
Input Voltage		V_{IN}	0		V_{CC}	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Operating Temperature		T_A	-40		125	°C
Input Transition Rise or Fall Rate	V_{CC}=2V	Δt/Δv			1000	ns
	V_{CC}=4.5V				500	ns
	V_{CC}=6V				400	ns

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-level input voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=3V	2.1			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
LOW-lever output voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=3V			0.9	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
High-Level Output Voltage, Q_A-Q_H	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	2.0		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		V
		V_{CC}=6V, I_{OH}=-20μA	5.9	6.0		V
		V_{CC}=3V, I_{OH}=-2.4mA	2.48			V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98			V
		V_{CC}=6V, I_{OH}=-7.8mA	5.48			V
Low-Level Output Voltage, Q_A-Q_H	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=3V, I_{OL}=2.4mA			0.26	V
		V_{CC}=4.5V, I_{OL}=6mA			0.26	V
		V_{CC}=6V, I_{OL}=7.8mA			0.26	V
High-Level Output Voltage, Q_H	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	2.0		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		V
		V_{CC}=6V, I_{OH}=-20μA	5.9	6.0		V
		V_{CC}=3V, I_{OH}=-2.4mA	2.48			V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48			V
Low-Level Output Voltage, Q_H	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=3V, I_{OL}=2.4mA			0.26	V
		V_{CC}=4.5V, I_{OL}=4mA			0.26	V
		V_{CC}=6V, I_{OL}=5.2mA			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}=V_{CC} or GND			±0.1	μA
Output OFF -state current	I_{OZ}	V_{CC}=6V, V_{OUT}=V_{CC} or GND			±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA
Input Capacitance	C_{IN}	V_{CC}=6V, V_{IN}=V_{CC} or GND			10	pF

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{max}	C_L=50pF	V_{CC}=2V	6	26		MHz
			V_{CC}=4.5V	30	38		MHz
			V_{CC}=6V	35	42		MHz
Propagation delay from input (SRCLK) to output ($Q_{H'}$)	t_{PD}	C_L=50pF	V_{CC}=2V		50	140	ns
			V_{CC}=4.5V		17	28	ns
			V_{CC}=6V		14	24	ns
Propagation delay from input (RCLK) to output (Q_A-Q_H)		C_L=50pF	V_{CC}=2V		50	140	ns
			V_{CC}=4.5V		17	28	ns
			V_{CC}=6V		14	24	ns
		C_L=150pF	V_{CC}=2V		60	200	ns
			V_{CC}=4.5V		22	40	ns
			V_{CC}=6V		19	34	ns
Propagation delay from input ($\overline{SRCLR}$) to output ($Q_{H'}$)	t_{PHL}	C_L=50pF	V_{CC}=2V		51	145	ns
			V_{CC}=4.5V		18	29	ns
			V_{CC}=6V		15	25	ns
Propagation delay from input ($\overline{OE}$) to output (Q_A-Q_H)	t_{en}	C_L=50pF	V_{CC}=2V		40	135	ns
			V_{CC}=4.5V		15	27	ns
			V_{CC}=6V		13	23	ns
		C_L=150pF	V_{CC}=2V		70	200	ns
			V_{CC}=4.5V		23	40	ns
			V_{CC}=6V		19	34	ns
Propagation delay from input ($\overline{OE}$) to output (Q_A-Q_H)	t_{dis}	C_L=50pF	V_{CC}=2V		42	150	ns
			V_{CC}=4.5V		23	30	ns
			V_{CC}=6V		20	26	ns
Propagation delay to output (Q_A-Q_H)	t_t	C_L=50pF	V_{CC}=2V		28	60	ns
			V_{CC}=4.5V		8	12	ns
			V_{CC}=6V		6	10	ns
		C_L=150pF	V_{CC}=2V		45	210	ns
			V_{CC}=4.5V		17	42	ns
			V_{CC}=6V		13	36	ns
Propagation delay to output ($Q_{H'}$)		C_L=50pF	V_{CC}=2V		28	75	ns
			V_{CC}=4.5V		8	15	ns
			V_{CC}=6V		6	13	ns

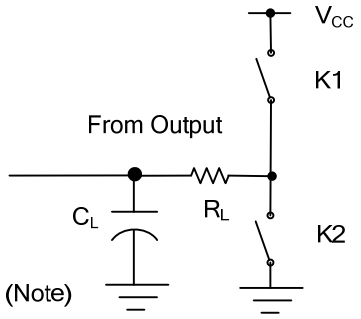
■ TIMING REQUIREMENTS (T_A=25°C,unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse duration, SRCLK or RCLK high or low	t_W	V_{CC}=2V	80			ns
		V_{CC}=4.5V	16			ns
		V_{CC}=6V	14			ns
Pulse duration, $\overline{\text{SRCLR}}$ Low		V_{CC}=2V	80			ns
		V_{CC}=4.5V	16			ns
		V_{CC}=6V	14			ns
Setup Time, SER before SRCLK↑	t_{SU}	V_{CC}=2V	100			ns
		V_{CC}=4.5V	20			ns
		V_{CC}=6V	17			ns
Setup Time, SRCLK↑ before RCLK↑		V_{CC}=2V	75			ns
		V_{CC}=4.5V	15			ns
		V_{CC}=6V	13			ns
Setup Time, $\overline{\text{SRCLR}}$ low before RCLK↑		V_{CC}=2V	50			ns
		V_{CC}=4.5V	10			ns
		V_{CC}=6V	9			ns
Setup Time, $\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑		V_{CC}=2V	50			ns
		V_{CC}=4.5V	10			ns
		V_{CC}=6V	9			ns
Hold Time, SER after SRCLK↑	t_H	V_{CC}=2V	3			ns
		V_{CC}=4.5V	3			ns
		V_{CC}=6V	3			ns

■ OPERATING CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		400		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

Note: C_L includes probe and jig capacitance. C_L=50pF, R_L=1KΩ