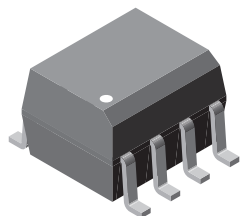
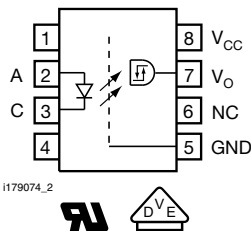




## High Speed Optocoupler, Single, 5 MBd, in SOIC-8 Package



i179074



i179074\_2



### FEATURES

- Data rate 5 Mbits/s (2.5 Mbit/s over temperature)
- Buffer
- Isolation test voltage, 4000 V<sub>RMS</sub>
- TTL, LSTTL and CMOS compatible
- Internal shield for very high common mode transient immunity
- Wide supply voltage range (4.5 V to 15 V)
- Low input current (1.6 mA to 5 mA)
- Parameters specified from 0 °C to 85 °C
- T<sub>amb</sub> from -40 °C to 100 °C
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

RoHS  
COMPLIANT

### DESCRIPTION

The single channel 5 Mb/s SFH6720 and SFH6721 high speed optocoupler consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector. The detector incorporates a Schmitt-trigger stage for improved noise immunity. A Faraday shield provides a common mode transient immunity of 1000 V/μs at V<sub>CM</sub> = 50 V for SFH6720 and 2500 V/μs at V<sub>CM</sub> = 400 V for SFH6721.

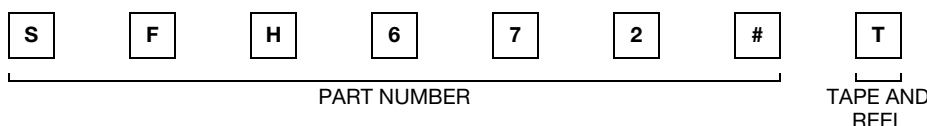
### AGENCY APPROVALS

- UL1577, file no. E52744 system code Y
- DIN EN 60747-5-5 (VDE 0884) available with option 1

### APPLICATIONS

- Industrial control
- Replace pulse transformers
- Routine logic interfacing
- Motion / power control
- High speed line receiver
- Microprocessor system interfaces
- Computer peripheral interfaces

### ORDERING INFORMATION



AGENCY CERTIFIED/PACKAGE	CMR (kV/μs)	CMR (kV/μs)
UL	1	2.5
SOIC-8	SFH6720T	SFH6721T
VDE, UL	1	2.5
SOIC-8	SFH6720-X001T	-

### TRUTH TABLE (positive logic)

PART	IR DIODE	OUTPUT
SFH6720	On	H
	Off	L
SFH6721	On	H
	Off	L



ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
<b>INPUT</b>				
Reverse voltage		$V_R$	3	V
DC forward current		$I_F$	10	mA
Surge forward	$t_p \leq 1\text{ }\mu\text{s}$ , 300 pulses/s	$I_{FSM}$	1	mA
Power dissipation		$P_{diss}$	20	mW
<b>OUTPUT</b>				
Supply voltage		$V_{CC}$	-0.5 to +15	V
Output voltage		$V_O$	-0.5 to +15	V
Average output current		$I_O$	25	mA
Power dissipation		$P_{diss}$	100	mW
<b>COUPLER</b>				
Storage temperature range		$T_{stg}$	-55 to +125	$^{\circ}\text{C}$
Ambient temperature range		$T_{amb}$	+ 85	$^{\circ}\text{C}$
Lead soldering temperature	$t = 10\text{ s}$	$T_{slid}$	260	$^{\circ}\text{C}$

**Note**

- <sup>(1)</sup> Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability

RECOMMENDED OPERATING CONDITIONS <sup>(1)</sup>						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		$V_{CC}$	4.5		15	V
Forward input current		$I_{Fon}$	1.6 <sup>(2)</sup>		5	mA
		$I_{Foff}$			0.1	mA
Operating temperature		$T_A$	-40		85	$^{\circ}\text{C}$

**Notes**

- <sup>(1)</sup> A 0.1  $\mu\text{F}$  bypass capacitor connected between pins 5 and 8 must be used  
<sup>(2)</sup> We recommended using a 2.2 mA if to permit at least 20 % CTR degradation guard band

ELECTRICAL CHARACTERISTICS <sup>(1)</sup>						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>INPUT</b>						
Forward voltage	$I_F = 5\text{ mA}$ , $25\text{ }^{\circ}\text{C}$	$V_F$		1.6	1.75	V
		$V_F$			1.9	V
Input current hysteresis	$V_{CC} = 5\text{ V}$ , $I_{HYS} = I_{Fon} - I_{Foff}$	$I_{HYS}$	0.1			V
Reverse current	$V_R = 3\text{ V}$	$I_R$		0.5	10	$\mu\text{A}$
Capacitance	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$	$C_O$		60		pF
Thermal resistance		$R_{thja}$		700		K/W



ELECTRICAL CHARACTERISTICS (1)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>OUTPUT</b>						
Logic low output voltage	$I_{OL} = 6.4 \text{ mA}$	$V_{OL}$			0.5	V
Logic high output voltage	$I_{OH} = -2.6 \text{ mA}$ , $V_{OH} = V_{CC} - 1.8 \text{ V}$	$V_{OH}$	2.4			V
Output leakage current ( $V_{OUT} > V_{CC}$ )	$V_O = 5.5 \text{ V}$ , $V_{CC} = 4.5 \text{ V}$ , $I_F = 5 \text{ mA}$	$I_{OHH}$		0.5	100	$\mu\text{A}$
	$V_O = 15 \text{ V}$ , $V_{CC} = 4.5 \text{ V}$ , $I_F = 5 \text{ mA}$	$I_{OHH}$		1	500	$\mu\text{A}$
Logic low supply current	$V_{CC} = 5.5 \text{ V}$ , $I_F = 0$	$I_{CCL}$		3.7	6	mA
	$V_{CC} = 15 \text{ V}$ , $I_F = 0$	$I_{CCL}$		4.1	6.5	mA
Logic high supply current	$V_{CC} = 5.5 \text{ V}$ , $I_F = 5 \text{ mA}$	$I_{CCH}$		3.4	4	mA
	$V_{CC} = 15 \text{ V}$ , $I_F = 5 \text{ mA}$	$I_{CCH}$		3.7	5	mA
Logic low short circuit output current (output short circuit time $\leq 10 \text{ ms}$ )	$V_O = V_{CC} = 5.5 \text{ V}$ , $I_F = 0$	$I_{OSL}$	25			mA
	$V_O = V_{CC} = 15 \text{ V}$ , $I_F = 0$	$I_{OSL}$	40			mA
Logic high short circuit output current (output short circuit time $\leq 10 \text{ ms}$ )	$V_{CC} = 5.5 \text{ V}$ , $V_O = 0 \text{ V}$ , $I_F = 5 \text{ mA}$	$I_{OSH}$			-10	mA
	$V_{CC} = 15 \text{ V}$ , $V_O = 0 \text{ V}$ , $I_F = 5 \text{ mA}$	$I_{OSH}$			-25	mA
Thermal resistance		$R_{thja}$		300		K/W
<b>COUPLER</b>						
Capacitance (input to output)	$f = 1 \text{ MHz}$ , pins 1 to 4 and 5 to 8 shorted together	$C_{IO}$		0.6		pF

**Note**

(1)  $-40^\circ\text{C} \leq T_{amb} \leq 85^\circ\text{C}$ ;  $4.5 \text{ V} \leq V_{CC} \leq 15 \text{ V}$ ;  $1.6 \text{ mA} \leq I_{Fon} \leq 5 \text{ mA}$ ;  $2 \leq V_{EH} \leq 15 \text{ V}$ ;  $0 \leq V_{EL} \leq 0.8 \text{ V}$ ;  $0 \text{ mA} \leq I_{Foff} \leq 0.1 \text{ mA}$ .

Typical values:  $T_{amb} = 25^\circ\text{C}$ ;  $V_{CC} = 5 \text{ V}$ ;  $I_{Fon} = 3 \text{ mA}$  unless otherwise specified.

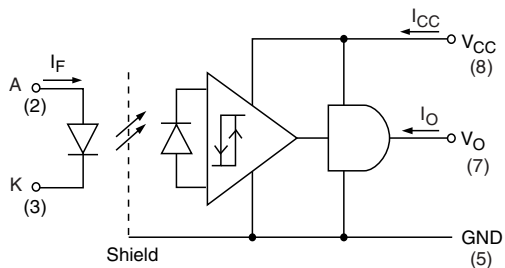
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements

SWITCHING CHARACTERISTICS (1)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low output level	Without peaking capacitor	$t_{PHL}$		120		ns
	With peaking capacitor	$t_{PHL}$		115	300	ns
Propagation delay time to logic high output level	Without peaking capacitor	$t_{PLH}$		125		ns
	With peaking capacitor	$t_{PLH}$		90	300	ns
Output rise time	10 % to 90 %	$t_r$		40		ns
Output fall time	90 % to 10 %	$t_f$		10		ns

**Note**

(1)  $0^\circ\text{C} \leq T_{amb} \leq 85^\circ\text{C}$ ;  $4.5 \text{ V} \leq V_{CC} \leq 15 \text{ V}$ ;  $1.6 \text{ mA} \leq I_{Fon} \leq 5 \text{ mA}$ ;  $0 \text{ mA} \leq I_{Foff} \leq 0.1 \text{ mA}$

Typical values:  $T_{amb} = 25^\circ\text{C}$ ;  $V_{CC} = 5 \text{ V}$ ;  $I_{Fon} = 3 \text{ mA}$  unless otherwise specified. A  $0.1 \mu\text{F}$  bypass capacitor connected between pins 5 and 8 must be used



isfh6720\_00

**COMMON MODE TRANSIENT IMMUNITY (1)**

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic high common mode transient immunity (2)	$ V_{CM}  = 50 \text{ V}$ , $I_F = 1.6 \text{ mA}$	SFH6720	$ CM_H $	1000			V/ $\mu\text{s}$
	$ V_{CM}  = 300 \text{ V}$ , $I_F = 1.6 \text{ mA}$	SFH6721	$ CM_H $	5000			V/ $\mu\text{s}$
Logic low common mode transient immunity (2)	$ V_{CM}  = 50 \text{ V}$ , $I_F = 0 \text{ mA}$	SFH6720	$ CM_L $	1000			V/ $\mu\text{s}$
	$ V_{CM}  = 1000 \text{ V}$ , $I_F = 0 \text{ mA}$	SFH6721	$ CM_L $	10 000			V/ $\mu\text{s}$

**Note**(1)  $T_{amb} = 25 \text{ }^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V}$  (2)(2)  $CM_H$  is the maximum slew rate of a common mode voltage  $V_{CM}$  at which the output voltage remains at logic high level ( $V_O > 2 \text{ V}$ ).  $CM_L$  is the maximum slew rate of a common mode voltage  $V_{CM}$  at which the output voltage remains at logic low level ( $V_O < 0.8 \text{ V}$ )**SAFETY AND INSULATION RATINGS**

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		55/100/21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, $t = 1 \text{ min}$	$V_{ISO}$	3333	$V_{RMS}$
Tested withstanding isolation voltage	According to UL1577, $t = 1 \text{ s}$	$V_{ISO}$	4000	$V_{RMS}$
Maximum transient isolation voltage	According to DIN EN 60747-5-5	$V_{IOTM}$	6000	$V_{peak}$
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	$V_{IORM}$	560	$V_{peak}$
Isolation resistance	$V_{IO} = 500 \text{ V}$ , $T_{amb} = 25 \text{ }^\circ\text{C}$	$R_{IO}$	$\geq 10^{12}$	$\Omega$
	$V_{IO} = 500 \text{ V}$ , $T_{amb} = 100 \text{ }^\circ\text{C}$	$R_{IO}$	$\geq 10^{11}$	$\Omega$
Output safety power		$P_{SO}$	350	mW
Input safety current		$I_{SI}$	150	mA
Input safety temperature		$T_S$	165	$^\circ\text{C}$
Creepage distance	SOIC-8		$\geq 4$	mm
Clearance distance	SOIC-8		$\geq 4$	mm
Insulation thickness		DTI	$\geq 0.2$	mm

**Note**

As per IEC 60747-5-5, § 7.4.3.8.2, this optocoupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits

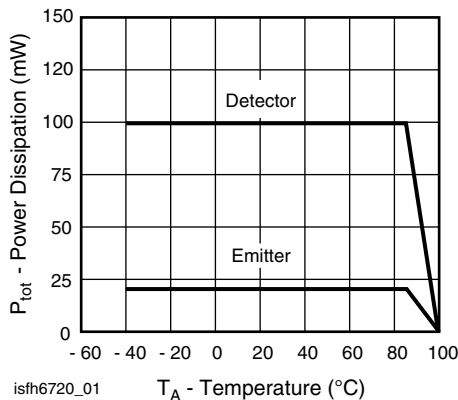
**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25 \text{ }^\circ\text{C}$ , unless otherwise specified)

Fig. 1 - Permissible Total Power Dissipation vs. Temperature

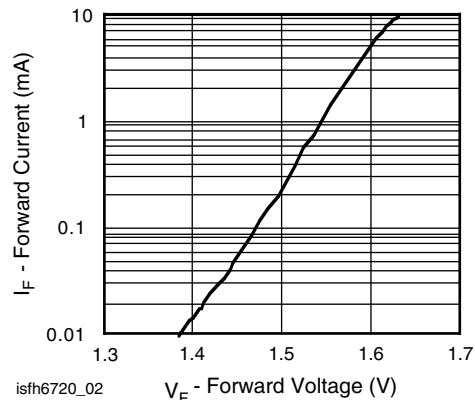


Fig. 2 - Typical Input Diode Forward Current vs. Forward Voltage

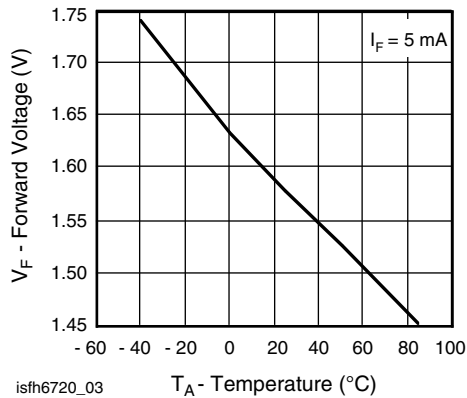


Fig. 3 - Typical Forward Input Voltage vs. Temperature

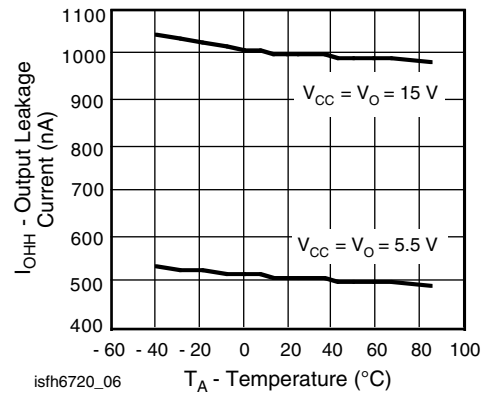


Fig. 6 - Typical Output Leakage Current vs. Temperature

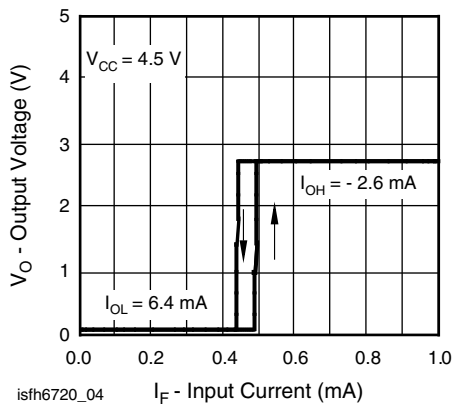


Fig. 4 - Typical Output Voltage vs. Forward Input Current

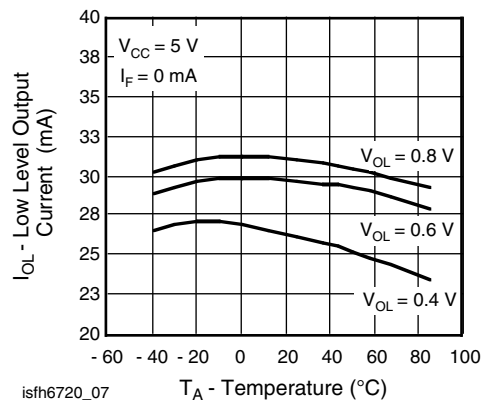


Fig. 7 - Typical Low Level Output Current vs. Temperature

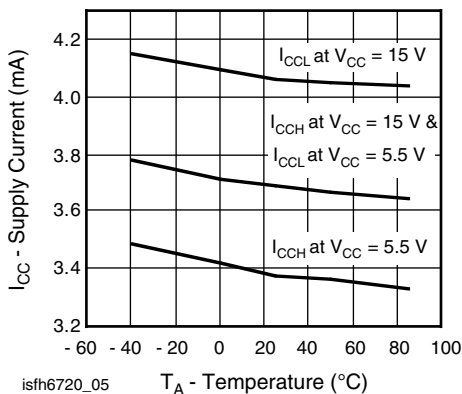


Fig. 5 - Typical Supply Current vs. Temperature

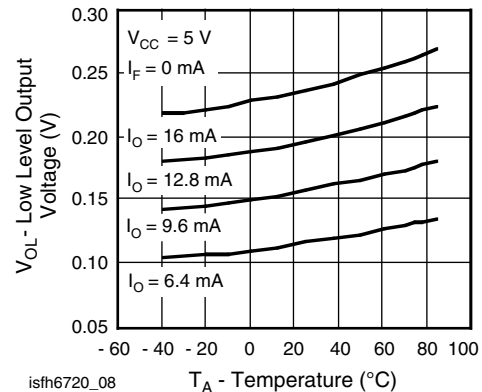


Fig. 8 - Typical Low Level Output Voltage vs. Temperature

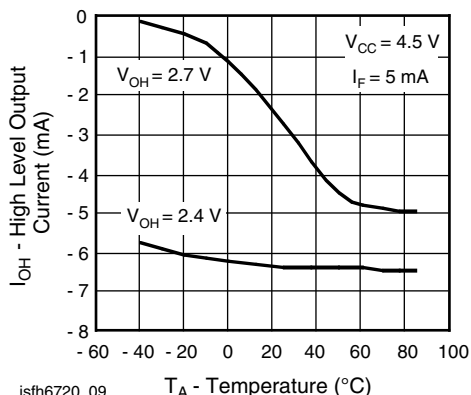


Fig. 9 - Typical High Level Output Current vs. Temperature

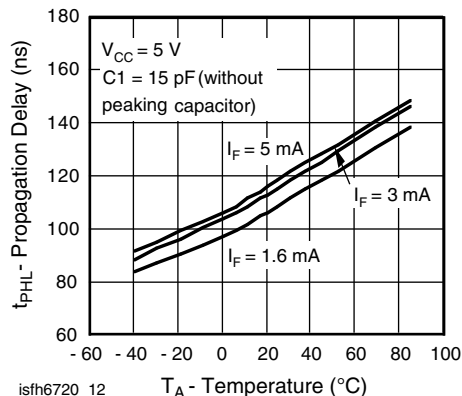


Fig. 12 - Typical Propagation Delays to Logic Low vs. Temperature

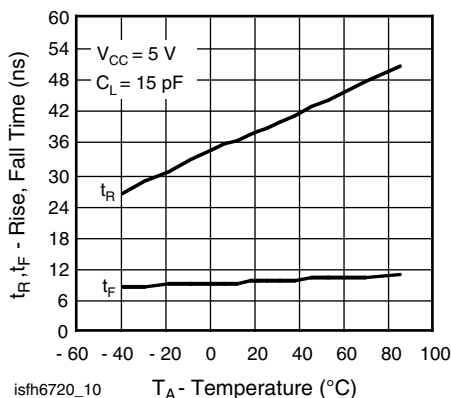


Fig. 10 - Rise and Fall Time vs. Ambient Temperature

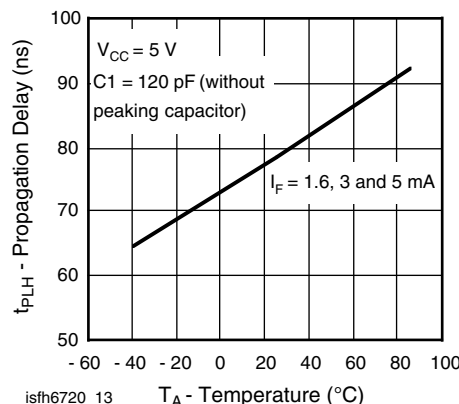


Fig. 13 - Typical Propagation Delays to Logic High vs. Temperature

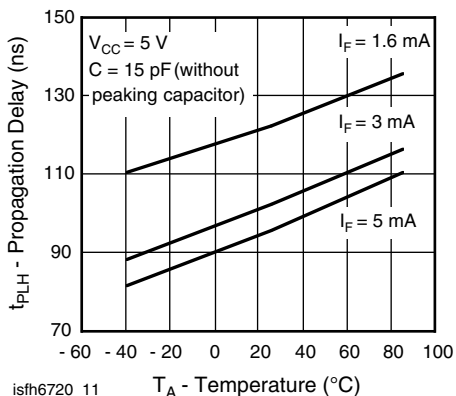


Fig. 11 - Typical Propagation Delays to Logic High vs. Temperature

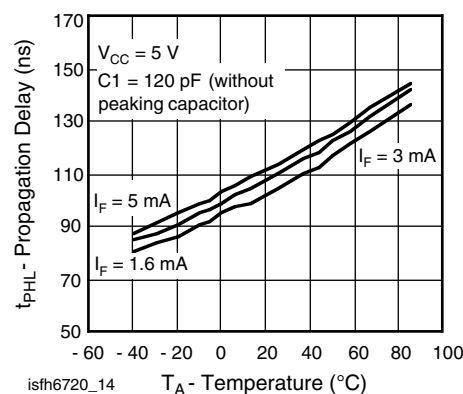


Fig. 14 - Typical Propagation Delays to Logic Low vs. Temperature

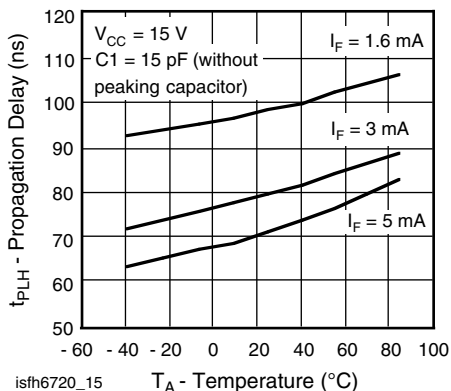


Fig. 15 - Typical Propagation Delays to Logic High vs. Temperature

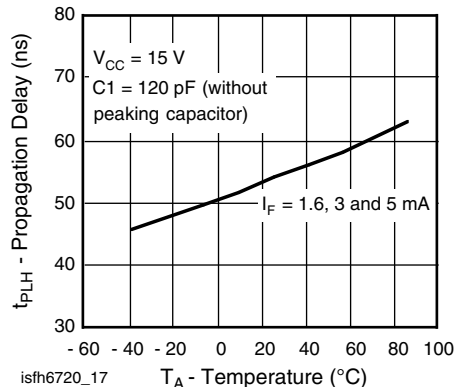


Fig. 17 - Typical Propagation Delays to Logic High vs. Temperature

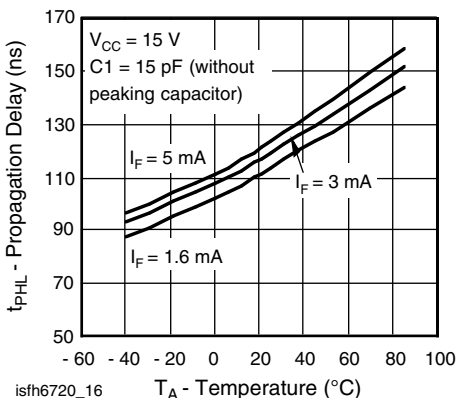


Fig. 16 - Typical Propagation Delays to Logic Low vs. Temperature

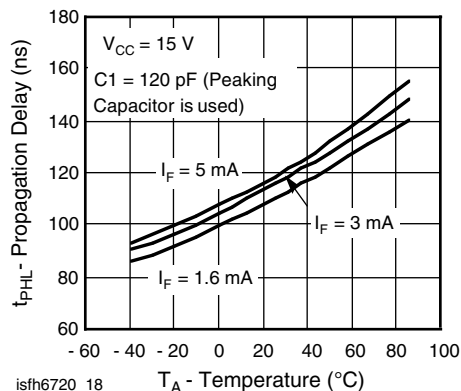


Fig. 18 - Typical Propagation Delays to Logic Low vs. Temperature

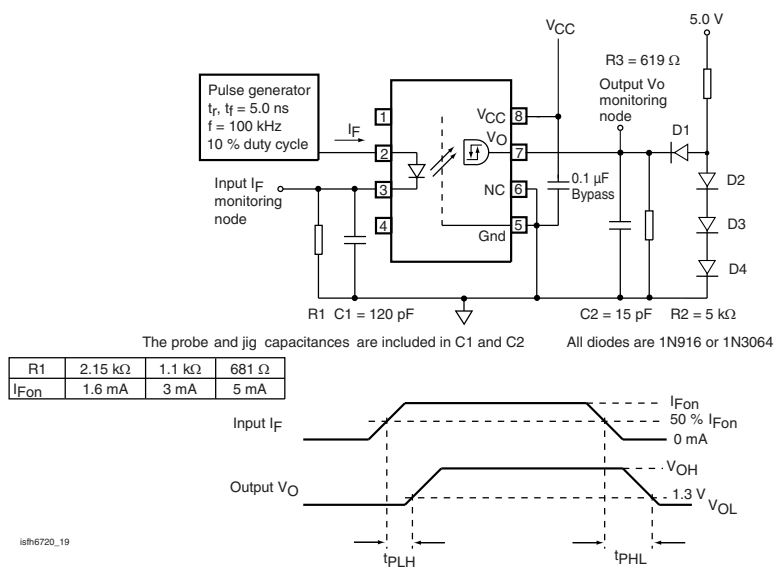


Fig. 19 - Test Circuit for tPLH, tPHL, tR and tF

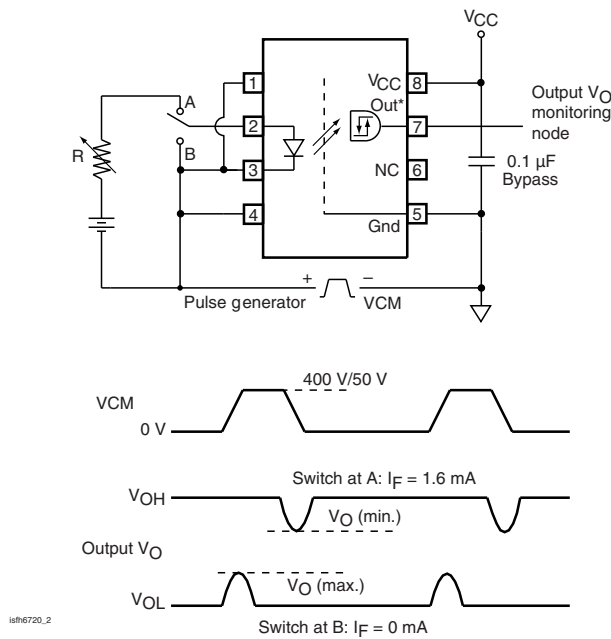


Fig. 20 - Test Circuit for Common Mode Transient Immunity and Typical Waveforms

**PACKAGE DIMENSIONS** (in millimeters)

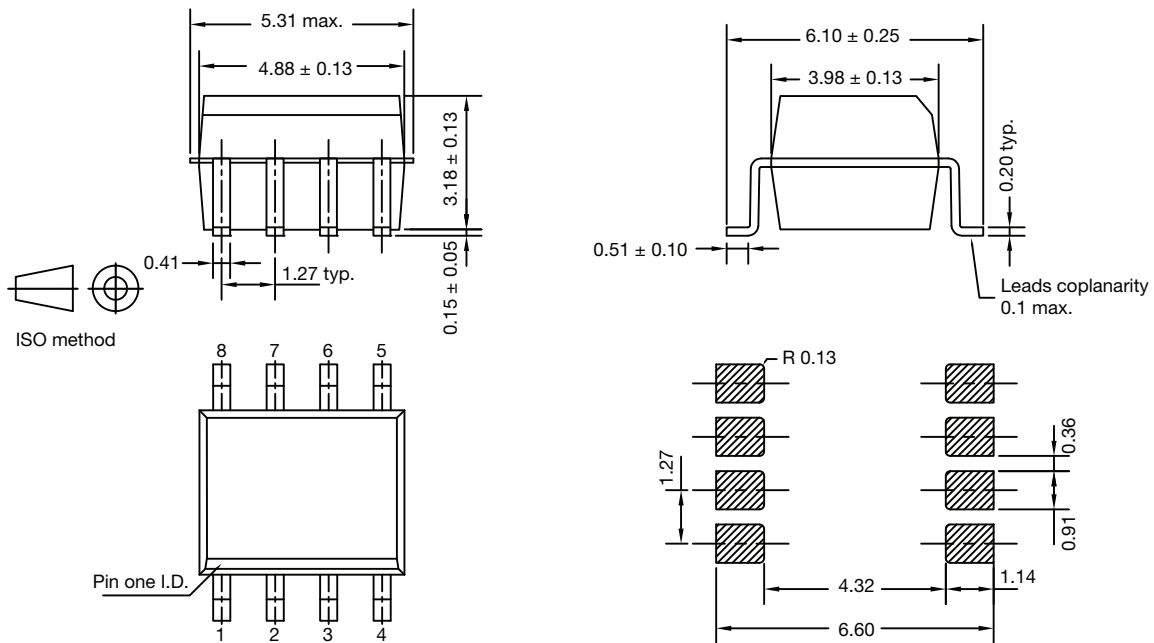


Fig. 21 - Package Dimensions

**PACKAGE MARKING**



Fig. 22 - SFH6720

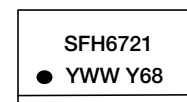


Fig. 23 - SFH6721

**Note**

- Tape and reel suffix (T) is not part of the package marking





**PACKAGE INFORMATION** (in millimeters)

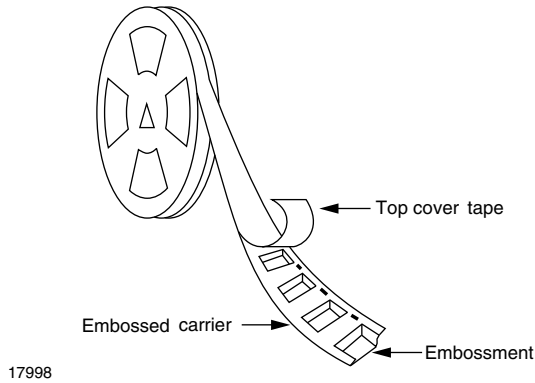


Fig. 24 - Tape and Reel Shipping Medium

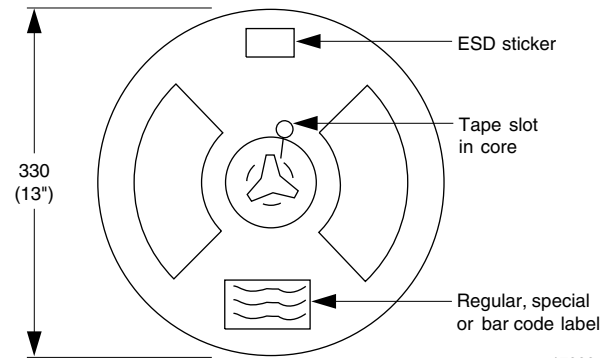


Fig. 25 - Tape and Reel Shipping Medium

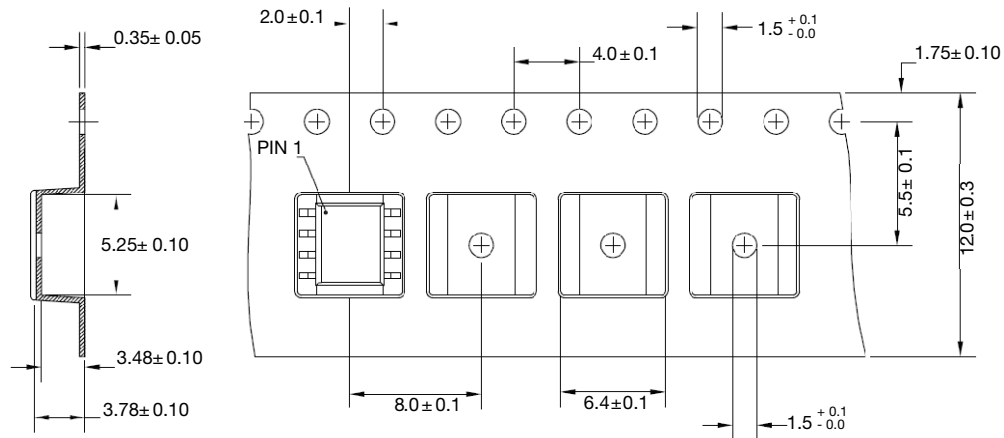


Fig. 26 - Tape and Reel Packing for SOIC (2000 pieces on reel)

**SOLDER PROFILES**

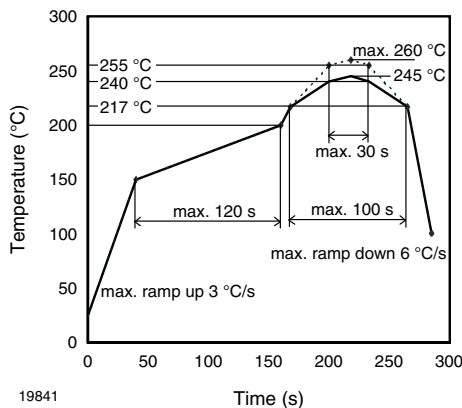


Fig. 27 - Lead (Pb)-free Reflow Solder Profile According to J-STD-020 for SMD Devices

**HANDLING AND STORAGE CONDITIONS**

ESD level: HBM class 2

Floor life: unlimited

Conditions:  $T_{amb} < 30\text{ °C}$ ,  $RH < 85\%$

Moisture sensitivity level 1, according to J-STD-020



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