Battery Disconnect Switch

DESCRIPTION

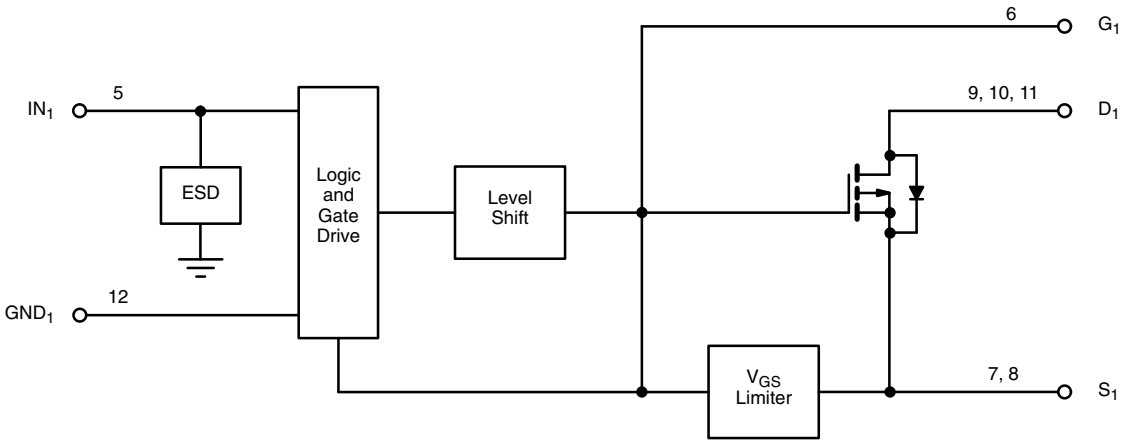
The Si4720CY is two level-shifted P-Channel MOSFETs. Operating together, these MOSFETs can be used as a reverse blocking switch for battery disconnect applications. It is a solution for multiple battery technology designs or designs that require isolation from the power bus during charging.

The Si4720CY is available in a 16-pin SOIC package and is rated for the commercial temperature range of - 25 °C to 85 °C.

FEATURES

- Solution for Bi-Directional Blocking
- 6 V to 30 V Operation
- Ground Referenced Logic Level Inputs
- Integrated Low $R_{DS(on)}$ MOSFET
- Level-Shifted Gate Drive with Internal MOSFET
- Two Independent Inputs
- Ultra Low Power Consumption in Off State (Leakage Current Only)
- Logic Supply Voltage is Not Required

FUNCTIONAL BLOCK DIAGRAM



Half a circuit shown here.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Limit	Unit
Voltage Referenced to GND V_S, V_D[a]			- 0.3 to 32	V
V_{SD}			- 0.3 to 30	
V_{IN1}, V_{IN2}			- 0.3 to 15	
V_{GS}			20	
Storage Temperature			- 55 to 150	°C
Power Dissipation[b]	t = 10 s		2.5	W
	t = Steady State		1.5	

Notes:
a. $V_{SD} \leq 30\ V_{DC}$.
b. Device mounted with all leads soldered to 1" x 1" FR4 with laminated copper PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Limit	Unit
V_S, V_D		6 to 30	V
V_{IN1}, V_{IN2}		0 to 13.2	
I_{DS}		0 to 6	A
Operating Temperature Range		- 25 to 85	°C
Junction Temperature		- 25 to 150	

This device has a maximum recommended operating junction temperature of 85 °C. This temperature limit is used for electrical specifications such as logic transition voltages only and is not a reliability limit. The device can be used with junction temperatures up to 150 °C if relaxed specifications can be tolerated, although limits for these specifications may not be given. Performance curves can be used to give an indication of specifications at higher temperatures, but are not guaranteed.

SPECIFICATIONS

Parameter		Symbol	Test Conditions Unless Otherwise Specified	Limits				Unit
				Temp.[a]	Min.[b]	Typ.[c]	Max.[b]	
On-Resistance		r_{DS}	V_S = 10 V, I_D = 1 A, V_{IN} = H	Room		0.0155	0.020	Ω
Leakage Current		$I_{DS(off)}$	V_{DS} = 10 V	Room			1	µA
Supply Current		$I_{S(off)}$	V_S = 21 V	Room			1	
		$I_{S(on)}$		Room		1.1	6	
Input Voltage Low		V_{INL}	V_S = 10 and V_S = 21	Full			1	V
Input Voltage High		V_{INH}		Full	2.5			
Input Leakage Current		I_{INH}	V_{IN} = 5 V	Full			5	µA
Turn-On Delay	IN to D or S	$t_{ON(IN)}$	V_S = 10 V, R_L = 5 Ω, Figure 1	Room	2.2	2.9	10	µs
Turn-Off Delay		$t_{OFF(IN)}$		Room		1.5	2.1	
Break-Before-Make[d]		t_{BBM}		Room		1.05		
Rise Time		t_{RISE}	V_S = 10 V, R_L = 5 Ω, Figure 1	Room		1.3	2.5	
Fall Time		t_{FALL}		Room		50	100	ns
Voltage Across pin 6 and 7		V_{GS}	V_S = 30	Room		10.2	18	V
Forward Diode		V_{SD}	I_D = - 1 A	Room			1.1	

Notes:
a. Room = 25 °C, full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production testing.

TIMING DIAGRAMS

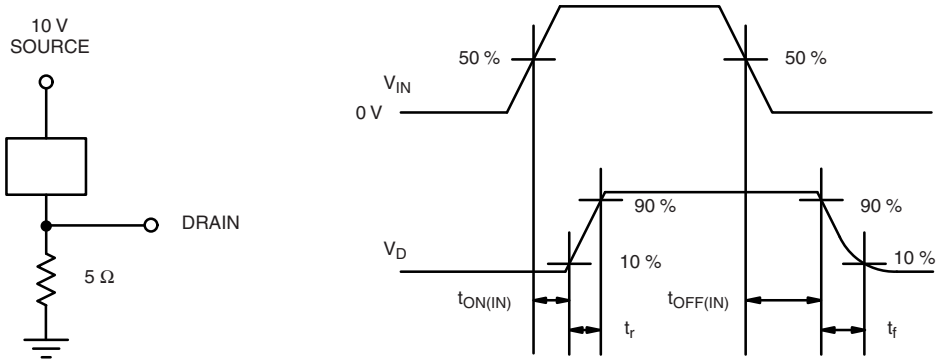
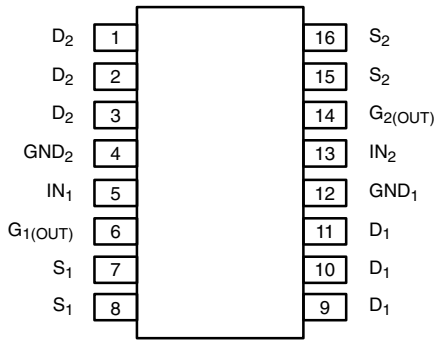


Figure 1.

PIN CONFIGURATION AND TRUTH			
V_{IN1}	V_{IN2}	Switch 1	Switch 2
0	0	Off	Off
0	1	Off	On
1	0	On	Off
1	1	On	On

SO-16

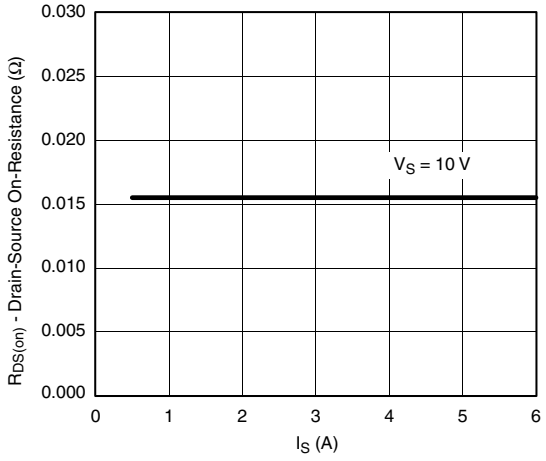


Top View

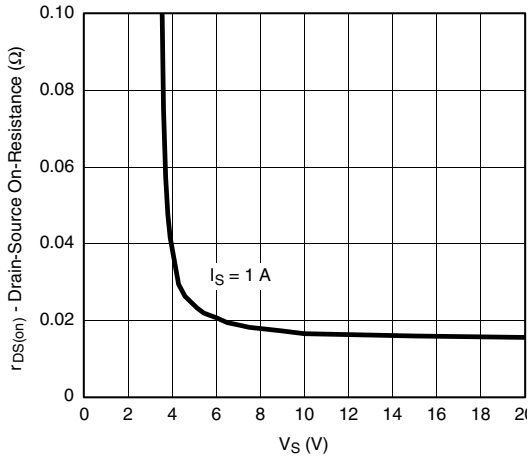
Order Number: Si4720CY

PIN DESCRIPTION (Subject to Change)		
Pin Number	**Symbol**	**Description**
1, 2, 3	D_2	Drain connection for MOSFET-2.
4, 12	GND	Ground
5	IN_1	Logic input, IN_1. High level turns on the switch.
6	$G_{1(OUT)}$	Gate output to MOSFET-1.
7, 8	S_1	Source connection for MOSFET-1.
9, 10, 11	D_1	Drain connection for MOSFET-1.
13	IN_2	Logic input, IN_2. High level turns on the switch.
14	$G_{2(OUT)}$	Gate output to MOSFET-2.
15, 16	S_2	Source connection for MOSFET-2.

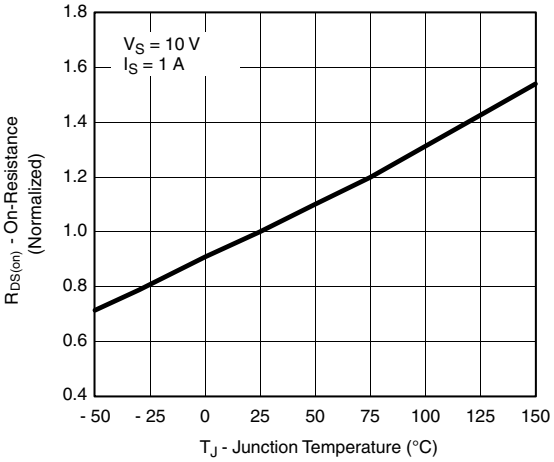
TYPICAL CHARACTERISTICS (25 °C unless noted)



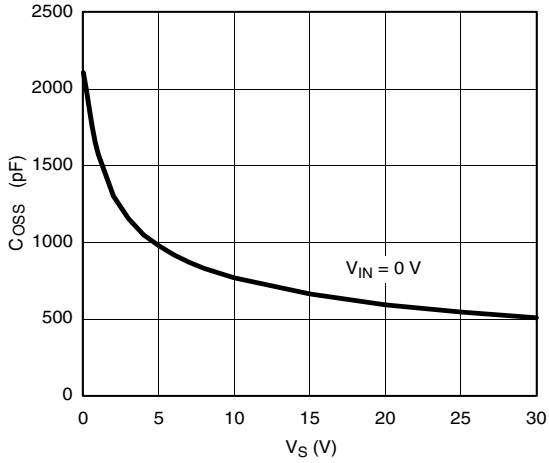
On-Resistance vs. Drain Current



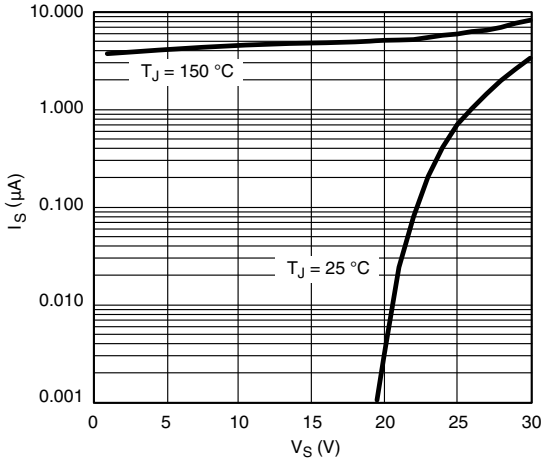
On-Resistance vs. Source Voltage



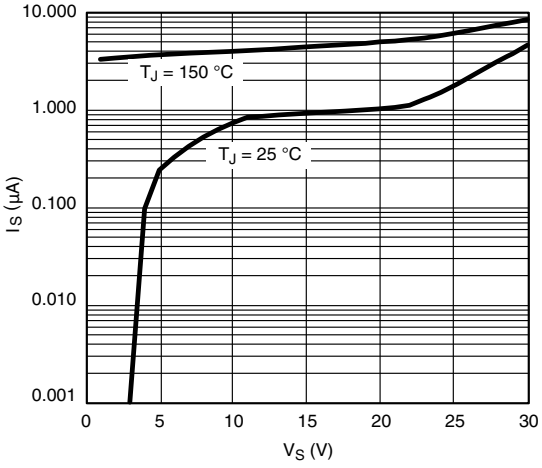
Normalized On-Resistance vs. Junction Temperature



Output Capacitance vs. Source Voltage

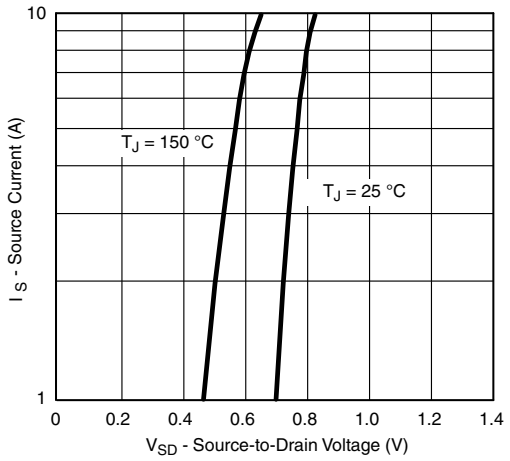


Off-Supply Current vs. Source Voltage

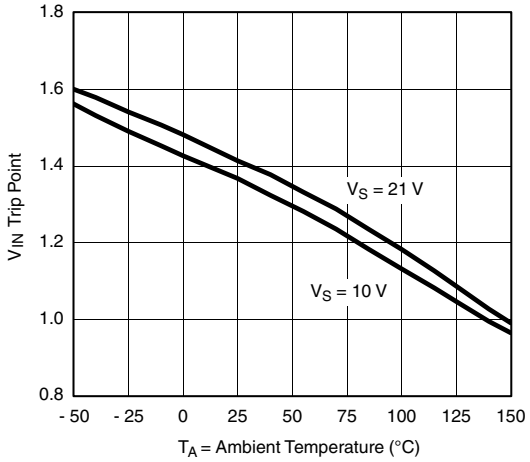


On-Supply Current vs. Source Voltage

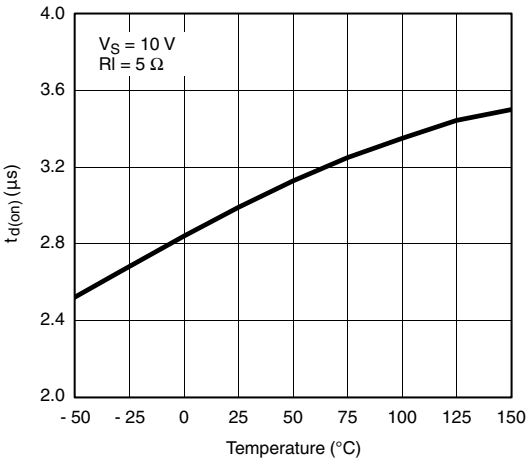
TYPICAL CHARACTERISTICS (25 °C unless noted)



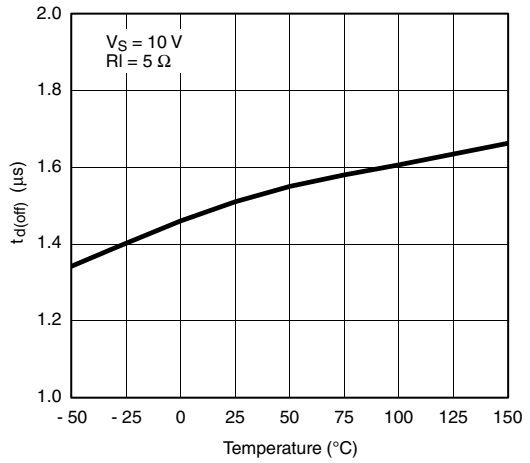
Drain-Source Diode Forward Voltage



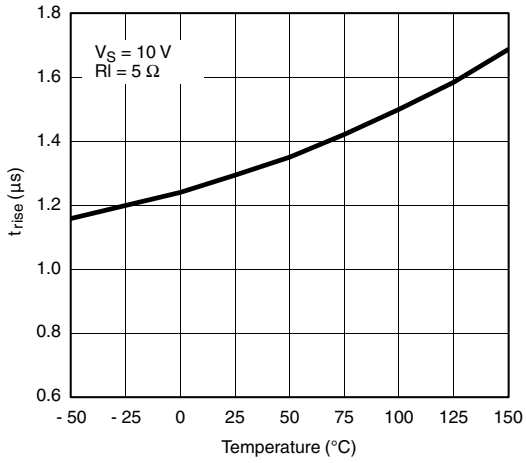
Input Voltage Trip Point vs. Temperature



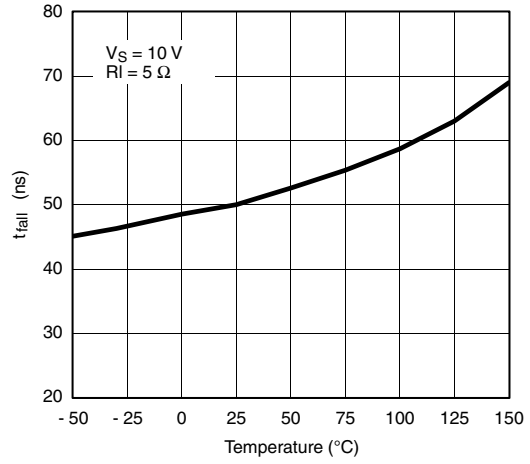
Turn-On Delay vs. Temperature



Turn-off Delay vs. Temperature

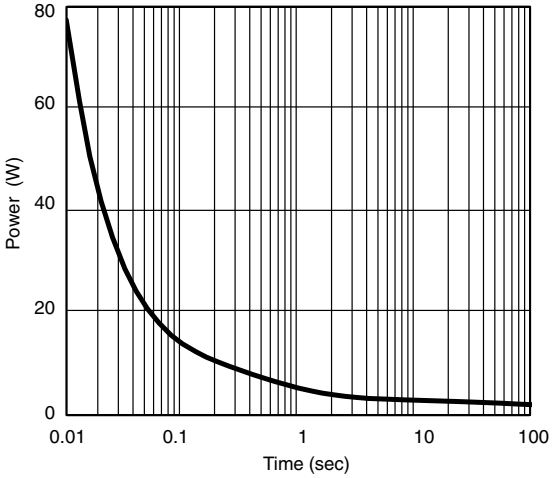


Rise Time vs. Temperature

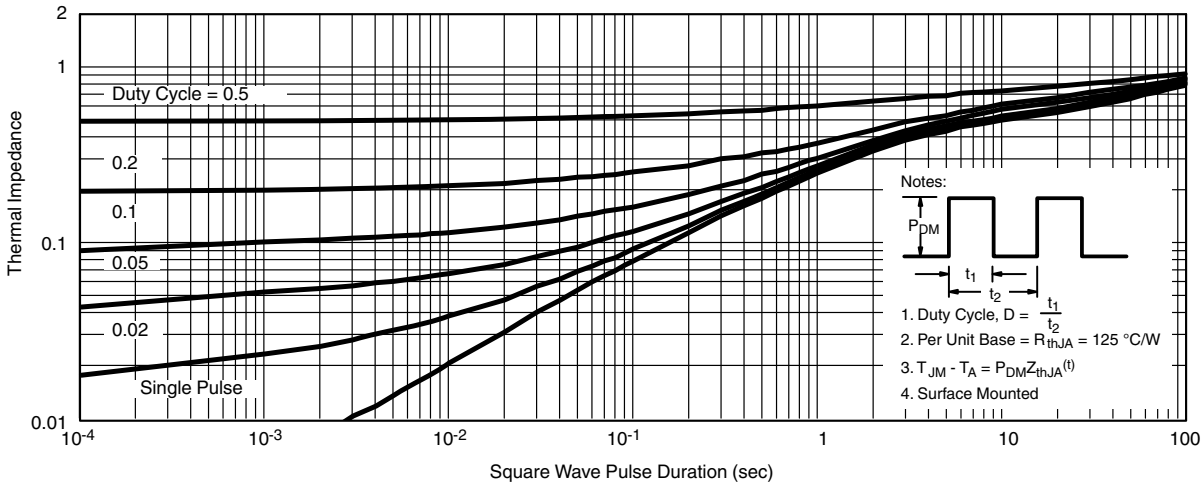


Fall Time vs. Temperature

TYPICAL CHARACTERISTICS (25 °C unless noted)



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

APPLICATION DRAWINGS

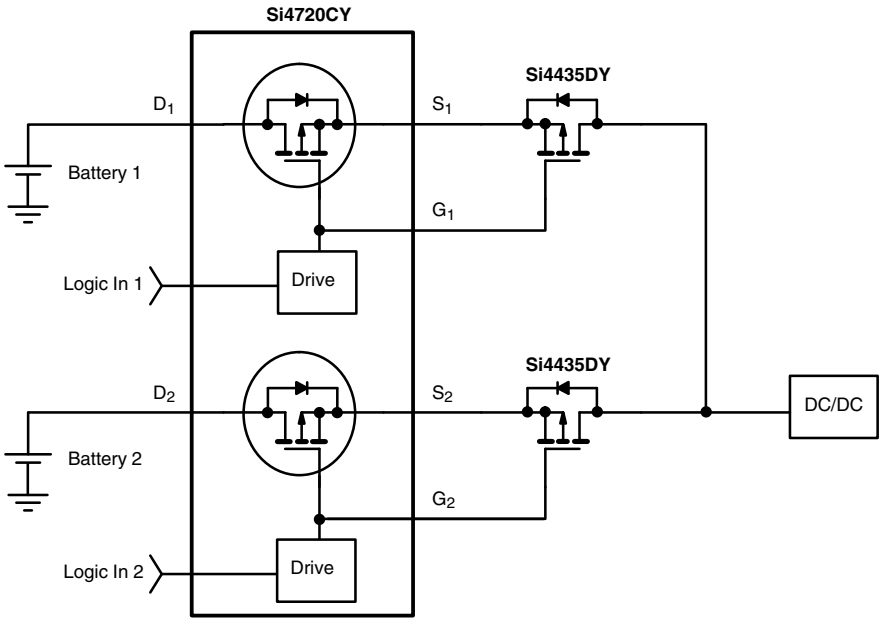


Figure 2.

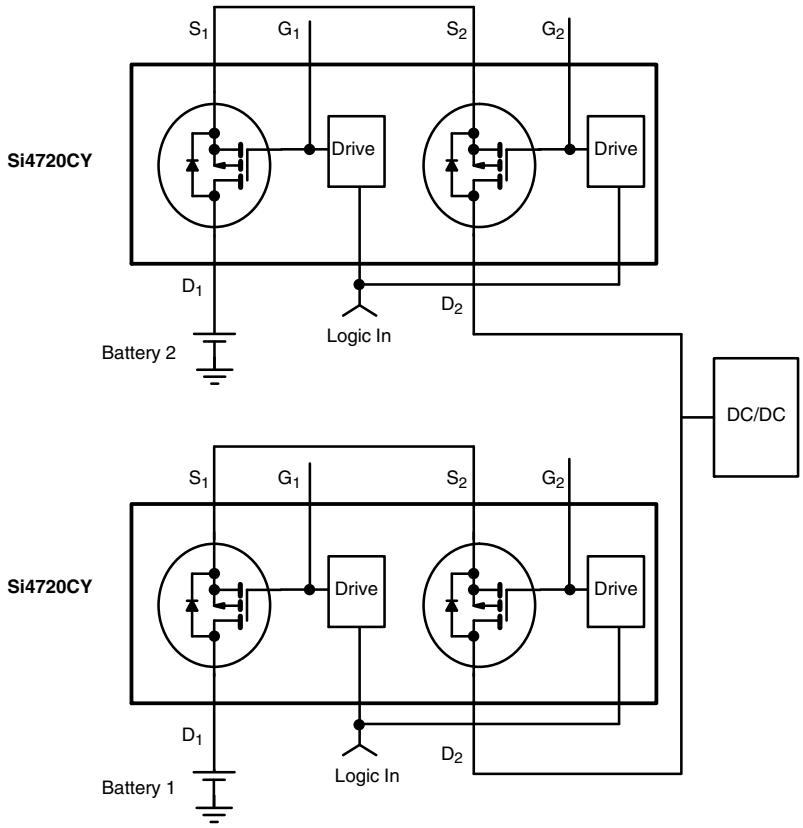


Figure 3.

APPLICATION DRAWINGS

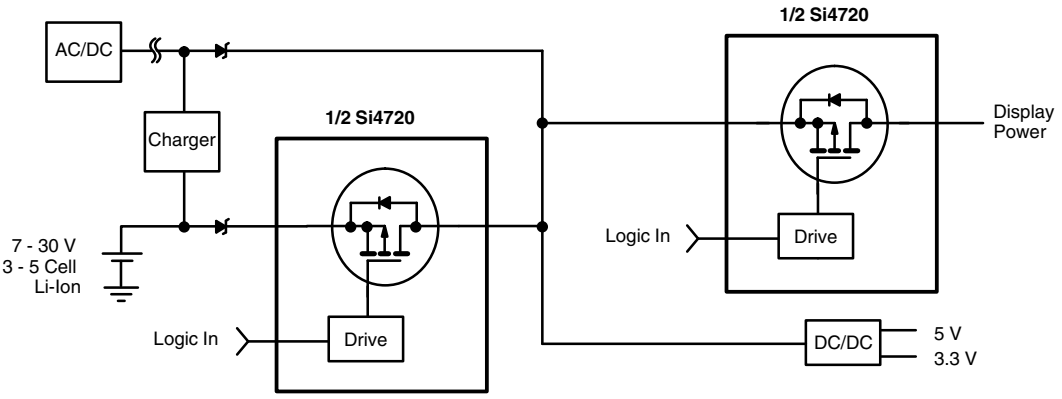


Figure 4. Low-Cost Laptop PC

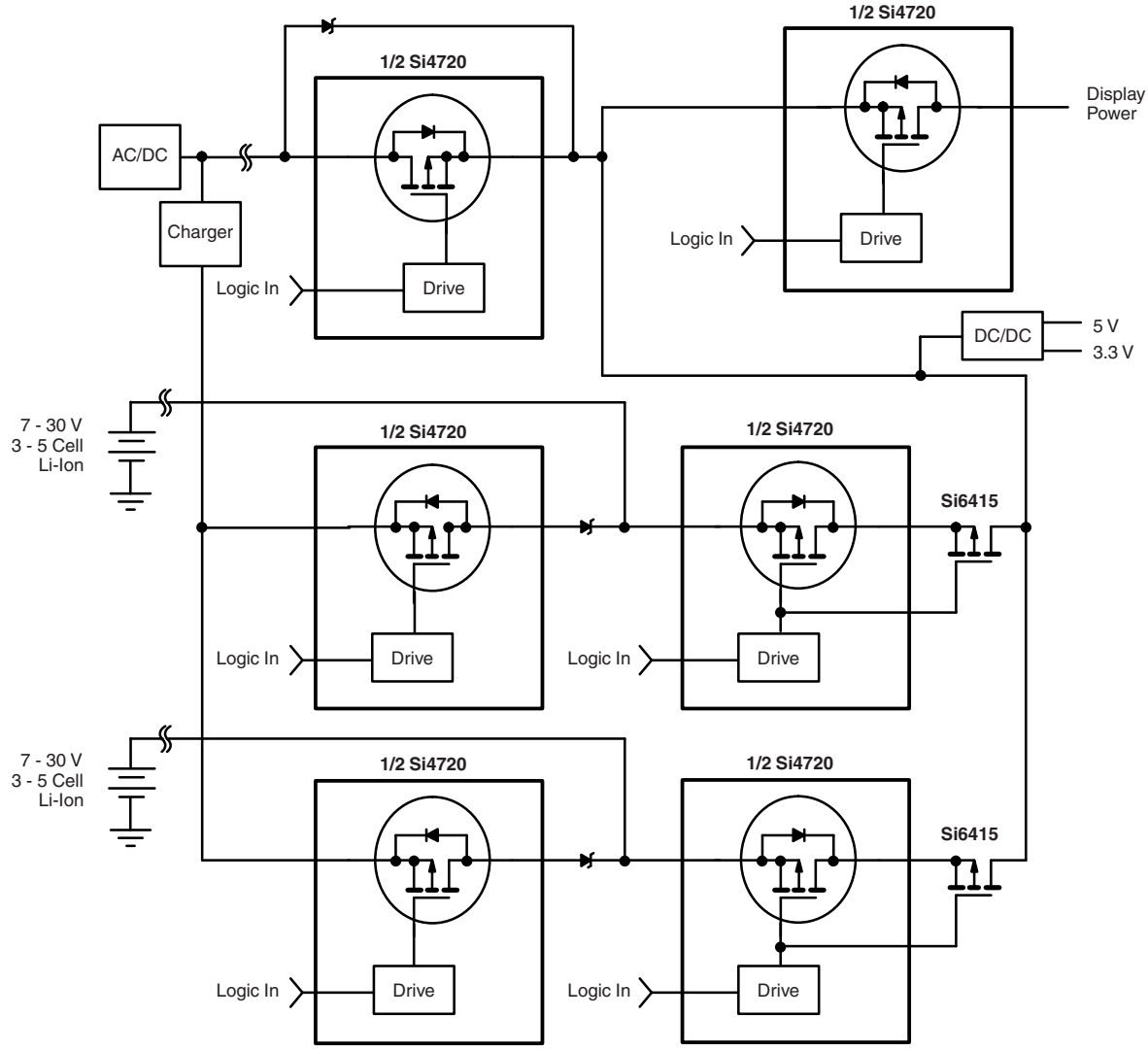


Figure 5. High-Performance Laptop PC

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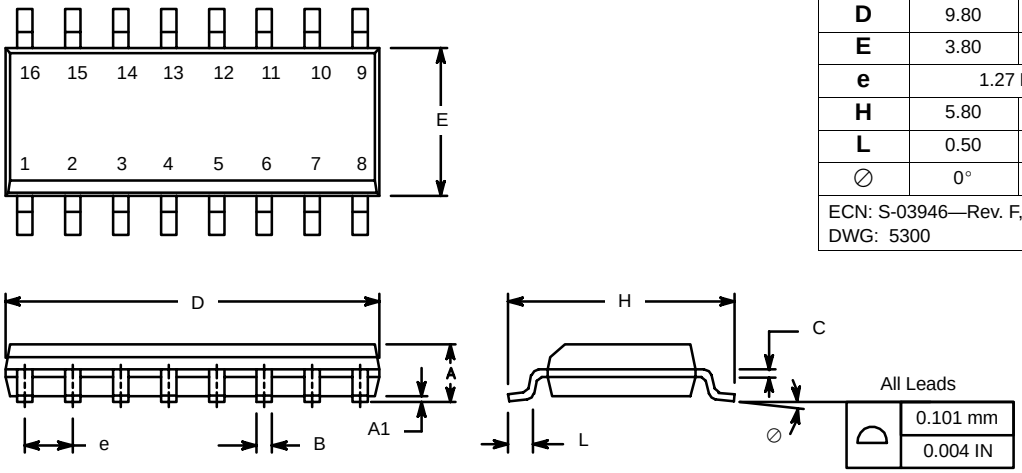
SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



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