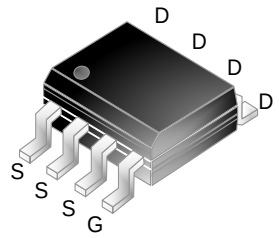
# WMS175N10LG2

## 100V N-Channel Enhancement Mode Power MOSFET

## Description

WMS175N10LG2 uses Wayon's 2nd generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

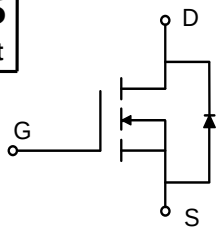



SOP-8L

## Features

- $V_{DS}$ = 100V, $I_D$ = 10A(Silicon Limited)
  $R_{DS(on)}$ < 18.5mΩ @ $V_{GS}$ = 10V
  $R_{DS(on)}$ < 26mΩ @ $V_{GS}$ = 4.5V
- Green Device Available
- 100% EAS Guaranteed
- Low Gate Charge
- High Speed Switching

RoHS compliant




## Applications

- DC/DC Converter
- Synchronous Rectifier

### Absolute Maximum Ratings

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current[1](Silicon Limited) | $T_A$=25℃ | $I_D$ | 10 | A |
| | $T_A$=100℃ | | 6.5 | |
| Pulsed Drain Current[2] | | $I_{DM}$ | 32 | A |
| Single Pulse Avalanche Energy[3] | | EAS | 51.2 | mJ |
| Avalanche Current | | $I_{AS}$ | 16 | A |
| Total Power Dissipation[4] | $T_A$=25℃ | $P_D$ | 3.1 | W |
| Operating Junction and Storage Temperature Range | | $T_J$ , $T_{STG}$ | -55 to 150 | °C |

### Thermal Characteristics

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance from Junction-to-Ambient[1] | $R_{\theta JA}$ | 40.3 | °C/W |

## Electrical Characteristics $T_c$ = 25°C, unless otherwise noted

| Parameter | | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | | |
| Drain-Source Breakdown Voltage | | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 100 | - | - | V |
| Gate-Body Leakage Current | | $I_{GSS}$ | $V_{DS}$ = 0V, $V_{GS}$ = ±20V | - | - | ±100 | nA |
| Zero Gate Voltage Drain Current | $T_J$=25℃ | $I_{DSS}$ | $V_{DS}$ = 100V, $V_{GS}$ = 0V | - | - | 1 | μA |
| | $T_J$=100℃ | | | - | - | 100 | |
| Gate-Threshold Voltage | | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 1.0 | - | 2.5 | V |
| Drain-Source on-Resistance[2] | | $R_{DS(on)}$ | $V_{GS}$ = 10V, $I_D$ = 8A | - | 15 | 18.5 | mΩ |
| | | | $V_{GS}$ = 4.5V, $I_D$ = 6A | - | 19.5 | 26 | |
| Forward Transconductance[2] | | $g_{fs}$ | $V_{DS}$ = 5V, $I_D$ = 15A | - | 38 | - | S |
| **Dynamic Characteristics** | | | | | | | |
| Input Capacitance | | $C_{iss}$ | $V_{DS}$ = 50V, $V_{GS}$ =0V, f =1MHz | - | 868 | - | pF |
| Output Capacitance | | $C_{oss}$ | | - | 172 | - | |
| Reverse Transfer Capacitance | | $C_{rss}$ | | - | 6 | - | |
| **Switching Characteristics** | | | | | | | |
| Gate Resistance | | $R_G$ | $V_{DS}$ = 0V, $V_{GS}$ =0V, f =1MHz | - | 1.25 | - | Ω |
| Total Gate Charge | | $Q_g$ | $V_{GS}$ = 4.5V, $V_{DS}$ = 50V, $I_D$= 15A | - | 6.2 | - | nC |
| Total Gate Charge | | $Q_g$ | $V_{GS}$ = 10V, $V_{DS}$ = 50V, $I_D$= 15A | - | 13.5 | - | |
| Gate-Source Charge | | $Q_{gs}$ | | - | 2.3 | - | |
| Gate-Drain Charge | | $Q_{gd}$ | | - | 2.3 | - | |
| Turn-on Delay Time | | $t_{d(on)}$ | $V_{GS}$ =10V, $V_{DS}$ = 50V, $R_G$ = 10Ω, $I_D$= 15A | - | 4.5 | - | nS |
| Rise Time | | $t_r$ | | - | 2.3 | - | |
| Turn-off Delay Time | | $t_{d(off)}$ | | - | 10 | - | |
| Fall Time | | $t_f$ | | - | 2.3 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Diode Forward Voltage[2] | | $V_{SD}$ | $I_S$ = 1A, $V_{GS}$ = 0V | - | - | 1 | V |
| Continuous Source Current[1,5] | | $I_S$ | $V_G$=$V_D$=0V , Force Current | - | - | 10 | A |
| Body Diode Reverse Recovery Time | | $t_{rr}$ | $V_R$ = 50V ,$I_F$ = 15A, dI/dt = 500A/μs | - | 24 | - | nS |
| Body Diode Reverse Recovery Charge | | $Q_{rr}$ | | - | 95 | - | nC |

Notes:

1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is $V_{DD}$=25V, $V_{GS}$=10V, L=0.4mH, $I_{AS}$=16A

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

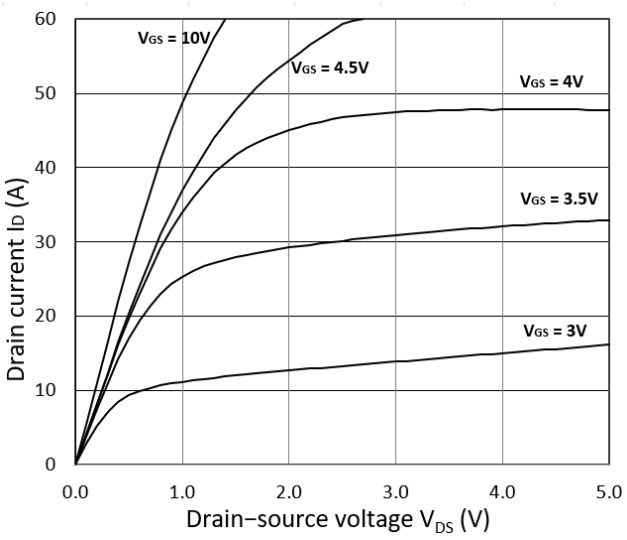



Figure 1. Output Characteristics

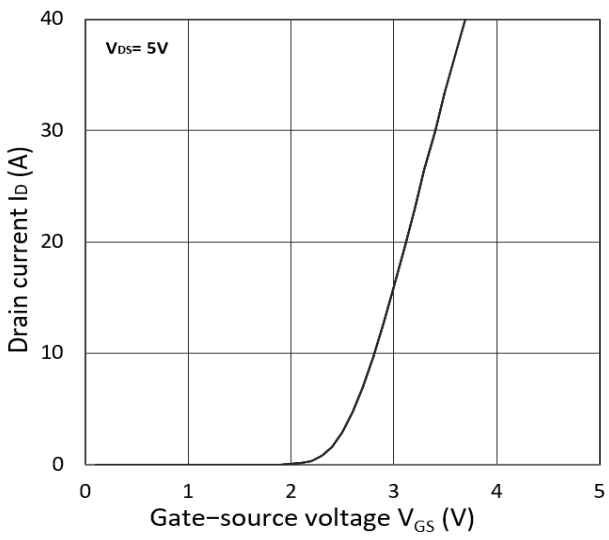



Figure 2. Transfer Characteristics

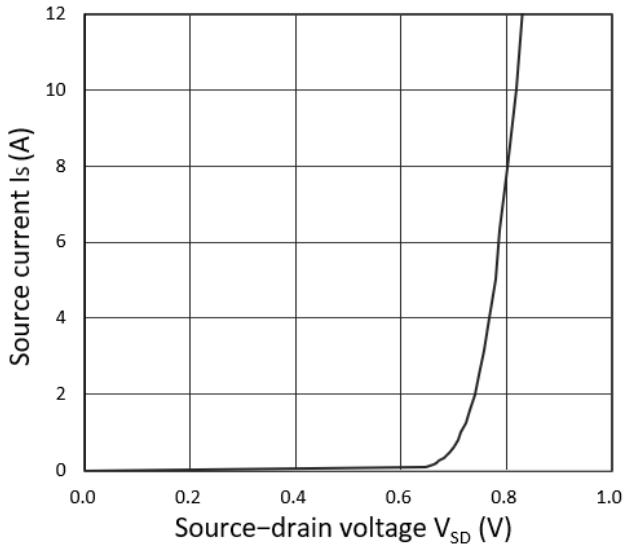



Figure 3. Forward Characteristics of Reverse

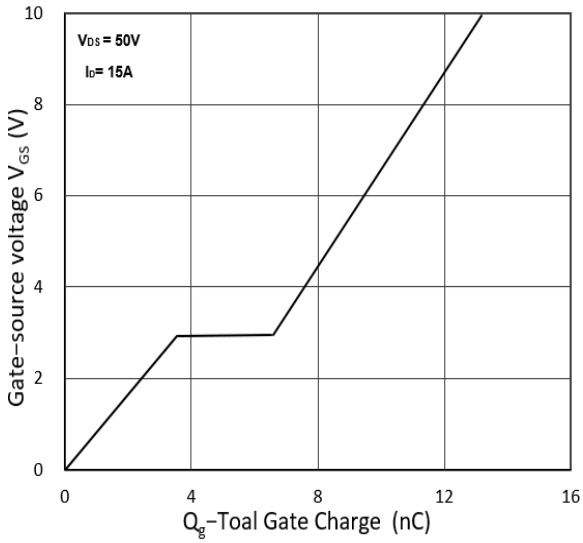



Figure 4. Gate Charge Characteristics

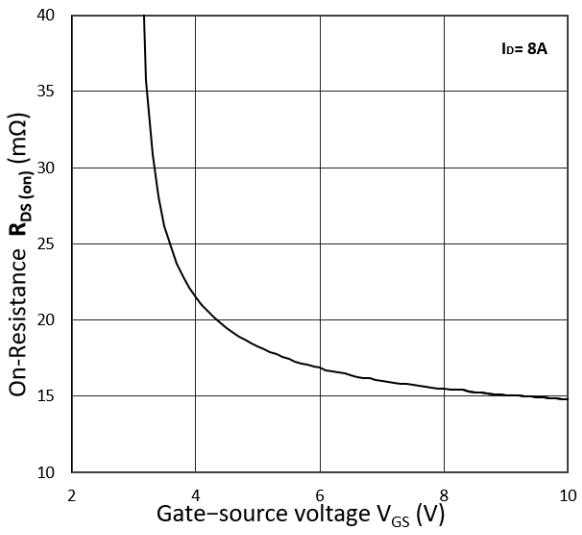



Figure 5. $R_{DS(ON)}$ vs. $V_{GS}$

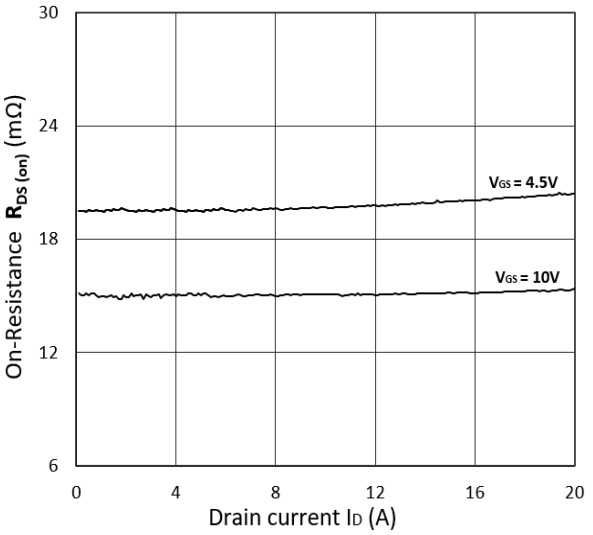



Figure 6. $R_{DS(ON)}$ vs. $I_D$

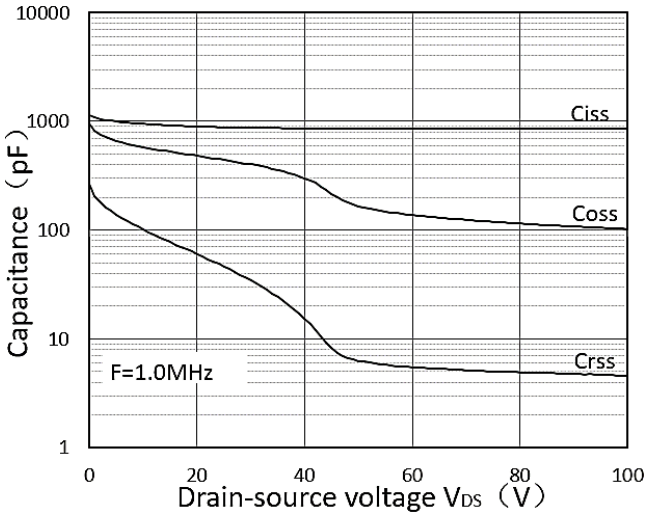



Figure 7. Capacitance Characteristics

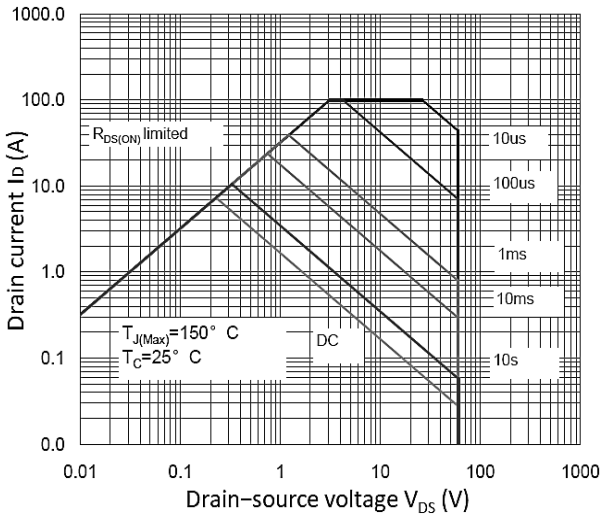



Figure 8. Safe Operating Area

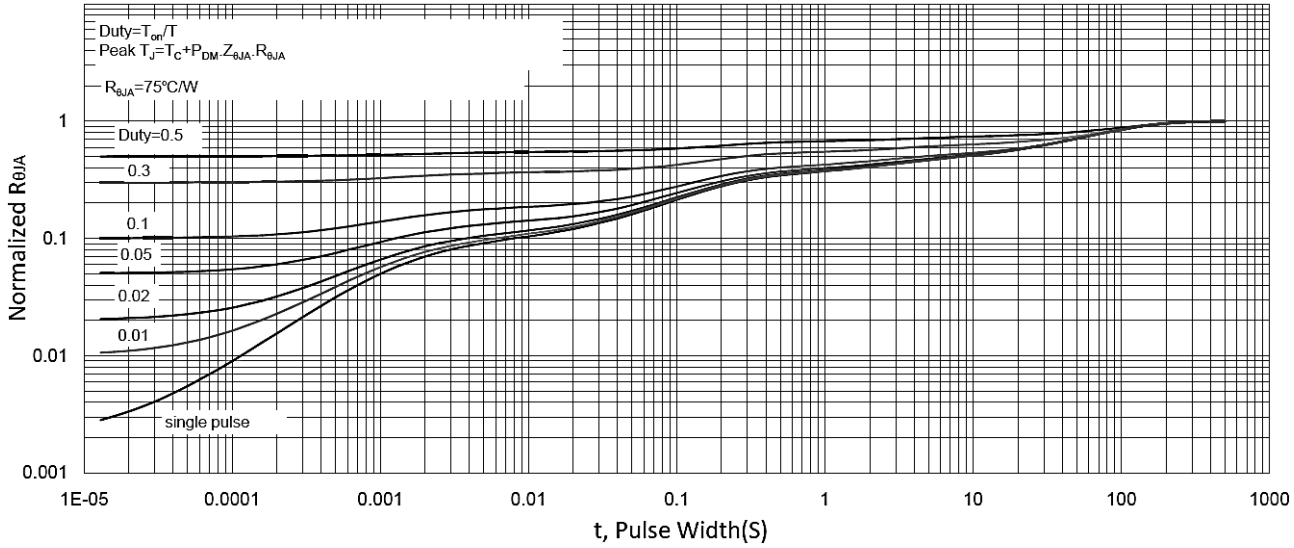



Figure 9. Normalized Maximum Transient Thermal Impedance

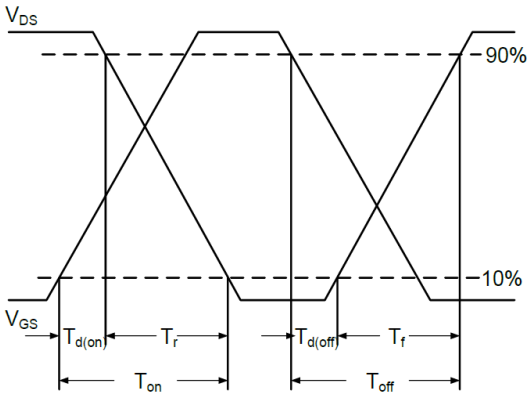



Figure 10. Switching Time Waveform

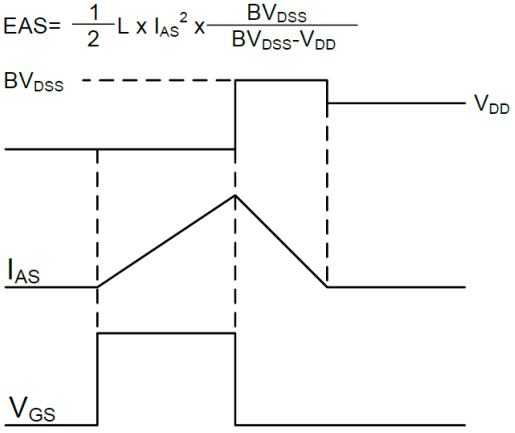
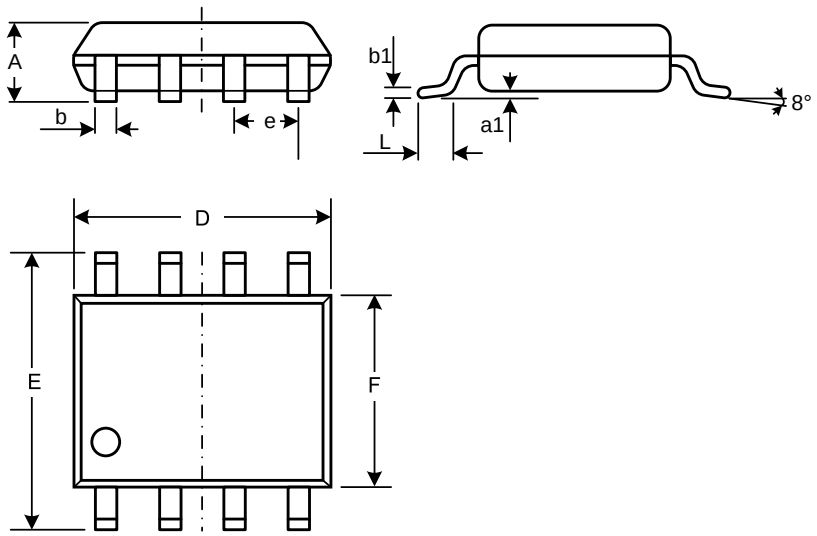



Figure 11. Unclamped Inductive Switching Waveform

**Mechanical Dimensions for SOP-8L**



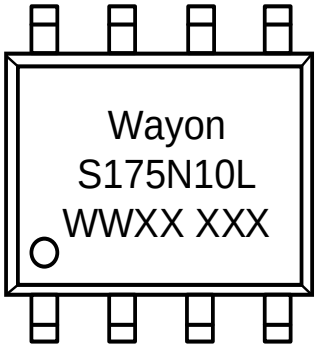

COMMON DIMENSIONS

| SYMBOL | MM | |
|---|---|---|
| | MIN | MAX |
| A | 1.23 | 1.75 |
| a1 | 0.05 | 0.25 |
| b | 0.31 | 0.51 |
| b1 | 0.16 | 0.25 |
| D | 4.70 | 5.15 |
| E | 5.75 | 6.25 |
| e | 1.07 | 1.47 |
| F | 3.70 | 4.10 |
| L | 0.4 | 1.27 |

## Ordering Information

| Part | Package | Marking | Packing method |
|---|---|---|---|
| WMS175N10LG2 | SOP-8L | S175N10L | Tape and Reel |

## Marking Information




S175N10L = Device code

WWXX XXX= Date code

## Contact Information

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