High-speed USB converter chip CH347

Datasheet
Version: 1A
http://wch.cn

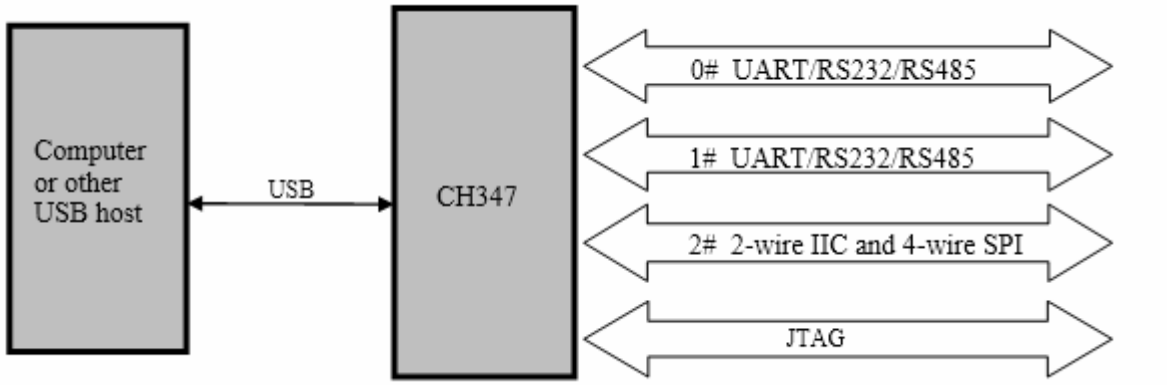
1. Introduction

CH347 is a high-speed USB bus converter chip that provides UART, I2C and SPI synchronous serial ports and JTAG interface through USB bus.

In UART mode, CH347 provides two high-speed serial ports, supports RS485 UART transceiver enable control, hardware flow control, and common MODEM signals, used to extend serial ports for computer, upgrade directly from normal serial device or MCU to USB bus.

In synchronous serial interface mode, CH347 provides one 2-line I2C interface (SCL line, SDA line) and one 4-line SPI interface(SCS line, SCK/CLK line, MISO/SDI/DIN line, MOSI/SDO/DOUT line) to extend 2-line or 4-line synchronous serial interface for computer to operate EEPROM, FLASH, sensors, etc.

In JTAG mode, CH347 provides a JTAG interface that supports either a 4-line or 5-line interface (TMS, TCK, TDI line, TDO line, and TRST line) for extending JTAG interface for computer to operate devices such as CPU, DSP, FPGA, and CPLD.



2. Features

2.1. Introduction

- 480Mbps high-speed USB device interface, peripheral components only need crystal oscillator and capacitor.
- Built-in EEPROM with configurable parameters such as operating mode, chip VID, PID, maximum current value, manufacturer and product information string.
- Supports only 3.3V power supply.
- RoHS compliant TSSOP-20 lead free package.
- Multiple working modes, suitable for high-speed USB converter applications.
- Functional customization can be carried out according to industry batch requirements.

2.2. UART

- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating system.
- Hardware full duplex UART interface, built-in transmit-receive buffer, supports communication baud rate from 1200bps to 9Mbps.
- UART supports 8 data bits, supports odd, even, none parity, and 1 or 2 stop bits.
- Each UART has a built-in 12K bytes receiving FIFO and 4K bytes sending FIFO.
- Supports common MODEM contact signals RTS, DTR, DCD, RI, DSR and CTS.
- Support CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW, used for controlling RS485 to transmit-receive switch.
- Supports up to 8 channels of GPIO input and output function.
- Support RS232, RS485, RS422 interface, etc. through external voltage converter chip.

2.3. I2C synchronous serial interface

- Works in Host/Master Host mode.
- 2 signal lines, SCL and SDA, supports 4 transmission speeds.
- With the cooperation of computer API, flexible operation of 2-line interface A/D, D/A, EEPROM and sensor components.

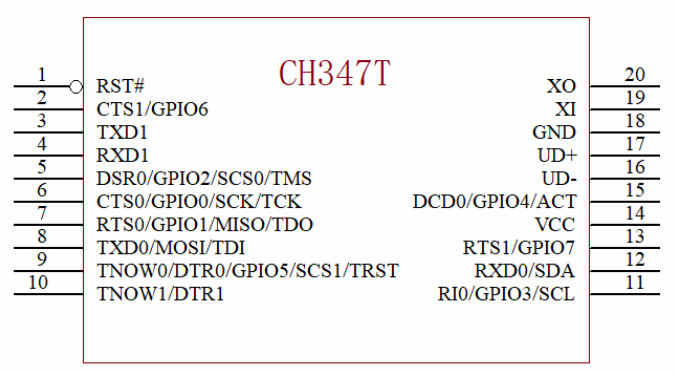
2.4. SPI synchronizes serial interface

- Works in Host/Master Host mode.
- Provide SCS, SCK/CLK, MISO/SDI/DIN, MOSI/SDO/DOUT four signal lines.
- Supports 2 chip select signal lines and can operate two SPI interface devices by time-sharing.
- Supports 8 bit /16 bit data structure, supports MSB and LSB transmission.
- Supports SPI mode 0/1/2/3, and supports transmission frequency configuration up to 36MHz.
- Supports hardware DMA sending and receiving.
- With the cooperation of computer API, flexible operation of FLASH, MCU, sensor and other devices with 4-line interface.

2.5. JTAG interface

- Works in Host/Master host mode.
- JTAG provides TMS, TCK, TDI, TDO, and TRST lines (optional).
- Support high-speed USB data transfer.
- With the cooperation of computer API, it can operate CPU, DSP, FPGA, CPLD, MCU and other devices flexibly.

3. Packages



Package	Body size		Lead pitch		Description	Part No.
TSSOP-20	4.4mm	173mil	0.65mm	25mil	Thin small 20 pin patch	CH347T

Note：USB transceiver of CH347 is designed according to the built-in design of USB2.0. UD+ and UD- pins cannot be connected in series with resistors, otherwise the signal quality will be affected.

4. Pin definitions

4.1. General descriptions

CH347 has multiple working modes, and the function and definition of the same pin in different working modes may be different. CH347 automatically configures the operating mode by detecting the configuration pin status during power-on reset or external reset.

Note: FT indicates pin withstands 5V when used as an input.

4.2. Standard common pins

Pin No.	Pin Name	Pin Type	Pin Description
14	VCC	POWER	Power supply voltage input, requires an external decoupling capacitor
18	GND	POWER	Ground, connected to ground of USB bus directly
1	RST#	IN	Input of external reset, active low, built-in pull-up resistor
17	UD+	USB signal	Connect to USB D+ Signal directly, do not series resistor
16	UD-	USB signal	Connect to USB D- Signal directly, do not series resistor
19	XI	IN	Input of crystal oscillator
20	XO	OUT	Inverted output of crystal oscillator

4.3. Working mode configures pins

Pin No.	Pin Name	Pin Type	Pin Description
10	DTR1/TNOW1	Input during reset (FT)	MODE0 configuration pin 0 for working mode when the chip is reset. Used with MODE1 pin, built-in pull-up resistor
13	RTS1/GPIO7	Input during reset (FT)	MODE1 configuration pin 1 for working mode when the chip is reset. Used with MODE0 pin, built-in pull-up resistor

4.4. Working mode 0 pins

Pin No.	Pin Name	Pin Type	Pin Description
8	TXD0	OUT	UART0 transmit asynchronous data output, idle state is high level
12	RXD0	IN(FT)	UART0 receive asynchronous data input, integrated pull-up resistor
3	TXD1	OUT	UART1 transmit asynchronous data output, idle state is high level
4	RXD1	IN(FT)	UART1 receive asynchronous data input, integrated pull-up resistor
9	DTR0/TNOW0 /GPIO5	OUT	MODEM output signal for UART0, data terminal ready, active low; RS485 transmit and receive control of UART0; General purpose GPIO5 for IO port input or output. During power-on, if DTR0 detects an external pull-down resistor, DTR0 and DTR1 switch to TNOW0 and TNOW1 respectively
10	DTR1/TNOW1	OUT	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control of UART1
6	CTS0/GPIO0	IN(FT)	MODEM input signal for UART0, clear to send, active low; General GPIO0 for IO port input or output

7	RTS0/GPIO1	OUT	MODEM output signal of UART0, request to send, active low; General GPIO1 for IO port input or output. During power-on, if RTS0 detects an external pull-down resistor, disable the configuration parameters in the internal EEPROM and enable the default parameters delivered with the chip
2	CTS1/GPIO6	IN(FT)	MODEM input signal of UART1, clear to send, active low; General GPIO6 for IO port input or output
13	RTS1/GPIO7	OUT	MODEM output signal of UART1, request to send, active low; General GPIO7 for IO port input or output
11	RI0/GPIO3	IN(FT)	MODEM input signal for UART0, ring indicator, active low; General GPIO3 for IO port input or output
15	DCD0/GPIO4	IN(FT)	MODEM input signal for UART0, data carrier detect, active low; General GPIO4 for IO port input or output
5	DSR0/GPIO2	IN(FT)	MODEM input signal of UART0, data set ready, active low; General GPIO2 for IO port input or output

4.5. Working mode 1/2 pins

Pin No.	Pin Name	Pin Type	Pin Description
3	TXD1	OUT	UART1 transmit asynchronous data output, idle state is high level
4	RXD1	IN(FT)	UART1 receive asynchronous data input, integrated pull-up resistor
10	DTR1/TNOW1	OUT	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control of UART1
2	CTS1	IN(FT)	MODEM input signal of UART1, clear to send, active low
13	RTS1	OUT	MODEM output signal of UART1, requests to sent, active low
7	MISO	IN(FT)	4-line serial port data input, alias DIN or SDI,

			built-in pull-up resistor
8	MOSI	OUT	4-line serial port data output, alias DOUT or SDO
6	SCK	OUT	4-line serial port clock output, alias DCK
5	SCS0	OUT	Chip selection output of 4-line serial port is 0
9	SCS1	OUT	Chip selection output of 4-line serial port is 1
12	SDA	OUT IN(FT)	2-line serial port data input and output, built-in pull-up resistance
11	SCL	OUT	2-line serial port clock output, built-in pull-up resistor
15	ACT	OUT	USB configuration completed status output pin, active low

4.6. Working mode 3 pins

Pin No.	Pin Name	Pin Type	Pin Description
3	TXD1	OUT	UART1 transmit asynchronous data output, idle state is high level
4	RXD1	IN(FT)	UART1 receive asynchronous data input, integrated pull-up resistor
10	DTR1/TNOW1	OUT	UART1 MODEM output signal, data terminal ready, active low; RS485 transmit and receive control of UART1
2	CTS1	IN(FT)	UART1 MODEM input signal, clear to send, active low
13	RTS1	OUT	MODEM output signal of UART1, requests to sent, active low
7	TDI	OUT	JTAG interface data output
8	TDO	IN(FT)	JTAG interface data input, built-in pull-up resistor
6	TCK	OUT	Clock output of JTAG interface
9	TRST	OUT	Reset output of JTAG interface
5	TMS	OUT	Mode selection of JTAG interface
11, 12	GPIO	IN/OUT	General GPIO, used for IO port input or output
15	ACT	OUT	USB configuration completed status output pin, active low

5. Function descriptions

5.1. General descriptions

CH347 is a high-speed USB bus converter chip that provides asynchronous serial port, common 2-line IIC and 4-line SPI synchronous serial port, JTAG interface, etc.

VCC of CH347 is power input, which requires 3.3V power supply voltage. Power supply pin VCC should be respectively connected to an external power decoupling capacitor of about 0.1uF.

CH347 chip has a built-in power-on reset circuit. When the chip is operating, it needs to provide an external 8MHz clock signal to the XI pin. The clock signal can be generated by the built-in inverter of CH347

through crystal frequency stabilization oscillation. The peripheral circuit needs to connect an 8MHz crystal between the XI and XO pins, and the both pins connect to the ground with an oscillation capacitor of about 22pF.

CH347 has built-in all peripheral circuits required by the USB bus, including the embedded USB controller and USB-PHY, the series matching resistor of the USB signal line, and the 1.5K pull-up resistor required by the Device. The UD+ and UD- pins can be directly connected to USB bus.

5.2. Working mode configuration

When CH347 is reset, the chip detects the level status of DTR1 (PIN10) and RTS1 (PIN13) pins. Chip working modes and their switching functions are described in the following table.

Working Mode	DTR1 and RTS1 Pin Status	Chip Function	Default Product ID
Mode 0	DTR1 floating or high level, RTS1 floating or high level	USB to high-speed dual serial ports. UART 0 supports full MODEM signals, UART 1 supports partial MODEM signals	55DAH
Mode 1	DTR1 floating or high, RTS1 pulled down low	Manufacturer's driver mode three-in-one: USB to high-speed single serial port + USB to 2-line I2C + USB to 4-line SPI	55DBH
Mode 2	DTR1 pulls down low level, RTS1 floating or high	HID Free drive mode three-in-one: USB to high-speed single serial port + USB to 2-line I2C + USB to 4-line SPI	55DCH
Mode 3	DTR1 pulls down low, RTS1 pulls down low	two-in-one: USB to high-speed single serial port + USB to JTAG port	55DDH

Working Mode 0: USB to high-speed dual serial ports, which is identified as two standard USB serial ports on the computer, suitable for the simultaneous use of double serial ports. UART0 supports full MODEM signals, and UART1 supports partial MODEM signals. Both serial ports support hardware flow control and RS485 serial port sending and receiving enable control.

Working Mode 1: Manufacturer driver mode three-in-one, USB to high-speed single serial port, USB to 2-line I2C and USB to 4-line SPI synchronous serial ports. Identified as a standard USB serial port and a custom interface for 2-line and 4-line synchronous serial interface communication on the computer, suitable for the simultaneous use of serial port and 2-line or 4-line synchronous serial interface requirements. UART1 supports partial MODEM signals, hardware flow control, and RS485 serial port sending and receiving enable control. 4-line synchronous serial interface supports configurations such as mode, data bits, and data sequence.

Working Mode 2: HID no-install driver mode three-in-one, USB to high-speed single serial port, USB to 2-line I2C and USB to 4-line SPI synchronous serial ports. On the computer, it is recognized as a class composite device with two customized HID interfaces (interface 0 is used for serial port data upload and down, and interface 1 is used for 2-line and 4-line synchronous serial interface communication). It is suitable for the simultaneous use of serial port and 2-line or 4-line synchronous serial interface, and it is not

convenient to install the manufacturer's driver. UART1 supports partial MODEM signals, hardware flow control, and RS485 serial port sending and receiving enable control. 4-line synchronous serial port supports mode (Mode 0/1/2/3), data bits (8-bit/16-bit), and data sequence (MSB/LSB).

Working Mode 3:Two-in-1, USB-to-high-speed single serial port and USB to JTAG interface. It can be identified as one standard USB serial port and one JTAG interface on the computer. It is suitable for using serial port and JTAG interface at the same time.

5.3. UART

CH347 provides one or two serial ports. Each UART contains TXD, RXD, CTS, RTS, and DTR pin, etc. UART0 supports all MODEM signals, and UART1 supports some MODEM signal lines.

In UART mode, CH347 contains: data transfer pins, MODEM interfaces signal pins and assistant pins.

Data transfer pins contain: TXD0, TXD1 and RXD0, RXD1. When UART input is idle, RXDx is high when UART transmission is idle. TXDx is high when UART reception is idle.

MODEM interface signal pins and RS485 transmit and receive control pins: CTS0, RTS0, DTR0, CTS1, RTS1, and DTR1.

UART of CH347 has intergrated separate transmit-receive buffer, which supports simplex, half-duplex or full-duplex asynchronous serial communication.

Serial data of CH347 contains 1 low-level start bit, 8 data bits, 1 /2 high level stop bits, and none/odd /even parity. Supports common baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5m, 2M, 3M, 4M, 5M, 6M, 7M, 8M, 9M, etc.

Both UART on CH347 supports CTSx and RTSx hardware automatic flow control. This function is disabled by default and can be enabled by VCP driver. If enabled, UART continues to send the next packet of data only when CTSx pin input is detected to be valid (active low), otherwise UART transmission is paused; UART automatically invalidates RTSx pin (active low) when the receive buffer is empty, invalidates RTSx pin until the receive buffer is nearly full, and then invalidates RTSx pin again when buffer is empty. With hardware automatic rate control, you can connect your CTSx pins to RTSx pins of the other side and your RTSx pins to CTSx pins of the other side.

The allowable baud rate error of CH347 UART receiving signal is less than 2%, the baud rate error of UART transmitting signal is less than 1%.

In Windows OS, install VCP vendor driver that supports high-speed communication. It can emulate serial port. So the mostly original serial applications are totally compatible, without any modification.

CH347 supports up to 8 channels of GPIO input/ output control funcation.

CH347 can be used to upgrade original UART peripherals, or expand extra serial ports for computer via USB bus. Through external level shifting chip provides RS232, RS485, RS422 and other interface can be further.

5.4. I2C synchronous serial interface

I2C/IIC synchronous serial interface of CH347 works in Host/Master mode, including SCL and SDA signal lines. SCL is used for unidirectional output synchronous clock, open leakage output and built-in pull-up

resistance, SDA is used for bidirectional data input and output, open-drain output and input and built-in pull-up resistance.

The basic operation elements of an I2C interface include: start bits, stop bits, bit outputs, and bit input.

The starting bit is defined as the falling edge of SCL output when SDA is at high current level.

Stop bits is defined as the rising edge of SCL output when SDA is at high current level.

Bit output is defined as when SCL is low, SDA outputs bit data, and then SCL outputs high level pulse.

Bit input is defined as the input of bit data from SDA before falling edge when SCL outputs a high level pulse.

I2C interface of CH347 supports four transmission speeds and can flexibly operate 2-line A/D, D/A, EEPROM and sensor components with the cooperation of computer API.

5.5. SPI synchronizes serial interface

4-line SPI synchronous serial interface of CH347 works in Host/Master mode, including four signal lines SCSx, SCK(CLK), MISO(SDI/DIN) and MOSI(SDO/DOUT). SCSx includes SCS0 and SCS1, which can operate two SPI interface devices in time-sharing mode. Support 8-bit / 16-bit data structure, support MSB and LSB transmission, support SPI mode 0/1/2/3, support transmission frequency configuration, etc. Built-in hardware DMA, batch data can be quickly sent and read. With the cooperation of computer API, flexible operation of FLASH, MCU, sensor and other devices with 4-line interface.

5.6. JTAG interface

JTAG interface of CH347 works in Host/Master mode. JTAG interface consists of five signal lines: TMS, TCK, TDI, TDO, and TRST. TRST is an optional signal line. Supports the fast mode and bit-bang mode of user-defined protocols, transmission rate up to 18Mbit/S.

Provide computer USB high-speed driver and USB to JTAG TAP function library, support secondary development and 1.8V, 2.5V interface level of the single chip scheme, used to build customized USB to high-speed JTAG debugger, FPGA downloader, CPU programmer and other products.

5.7. Chip parameter configuration

In larger batch applications, vendor identification code (VID) and product identification code (PID) of CH347 and product information can be customized.

In less batch applications, parameters can be configured by built-in EEPROM. After installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, it can be flexibly configured the identification code (VID), product identification code (PID), maximum current value, BCD version number, manufacture information and product information string and other descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

(critical state or exceeding maximum can cause chip to not work or even be damaged.)

Symbol	Parameter Description	Min.	Max.	Unit

TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-40	125	℃
VCC	Power supply voltage (VCC connects to power, GND to ground)	-0.3	4.0	V
VUSB	USB signal voltage	-0.5	3.8	V
VIO5	Withstand input voltage on 5V pins	-0.5	5.6	V
VIO3	Input voltage on other pins	-0.5	VCC+0.3	V

6.2. Electrical characteristics

(Test conditions: TA=25℃, VCC=3.3V, exclude pins connected to USB bus.)

Symbol	Parameter Description	Min.	Typ.	Max.	Unit
VCC	Power supply voltage (VCC power supply, GND connects to ground)	3.0	3.3	3.6	V
ICC	Power supply current when the chip is working normally	28	38	50	mA
ISLP	Suspending USB supply current	180	260	350	uA
VIL	Low level input voltage	0		0.8	V
VIH3	Does not tolerate high level input voltage of 5V pins	2.0		VCC	V
VIH5	Tolerate high level input voltage of 5V pins	2.0		5.0	V
VOL	Output low voltage, single pin suction 8mA current			0.4	V
VOH	Output high level, single pin output 8mA current	VCC-0.4			V
RPU	Built-in pull-up equivalent resistance	30	40	60	KΩ
VPOR	Threshold voltage for power-on/power-off reset	1.9	2.2	2.5	V
VESD	ESD electrostatic withstand voltage (human body model, non-contact)	4			KV

6.3. Timing parameters

(Test conditions: TA=25℃, VCC= 3.3V.)

Symbol	Parameter Description	Min.	Typ.	Max.	Unit
TRSTD	Reset delay after power on or external reset input	15	28	40	mS
TSUSP	Check the USB automatic suspension time	3	5	9	mS
TWAKE	Chip post-sleep wake completion time	0.3	0.5	2	mS

7. Applications

7.1. USB to dual UART

The figure below is the reference circuit diagram of USB-to-dual-channel high-speed TTL serial port realized

by CH347, which works in mode 0.

The signal lines in the figure can only be connected to RXDx, TXDx, and public ground. Other signal lines CTSx, RTSx, and DTRx can be selected as required, and can be suspended when not needed.

If DTR0 is connected to a 4.7KΩ pull-down resistor, DTR0 and DTR1 functions as TNOW0 and TNOW1 respectively, indicating UART sending status and controlling RS485 transceiver switching.

P1 is USB port, and USB bus includes a pair of 5V power lines and a pair of data signal lines. Generally, +5V power line is red, ground line is black, D+ signal line is green, and D- signal line is white. USB bus provides power current up to 500mA.

P2 and P3 are TTL connection pins of two serial ports, including 3.3V, GND, RXDx, TXDx, RTSx, CTSx, and DTRx pins. Can be applied level conversion device (must support high baud rate), TTL to RS232, RS485, RS422 signal conversion.

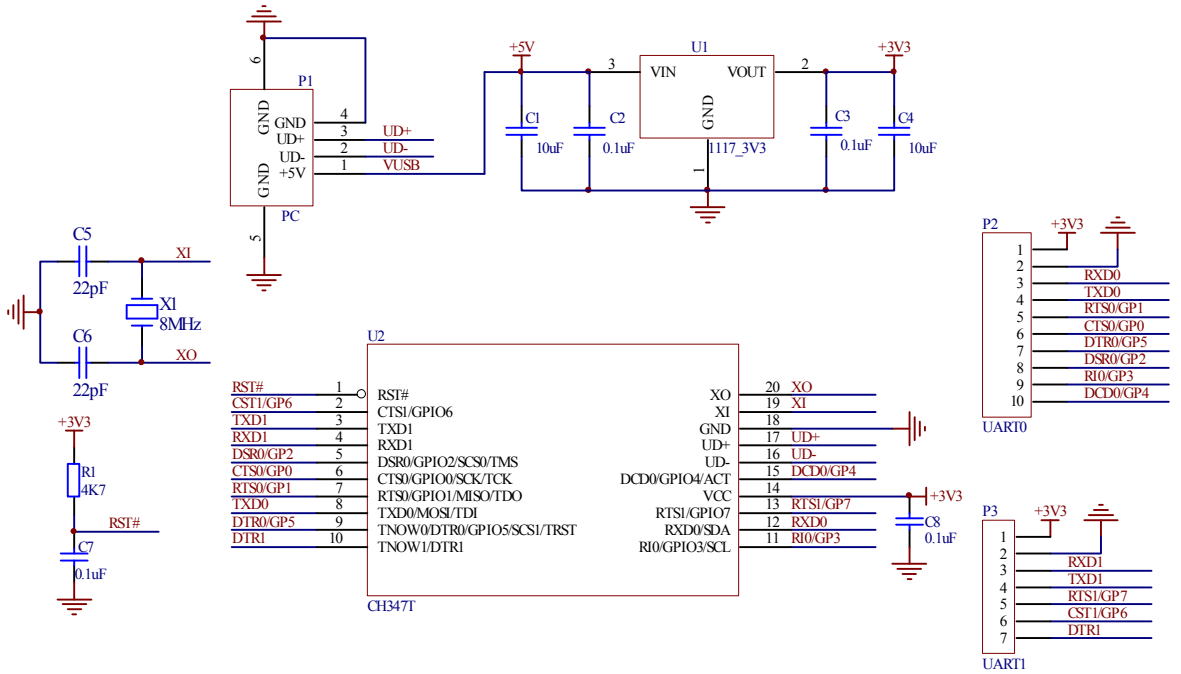
CH347 VCC pins input 3.3V power supply voltage, and each power supply pin should be connected with a power decoupling capacitor with an external capacity of about 0.1uF. C8 is the power decoupling capacitor as shown in the figure.

Crystal X1 and capacitors C5 and C6 are used for clock oscillation circuit of CH347. X1 has a frequency of 8MHz± 0.4%, and C5 and C6 are monolith or high-frequency chip capacitors with a capacity of about 22pF. R1 and C7 are optional devices.

It is recommended to add ESD protection device for USB signal line. The parasitic capacitance of ESD chip should be less than 2pF, such as ch412k.

It is recommended that the serial port peripherals and the CH347 use the same power supply. Otherwise, the I/O pin reverse current when the serial port peripherals are powered separately must be considered.

When designing the circuit board (PCB), note: the decoupling capacitor C8 should be close to the power pin connected to CH347. D+ and D- signal lines of USB ports are laid in parallel according to high-speed USB specifications to ensure characteristic impedance. Ground wire or copper cladding should be provided on both sides as far as possible to reduce signal interference from outside.

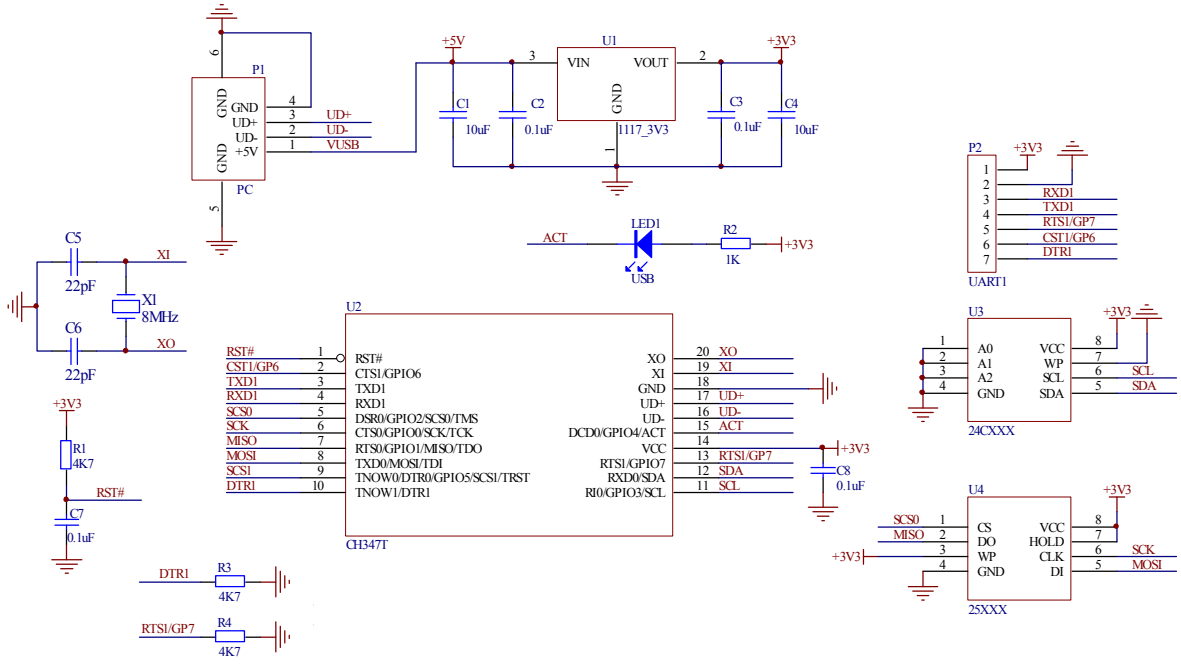


7.2. USB to SPI, USB to I2C, USB to UART 3-in-1

The figure below is the reference circuit diagram of USB to high-speed single serial port and 2-line and 4-line synchronous serial interface realized by CH347. Remove R3 but keep R4 to set the chip to work in mode 1, remove R4 but keep R3 to set the chip to work in mode 2.

P1 is USB port, and P2 is TTL connection pin of UART including VCC, GND, RXD1, TXD1, RTS1, CTS1 and DTR1 pins. Can be added level conversion device, TTL to RS232, RS485, RS422 signal conversion.

U3 is a 2-line synchronous serial interface IIC device. U4 is a 4-line synchronous serial interface SPI device. It is recommended that the peripherals use the same power supply as CH347.



7.3. USB to JTAG, USB to UART 2-in-1

The figure below is the reference circuit diagram of USB to high-speed single serial port and JTAG interface realized by CH347. Resistors R3 and R4 set the chip to work in mode 3.

P1 is USB port, and P2 is TTL connection pin of UART, including VCC, GND, RXD1, TXD1, RTS1, CTS1 and DTR1 pins. Can be added level conversion device, TTL to RS232, RS485, RS422 signal conversion.

P3 is a JTAG interface, directly connected to FPGA, CPU and other chips, can also be customized to provide 1.8V or 2.5V interface level of the single chip scheme.