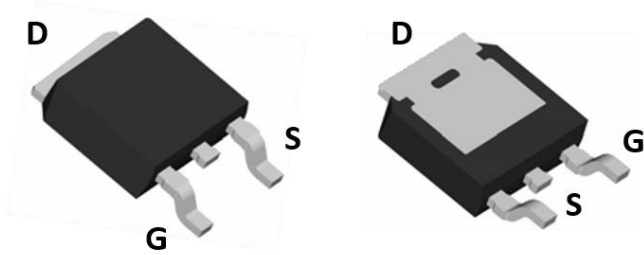
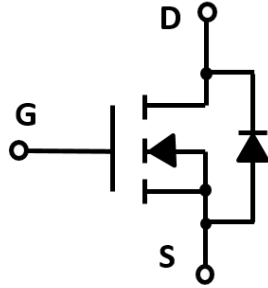


N-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} 20V
- I_D 60A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <6.0mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) <8.8mohm
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) <14mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_C=25^\circ C$	I_D	60	A
	$T_C=100^\circ C$		42	
Pulsed Drain Current ^A		I_{DM}	210	A
Total Power Dissipation	$T_C=25^\circ C$	P_D	35	W
	$T_C=100^\circ C$		18	
Single Pulse Avalanche Energy ^B		E_{AS}	195	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	4.3	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+175	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD60N02A	F2	YJD60N02A	2500	2500	25000	13" reel



YJD60N02A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.62	1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=20A$		4.5	6.0	m Ω
		$V_{GS}=2.5V, I_D=15A$		5.5	8.8	
		$V_{GS}=1.8V, I_D=10A$		8.0	14	
Diode Forward Voltage	V_{SD}	$I_S=20A, V_{GS}=0V$			1.2	V
Maximum Body-Diode Continuous Current	I_S				60	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHZ}$		2450		pF
Output Capacitance	C_{oss}			430		
Reverse Transfer Capacitance	C_{rss}			205		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=4.5V, V_{DS}=10V, I_D=15A$		65		nC
Gate-Source Charge	Q_{gs}			15		
Gate-Drain Charge	Q_{gd}			13		
Reverse Recovery Charge	Q_{rr}	$I_r=15A, di/dt=100A/us$		39		ns
Reverse Recovery Time	t_{rr}			35		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DD}=10V, I_D=10A, R_L=1\Omega$ $R_{GEN}=3\Omega$		12		ns
Turn-on Rise Time	t_r			26		
Turn-off Delay Time	$t_{D(off)}$			35		
Turn-off fall Time	t_f			10		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $T_J=25^\circ\text{C}$, $V_{DD}=15V$, $V_G=10V$, $L=0.5\text{mH}$, $R_g=25\Omega$

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

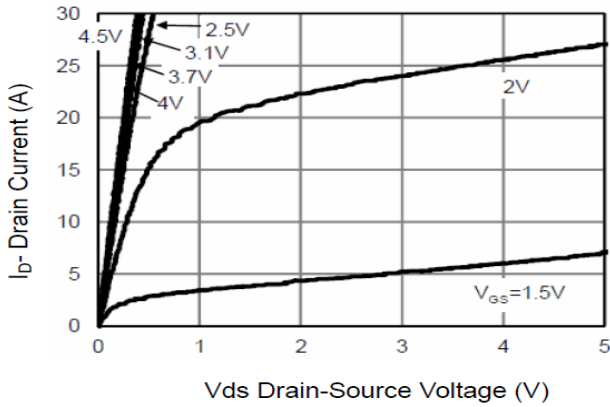


Figure1. Output Characteristics

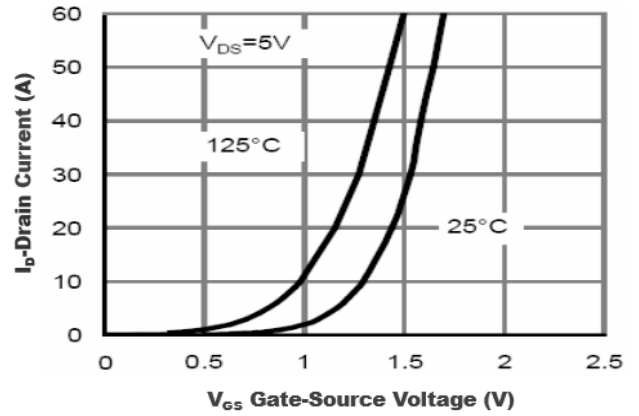


Figure2. Transfer Characteristics

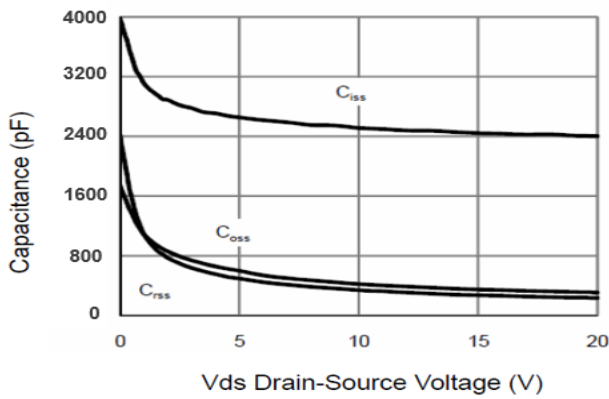


Figure3. Capacitance Characteristics

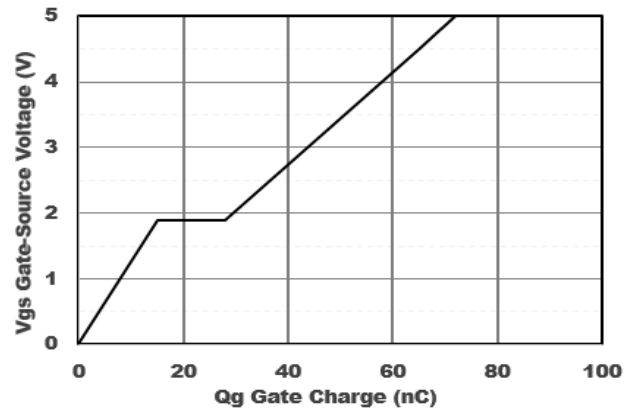


Figure4. Gate Charge

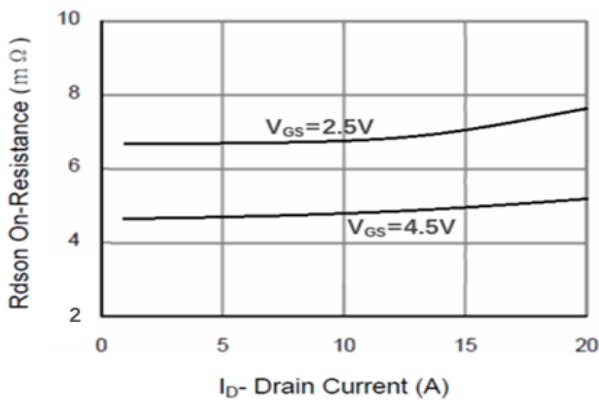


Figure5. Drain-Source on Resistance

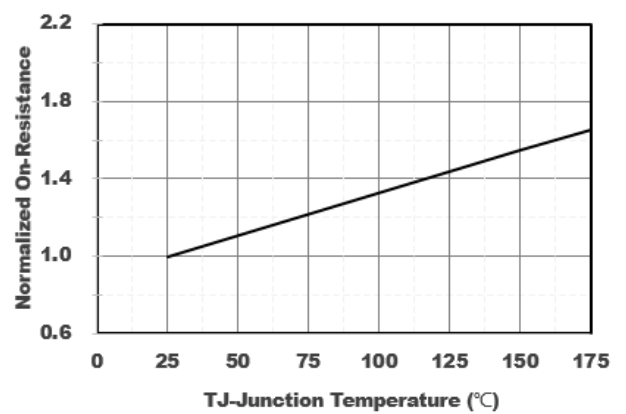
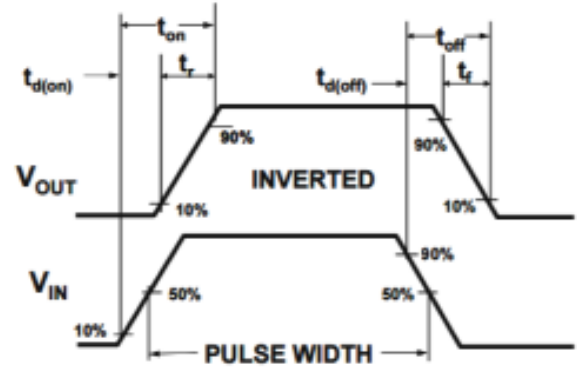
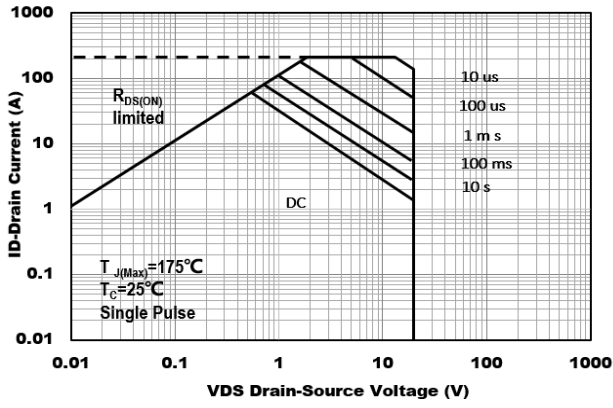


Figure6. Drain-Source on Resistance



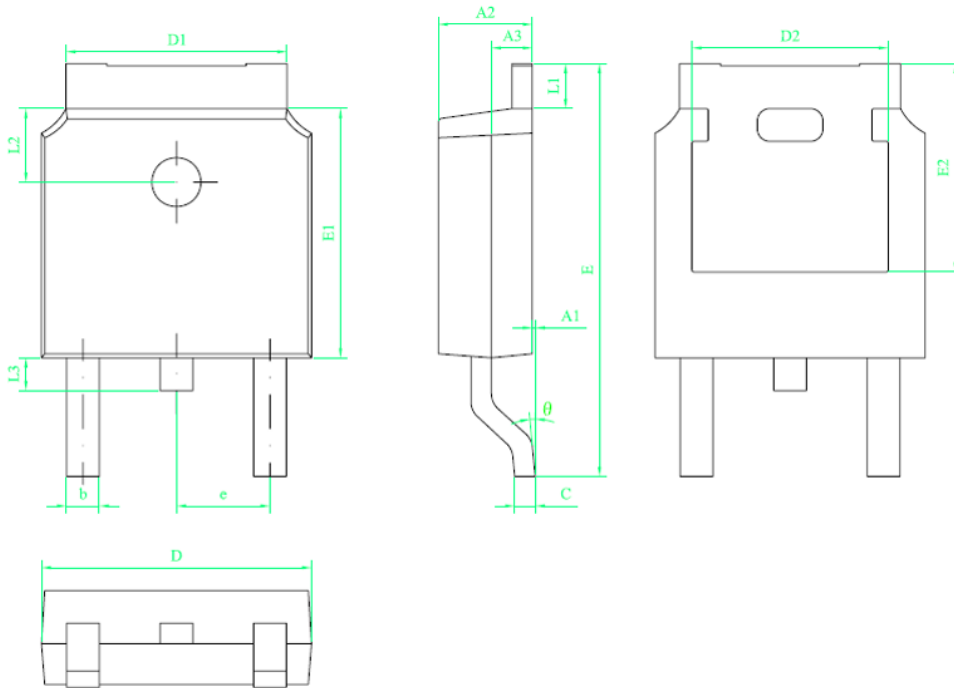
YJD60N02A





YJD60N02A

■ TO-252 Package information



符号	尺寸		
	min	nom	max
A1	0	---	0.10
A2	2.20	2.30	2.40
A3	0.90	1.00	1.10
b	0.75	---	0.85
c	0.50	---	0.60
D	6.50	6.60	6.70
D1	5.30	5.40	5.50
D2	4.70	4.80	4.90
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.20	5.30	5.40
e	2.20	2.286	2.40
L1	0.90	---	1.25
L2	1.70	1.80	1.90
L3	0.60	0.80	1.00
θ	0°	---	8°

技术要求:

1. 树脂体不应有崩裂、缺损等缺陷;
2. 树脂上下部X、Y方向偏差不超过0.20;
3. 胶体两端留胶总和宽度不超过0.50;
4. 所有单位为mm;



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