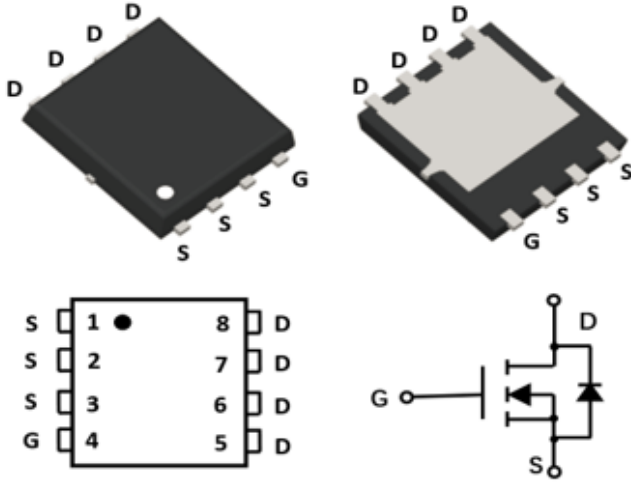


## N-Channel Enhancement Mode Field Effect Transistor

### PDFN5060



### Product Summary

- $V_{DS}$  40V
- $I_D$  200A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $< 1.35\text{mohm}$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ )  $< 2.1\text{mohm}$
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Invertors

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_c=25^\circ\text{C}$	$I_D$	200	A
	$T_c=100^\circ\text{C}$		152	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	600	A
Avalanche energy <sup>B</sup>		$E_{AS}$	625	mJ
Total Power Dissipation <sup>C</sup>	$T_c=25^\circ\text{C}$	$P_D$	120	W
	$T_c=100^\circ\text{C}$		48	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10\text{S}$	$R_{\theta JA}$	14	19	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		37	48	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.85	1.04	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG200G04AR	F1	G200G04AR	5000	10000	100000	13" reel



# YJG200G04AR

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	1.1	1.35	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	1.5	2.1	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	-	1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	200	A
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain	-	3.4	-	Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	-	7100	-	pF
Output Capacitance	C <sub>oss</sub>		-	1298	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	55	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g(10V)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A	-	132	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	25	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	24.6	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us	-	54	-	ns
Reverse Recovery Time	t <sub>rr</sub>		-	56	-	
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =20A R <sub>GEN</sub> =2.2Ω	-	18.8	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	70.1	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	136.8	-	
Turn-off fall Time	t <sub>f</sub>		-	92.3	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=25V, V<sub>G</sub>=10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=50A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation PDSM is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



## ■ Typical Performance Characteristics

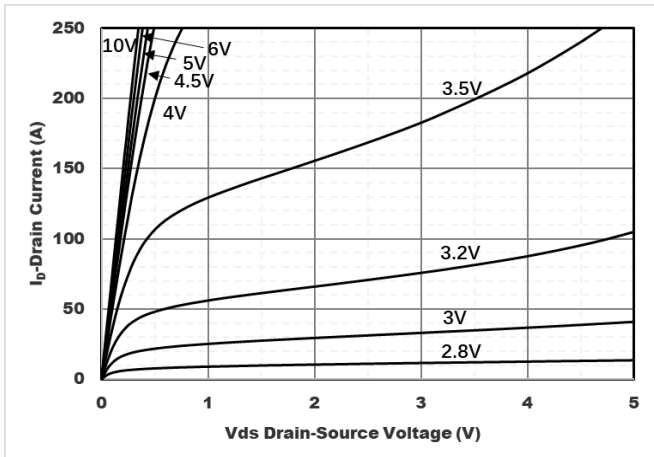


Figure1. Output Characteristics

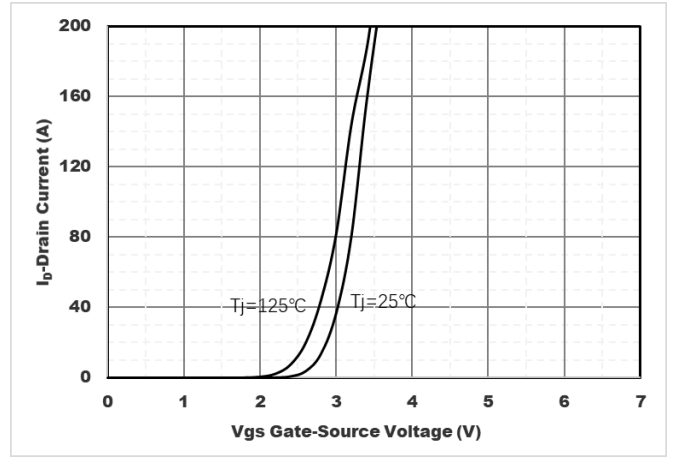


Figure2. Transfer Characteristics

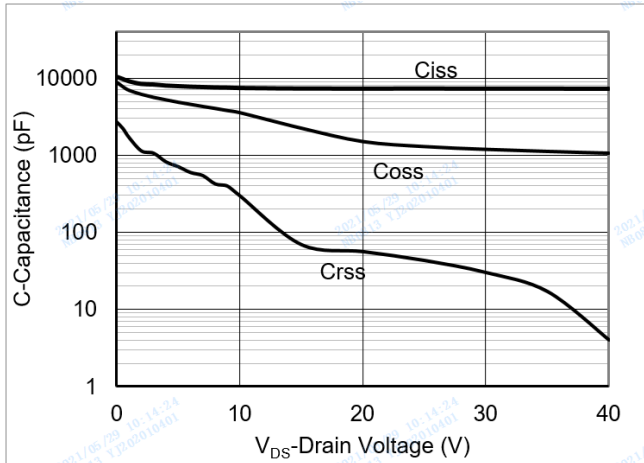


Figure3. Capacitance Characteristics

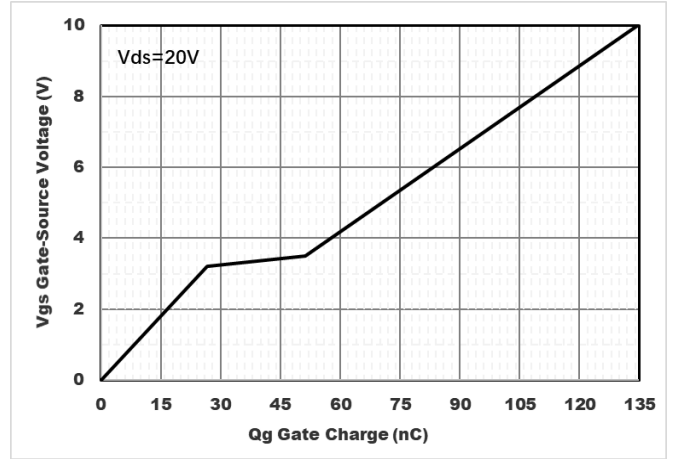


Figure4. Gate Charge

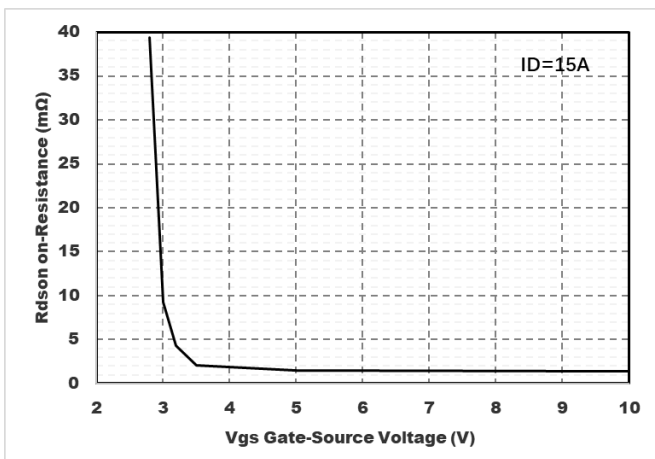


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

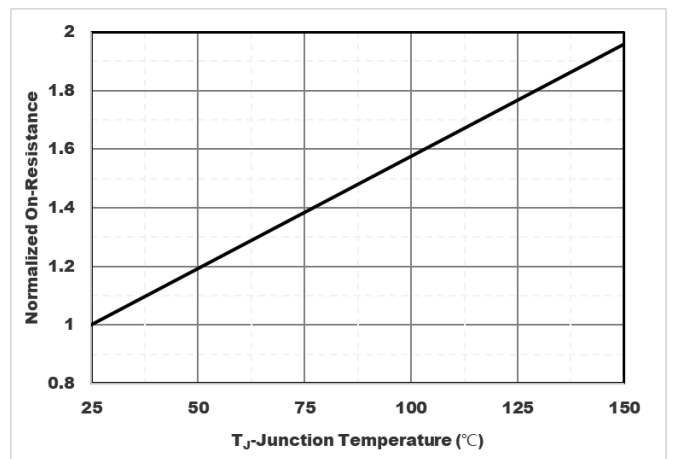


Figure6. Normalized On-Resistance



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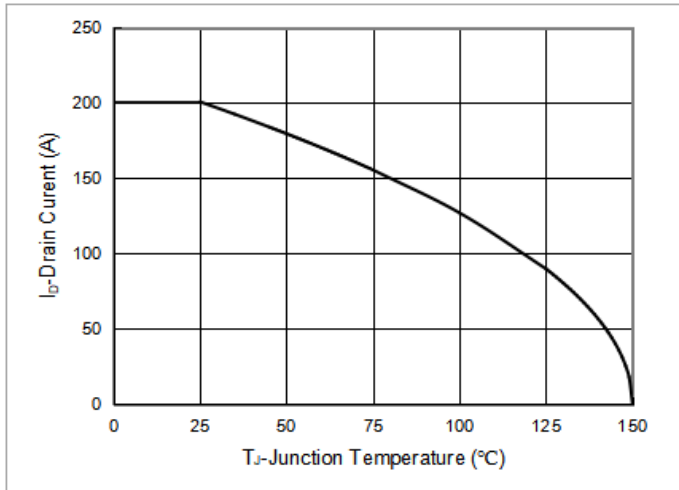


Figure7. Drain current

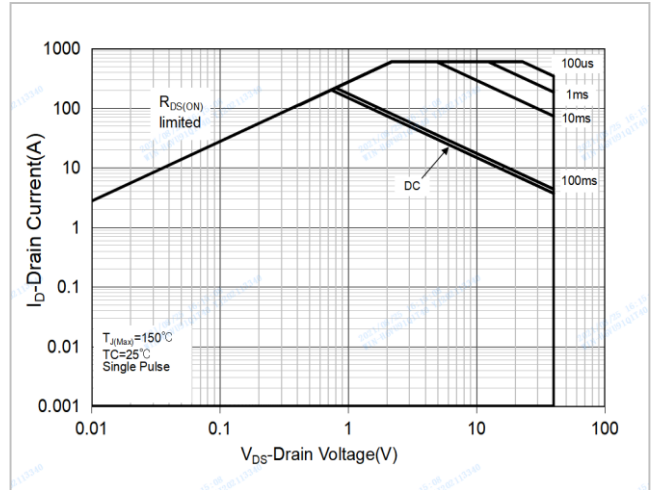


Figure8.Safe Operation Area

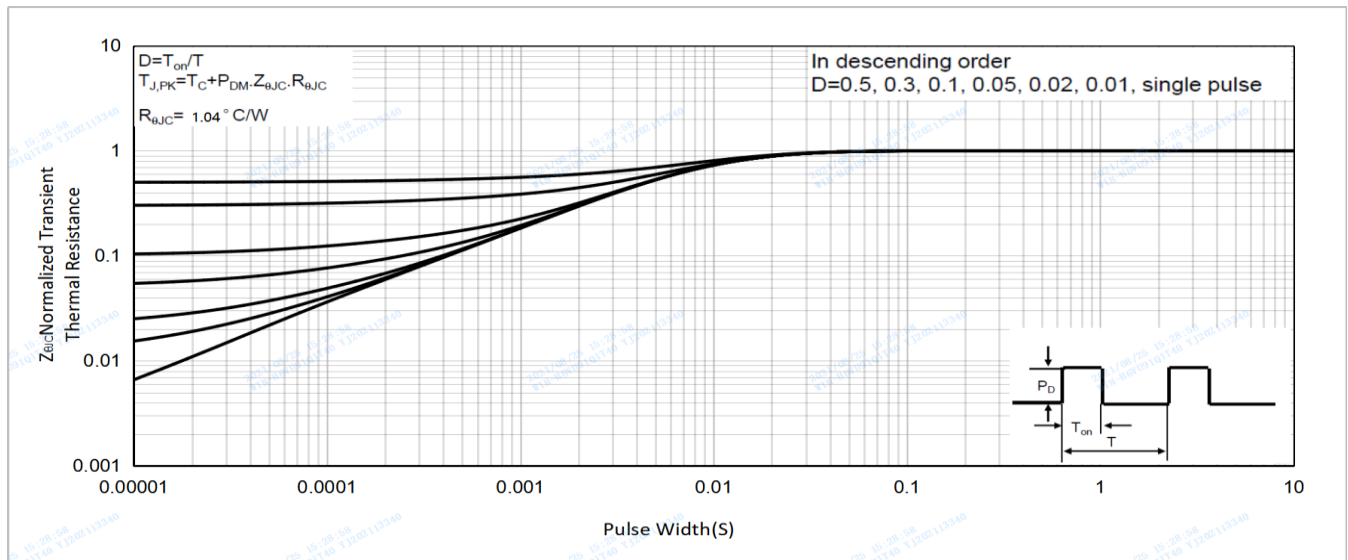
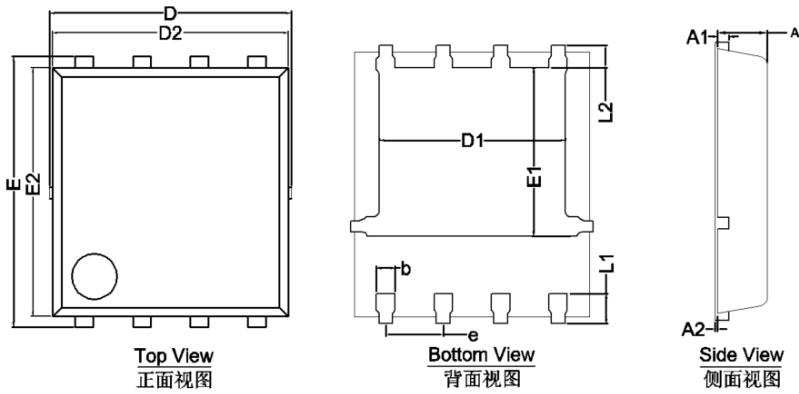


Figure9.Normalized Maximum Transient thermal impedance

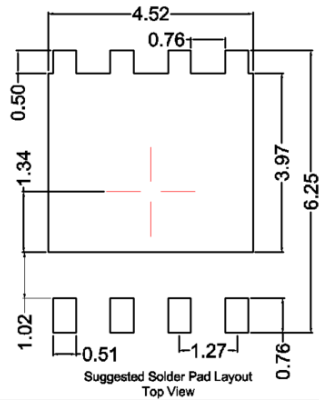


# YJG200G04AR

## ■ PDFN5060-8L-D-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Note:  
 1. Controlling dimension: In millimeters.  
 2. General tolerance:  $\pm 0.10$ mm.  
 3. The pad layout is for reference purposes only.



## YJG200G04AR

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