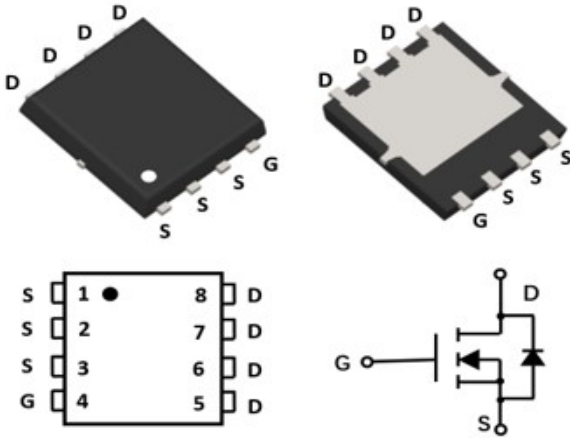


N-Channel Enhancement Mode Field Effect Transistor

PDFN 5X6



Product Summary

- V_{DS} 100V
- I_D 90A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <5.0mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <7.1mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_c=25^\circ\text{C}$	I_D	90	A
	$T_c=100^\circ\text{C}$		57	
Pulsed Drain Current ^A		I_{DM}	360	A
Avalanche energy ^B		E_{AS}	400	mJ
Total Power Dissipation ^C	$T_c=25^\circ\text{C}$	P_D	120	W
	$T_c=100^\circ\text{C}$		48	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10\text{S}$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.84	1.04	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG90G10A	F1	YJG90G10A	5000	10000	100000	13" reel



YJG90G10A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		4.1	5.0	mΩ
		V _{GS} =4.5V, I _D =20A		5.7	7.1	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				90	A
Gate resistance	R _G	f=1MHz, Open drain		0.9		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		3927		pF
Output Capacitance	C _{oss}			1658		
Reverse Transfer Capacitance	C _{rss}			36		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =20A		66		nC
Gate-Source Charge	Q _{gs}			15.4		
Gate-Drain Charge	Q _{gd}			10.6		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us		82		
Reverse Recovery Time	t _{rr}			64		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =20A R _{GEN} =2.2Ω		17.6		ns
Turn-on Rise Time	t _r			34.7		
Turn-off Delay Time	t _{D(off)}			43.8		
Turn-off fall Time	t _f			61.4		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=2Mh, I_{AS}=31A.

C. P_g is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation PDSM is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



■ Typical Performance Characteristics

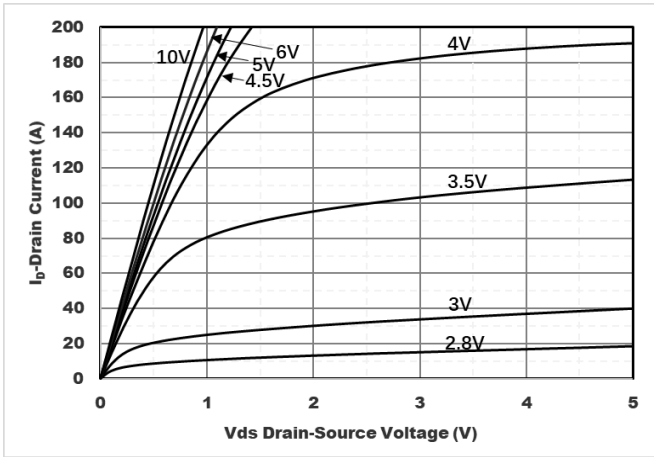


Figure1. Output Characteristics

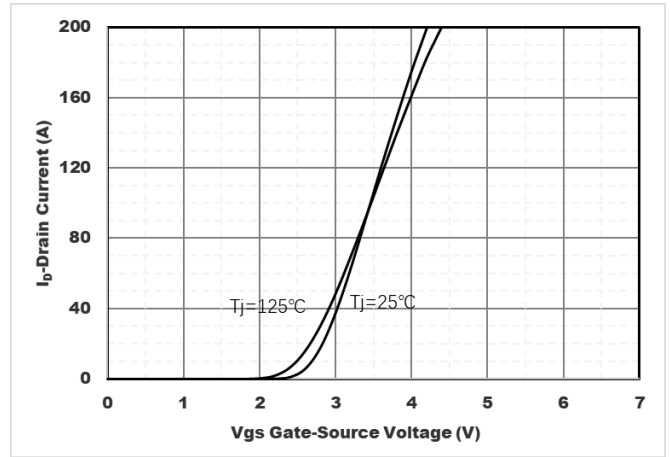


Figure2. Transfer Characteristics

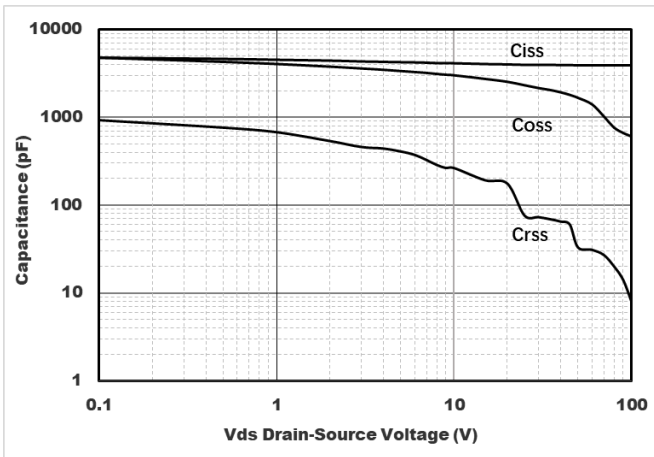


Figure3. Capacitance Characteristics

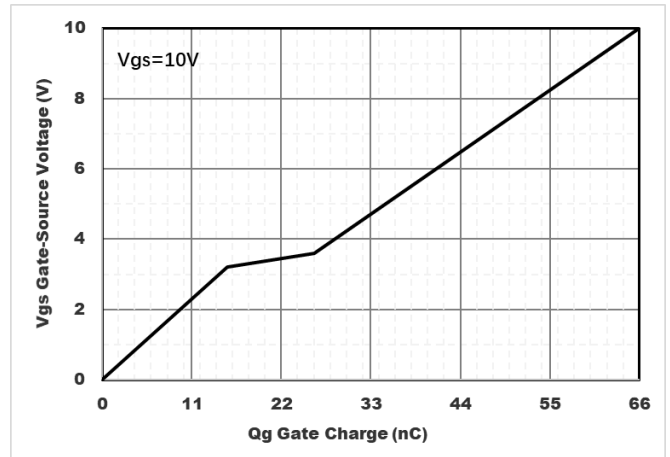


Figure4. Gate Charge

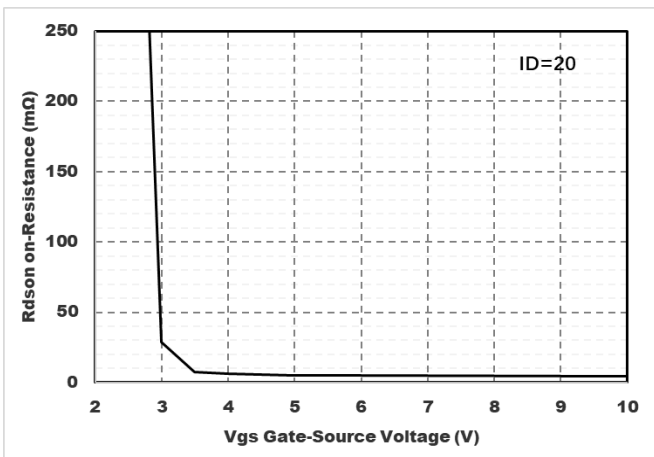


Figure5. : On-Resistance vs. Gate to Source Voltage

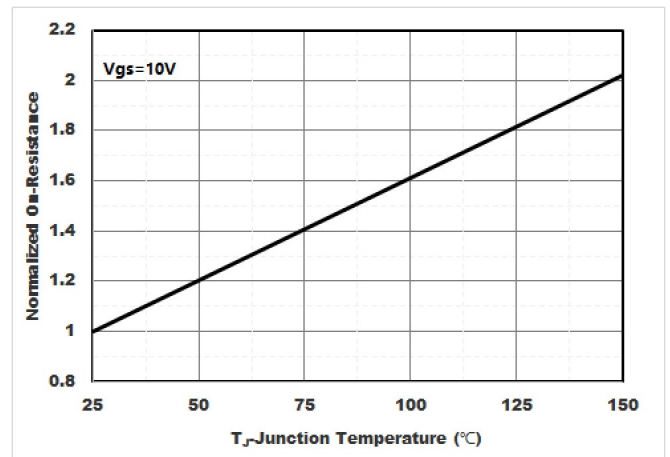


Figure6. Normalized On-Resistance



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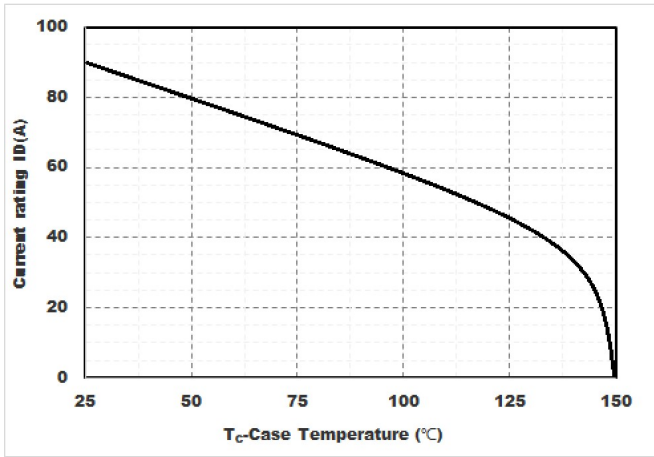


Figure7. Drain current

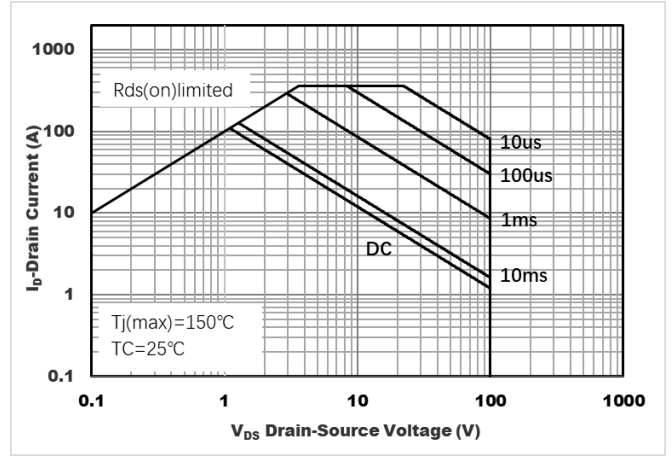


Figure8.Safe Operation Area

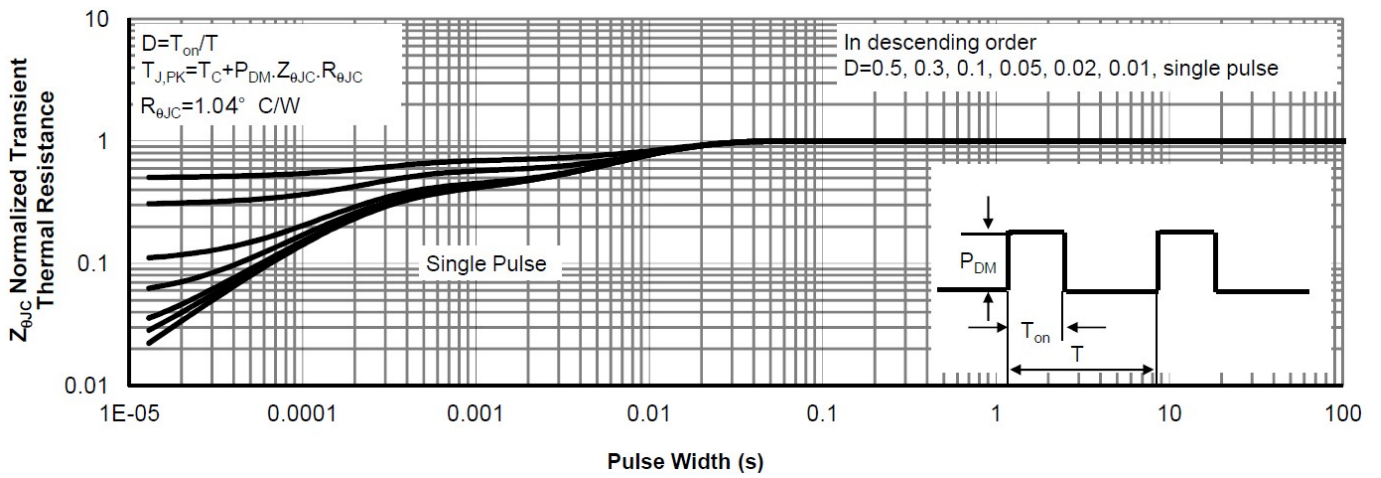
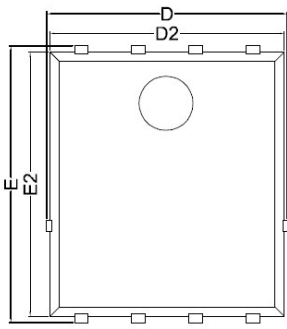


Figure9.Normalized Maximum Transient thermal impedance

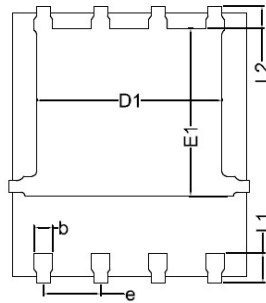


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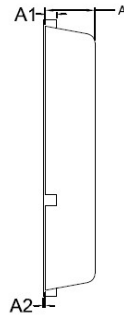
■ PDFN5x6 Package information



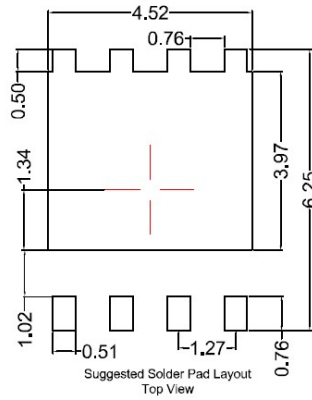
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



YJG90G10A

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